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Pentium® Processors and Related Products

In 1993, Intel introduced the Pentium® processor, the fifth generation processor based on the Intel Architecture. The Pentium processor utilizes advanced design techniques, superscalar technology and enhanced floating-point to increase performance of today's applications and enable tomorrow's emerging technologies. The newest addition to the Pentium processor family is the Pentium processor with MMX™ technology introduced in January 1997 (for information on the Pentium Pro and Pentium II processors please see the Pentium Pro and Pentium II Processors and Related Products manual). Pentium processors with MMX technology, combined with software applications that use the MMX technology instruction set, give PCs a new level of multimedia performance including higher quality audio, rich colors, realistic 3D rendering and smooth animation and video. Pentium processors, including the Pentium processor with MMX technology, are fully code-compatible with previous members of the Intel Architecture family of microprocessors, preserving the value of user's software investment.

Pentium processors, as well as Pentium processor with MMX technology, are ideal for embedded applications. Intel's commitment to the embedded market segment now includes support for these high-performance processors.

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Pentium® Processor and Related Products

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Chapter 1: Intel Architecture

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Intel MMX™ Technology Overview

March 1996

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Intel MMX™ Technology Overview

INTRODUCTION

The volume and complexity of data processed by today's personal computer are increasing exponentially, placing incredible demands on the microprocessor. New communications, games and "edutainment" applications feature video, 3D graphics, animation, audio and virtual reality, all of which demand ever increasing levels of performance.

Intel's MMX™ technology is designed to accelerate multimedia and communications applications. The technology includes new instructions and data types that allow applications to achieve a new level of performance. It exploits the parallelism inherent in many multimedia and communications algorithms, yet maintains full compatibility with existing operating systems and applications.

MMX technology is the most significant enhancement to the Intel Architecture since the Intel386™ processor, which extended the architecture to 32 bits. Processors enabled with MMX technology will deliver enough performance to execute compute-intensive communications and multimedia tasks with headroom left to run other tasks or applications. They allow software developers to design richer, more exciting applications for the PC. The volume of MMX technology-enabled systems will grow rapidly in 1997 as the technology is incorporated into multiple processor generations from Intel.

The definition of MMX technology resulted from a joint effort between Intel's microprocessor architects and software developers. A wide range of software applications was analyzed, including graphics, MPEG video, music synthesis, speech compression, speech recognition, image processing, games, video conferencing and more. These applications were broken down to identify the most compute-intensive routines, which were then analyzed in details using advanced computer-aided engineering tools. The results of this extensive analysis showed many common, fundamental characteristics across these diverse software categories. The key attributes of these applications were:

- Small integer data types (for example: 8-bit graphics pixels, 16-bit audio samples)
- Small, highly repetitive loops
- Frequent multiplies and accumulates
- Compute-intensive algorithms
- Highly parallel operations

MMX technology is designed as a set of basic, general purpose integer instructions that can be easily applied to the needs of the wide diversity of multimedia and communications applications. The highlights of the technology are:

- Single Instruction, Multiple Data (SIMD) technique
- 57 new instructions
- Eight 64-bit wide MMX registers
- Four new data types

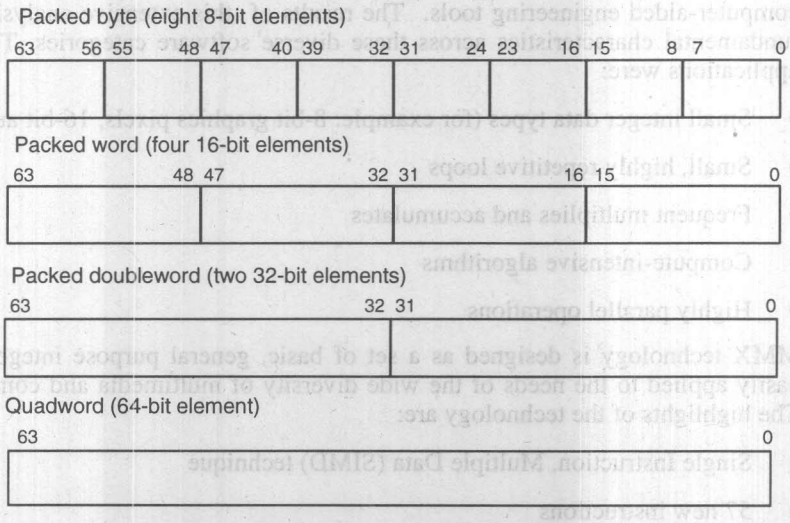
The basis for MMX technology is a technique called Single Instruction, Multiple Data (SIMD). This allows many pieces of information to be processed with a single instruction, providing parallelism that greatly increases performance. This technology combined with the IA superscalar architecture will provide substantial performance enhancement to the PC platform. MMX technology is integrated into Intel Architecture processors in a way that maintains full compatibility with existing operating systems, including MS DOS*, Windows* 3.1, Windows 95, OS/2* and Unix*. In addition, the full base of Intel architecture software will run on MMX technology-enabled systems.

MMX technology was defined to be simple. MMX technology is general enough to address the needs of a large domain of PC applications built from current and future algorithms. MMX instructions are not privileged; they can be used in applications, codecs, algorithms, and drivers.

- Packed byte — Eight bytes packed into one 64-bit quantity
- Packed word — Four 16-bit words packed into one 64-bit quantity
- Packed doubleword — Two 32-bit double words packed into one 64-bit quantity
- Quadword — One 64-bit quantity

As an example, graphics pixel data are generally represented in 8-bit integers, or bytes. With MMX technology, eight of these pixels are packed together in a 64-bit quantity and moved into an MMX register. When an MMX instruction executes, it takes all eight of the pixel values at once from the MMX register, performs the arithmetic or logical operation on all eight elements in parallel, and writes the result into an MMX register.

Data Types in 64-bit Registers



COMPATIBILITY

MMX technology retains its full compatibility with existing operating systems and applications by aliasing its registers and state upon the IA floating-point registers and state. Therefore, no new registers or states are added to support MMX technology. This means that the operating system uses the standard mechanisms for interacting with the floating point state to save and restore MMX code. For example, during a task switch, the operating system would use an FSAV and FRSTR to preserve either floating point or MMX code. Aliasing the MMX state upon the floating-point state does not preclude applications from executing both MMX technology routines and floating point routines.

Floating-point instructions that save/restore the floating-point state also handle the MMX state (for example, during context switching). The same techniques used by the floating-point architecture to interface with the operating system are used by MMX technology. MMX technology does not introduce any new exception or state information, so today's operating systems can enable applications using MMX instructions.

DETECTING THE PRESENCE OF MMX™ TECHNOLOGY

Detecting the existence of MMX technology on an Intel microprocessor is done by executing the CPUID instruction and checking a set bit. This gives software developers the flexibility to determine the specific code in their software to execute. During install or run time the software can query the microprocessor to determine if MMX technology is supported and install or execute the code that includes, or does not include, MMX instructions based on the result.

INSTRUCTIONS

The MMX instructions cover several functional areas including:

- Basic arithmetic operations such as add, subtract, multiply, arithmetic shift and multiply-add
- Comparison operations
- Conversion instructions to convert between the new data types - pack data together, and unpack from small to larger data types
- Logical operations such as AND, AND NOT,OR, and XOR
- Shift operations
- Data Transfer (MOV) instructions for MMX register-to-register transfers, or 64-bit and 32-bit load/store to memory

Arithmetic and logical instructions are designed to support the different packed integer data types. These instructions have a different op code for each data type supported. As a result, the new MMX technology instructions are implemented with 57 op codes.

MMX technology uses general-purpose, basic instructions that are fast and are easily assigned to the parallel pipelines in Intel processors. By using this general-purpose approach, MMX technology provides performance that will scale well across current and future generations of Intel processors.

MMX™ Instruction Set Summary

The instructions and corresponding mnemonics in the table below are grouped by function categories.

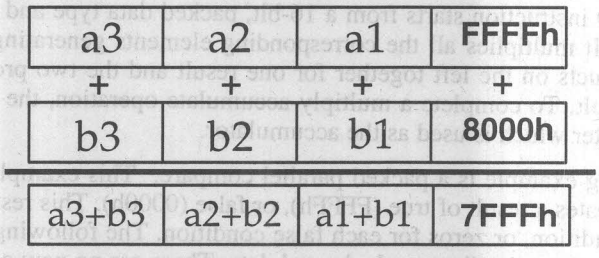
If an instruction supports multiple data types—byte (B), word (W), doubleword (DW), or quadword (QW), the datatypes are listed in brackets. Only one data type may be chosen for a given instruction. For example, the base mnemonic PADD (packed add) has the following variations: PADDB, PADDW, and PADDD. The number of opcodes associated with each base mnemonic is listed.

Category	Mnemonic	Number of Different Opcodes	Description
Arithmetic	PADD[B,W,D]	3	Add with wrap-around on [byte, word, doubleword]
	PADDS[B,W]	2	Add signed with saturation on [byte, word]
	PADDUS[B,W]	2	Add unsigned with saturation on [byte, word]
	PSUB[B,W,D]	3	Subtraction with wrap-around on [byte, word, doubleword]
	PSUBS[B,W]	2	Subtract signed with saturation on [byte, word]
	PSUBUS[B,W]	2	Subtract unsigned with saturation on [byte, word]
	PMULHW	1	Packed multiply high on words
	PMULLW	1	Packed multiply low on words
	PMADDWD	1	Packed multiply on words and add resulting pairs
Comparison	PCMPEQ[B,W,D]	3	Packed compare for equality [byte, word, doubleword]
	PCMPGT[B,W,D]	3	Packed compare greater than [byte, word, doubleword]
Conversion	PACKUSWB	1	Pack words into bytes (unsigned with saturation)
	PACKSS[WB,DW]	2	Pack [words into bytes, doublewords into words] (signed with saturation)
	PUNPCKH [BW,WD,DQ]	3	Unpack (interleave) high-order [bytes, words, doublewords] from MMX™ register
	PUNPCKL [BW,WD,DQ]	3	Unpack (interleave) low-order [bytes, words, doublewords] from MMX register
Logical	PAND	1	Bitwise AND
	PANDN	1	Bitwise AND NOT
	POR	1	Bitwise OR
	PXOR	1	Bitwise XOR
Shift	PSLL[W,D,Q]	6	Packed shift left logical [word, doubleword, quadword] by amount specified in MMX register or by immediate value
	PSRL[W,D,Q]	6	Packed shift right logical [word, doubleword, quadword] by amount specified in MMX register or by immediate value
	PSRA[W,D]	4	Packed shift right arithmetic [word, doubleword] by amount specified in MMX register or by immediate value
Data Transfer	MOV[D,Q]	4	Move [doubleword, quadword] to MMX register or from MMX register
FP & MMX State Mgmt	EMMS	1	Empty MMX state

Instruction Examples

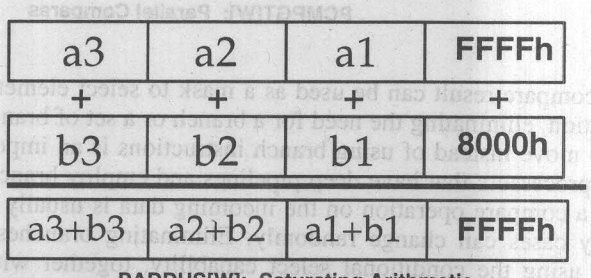
The following section will describe briefly five examples of MMX instructions. For illustration, the data type shown in this section will be the 16-bit word data type; most of these operations also exist for 8-bit or 32-bit packed data types.

The following example shows a packed add word with wrap around. It performs four additions of the eight, 16-bit elements, with each addition independent of the others and in parallel. In this case, the right-most result exceeds the maximum value representable in 16-bits—thus it wraps-around. This is the way regular IA arithmetic behaves. FFFFh + 8000h would be a 17 bit result. The 17th bit is lost because of wrap around, so the result is 7FFFh.



PADD[W]: Wrap-around Add

The following example is for a packed add word with unsigned saturation. This example uses the same data values from before. The right-most add generates a result that does not fit into 16 bits; consequently, in this case saturation occurs. Saturation means that if addition results in overflow or subtraction results in underflow, the result is clamped to the largest or the smallest value representable. For an unsigned, 16-bit word, the largest and the smallest representable values are FFFFh and 0x0000; for a signed word the largest and the smallest representable values are 7FFFh and 0x8000. This is important for pixel calculations where this would prevent a wrap-around add from causing a black pixel to suddenly turn white while, for example, doing a 3D graphics Gouraud shading loop.



PADDUS[W]: Saturating Arithmetic

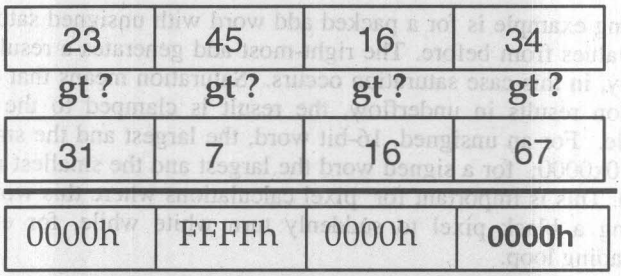
The specific instruction here is Packed Add Unsigned Saturation Word (PADDUSW). A complete set of ADD operations exists for signed and unsigned cases. The number FFFFh, treated as unsigned (65,535 decimal), is added to 0x8000 unsigned (32,768), and the result saturates to FFFFh - the largest representable unsigned 16-bit value.

There is no "saturation mode bit" as a new mode bit would require a change to the operating system. Separate instructions are used to generate wrap-around and saturating results.

The next example shows the key instruction used for multiply-accumulate operations, which are fundamental to many signal processing algorithms like vector-dot-products, matrix multiplies, FIR and IIR Filters, FFTs, DCTs etc. This instruction is the packed multiply add (PMADD).

The PMADD instruction starts from a 16-bit, packed data type and generates a 32-bit packed, data type result. It multiplies all the corresponding elements generating four 32-bit results, and adds the two products on the left together for one result and the two products on the right together for the other result. To complete a multiply-accumulate operation, the results would then be added to another register which is used as the accumulator.

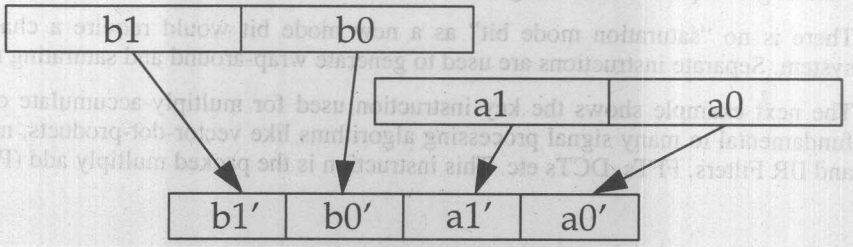
The following example is a packed parallel compare. This example compares four pairs of 16-bit words. It creates a result of true (FFFFh), or false (0000h). This result is a packed mask of ones for each true condition, or zeros for each false condition. The following example shows an example of a compare "greater than" on packed word data. There are no new condition code flags, nor are any existing IA condition code flags affected by this instruction.



PCMPGT[W]: Parallel Compares

The packed compare result can be used as a mask to select elements from different inputs using a logical operation, eliminating the need for a branch or a set of branch instructions. The ability to do a conditional move instead of using branch instructions is an important performance enhancement in advanced processors that have deep pipelines and employ branch prediction. A branch based on the result of a compare operation on the incoming data is usually difficult to predict, as incoming data in many cases can change randomly. Eliminating branches that are used to perform data selection by using the conditional select capability, together with the parallelism of the MMX instruction set, is an important performance enhancement feature of the MMX technology.

The following is an example of a pack instruction. It takes four 32-bit values and packs them into four 16-bit values, performing saturation if one of the 32-bit source values does not fit into a 16-bit result. There are also instructions that perform the opposite - unpack, for example, a packed byte data type into a packed word data type.



PACKSS[DW]: Pack Instruction

The pack and unpack instructions exist to facilitate conversion between the new packed data types. These are especially important when an algorithm needs higher precision in its intermediate calculations, as in image filtering. A filter on an image usually involves a set of multiply operations between filter coefficients and a set of adjacent image pixels, accumulating all the values together. These multiplies and accumulations need more precision than 8-bits, the original data type of the pixels. The solution is to unpack the image's 8-bit pixels into 16-bit words, perform the calculations in 16-bit words without concern for overflow, then pack back to 8-bit pixels before storing the filtered pixels to memory.

APPLICATION EXAMPLES

The following section describes example uses of the MMX instruction set to implement basic coding structures:

Conditional Select

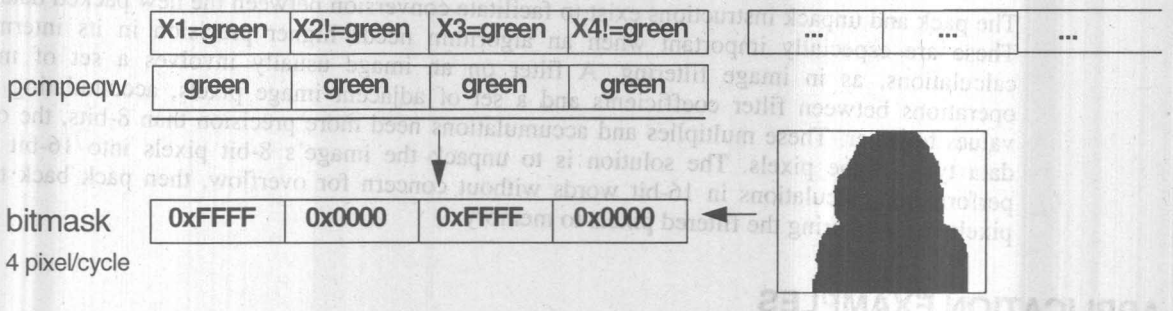
Multimedia applications must process large sets of data. In some cases there is a need to select the data based on a condition query performed on the incoming data. Intel has been able to improve performance in its family of processors by implementing micro-architectural features for increased performance and deeper pipelines. Branch prediction is an important part of making the pipelines run efficiently, as a misprediction can cause the pipelines to flush and degrade performance. The following example shows an efficient way to reduce the need to use branch instructions, especially those that are data dependent, and thus very difficult to predict. The Chroma Keying example demonstrates how conditional selection using the MMX instruction set removes branch mispredictions, in addition to performing multiple selection operations in parallel. Text overlay on a graphics/video background, and sprite overlays in games are some of the other operations that would benefit from this technique.

Chroma Keying

Most have seen the television weather man overlaid on the image of a weather map. In this example we use a green screen to overlay an image of a woman on a picture of spring blossom. We'll illustrate this example by processing four 16-bit pixels in parallel. The instructions also allow the processing of eight 8-bit pixels in parallel for a substantial performance speed-up potential.

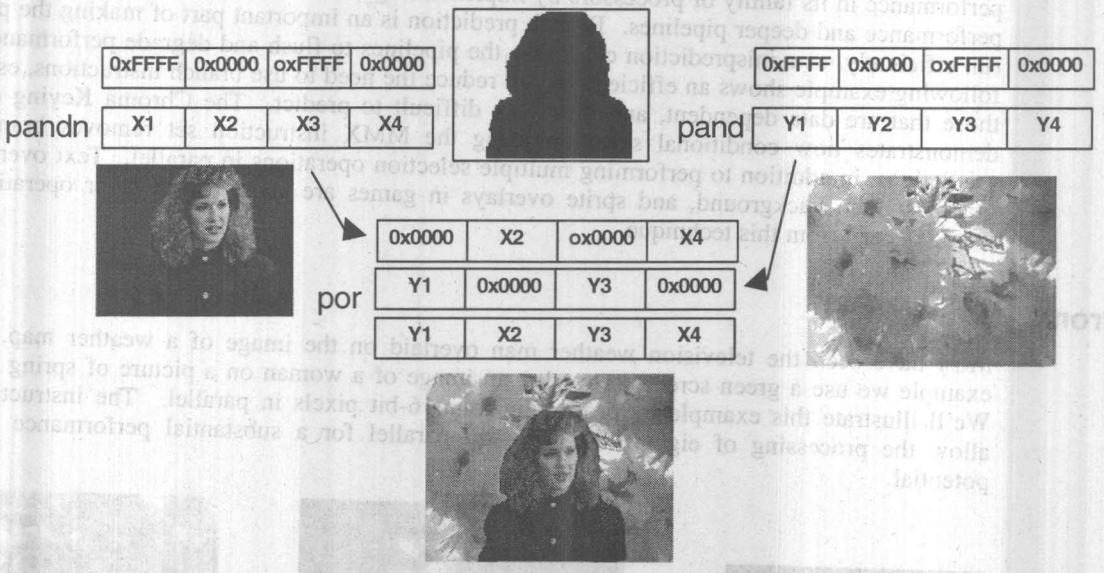


First we'll take four pixels from the picture with the woman on a green background. The top row of the data below represents pixels that alternate between green, not green, green, and not green. The compare instruction builds a mask for that data. That mask is a sequence of words that are all ones or all zeros representing the Boolean values of true and false. We now know what is the unwanted background and what we want to keep. This is shown below using a shadow picture.



This mask is now used on the same four pixels from the picture with the woman and the equivalent four pixels from the Spring blossom. The "AND NOT" and "AND" instructions use the mask to identify which pixels to keep from the Spring blossom and the woman. They also turn the unwanted pixels to zeros. The "OR" instruction builds the final picture. Four pixels were mapped using only four MMX instructions without any branches.

In working through this example, the PANDN instruction inverts all the bits in mask before applying the AND operation.

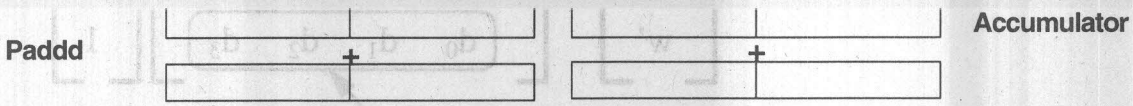


Without MMX technology, each pixel is processed separately and requires a conditional branch. Using MMX instructions, eight 8-bit pixels can be processed in parallel and no conditional branches are involved.

Vector Dot Product

The vector dot product is one of the most basic algorithms used in signal-processing of natural data such as images, audio, video and sound. The following example shows how the PMADD instruction helps speed up algorithms using vector dot products. The PMADD instruction will handle four multiplies and two additions at a time. Coupled with a PADD instruction, as described before, eight multiply-accumulate operations are performed. These eight element vectors fit nicely into two PMADD instructions and two PADD instructions.

Assuming that the precision supported by the PMADD instruction is sufficient, this dot-product example on eight-element vectors can be completed using eight MMX instructions: Two PMADDs, two more PADDs, two shifts (if needed to fix the precision after the multiply operation), and two memory moves to load one of the vectors (the other vector is loaded by the PMADD instruction which can have one of its operands come from memory).



Note: Input data and coefficients are 16-bit precision.
If not, first unpack to 16 bit.

Comparing instruction counts with and without MMX technology for this operation yields the following:

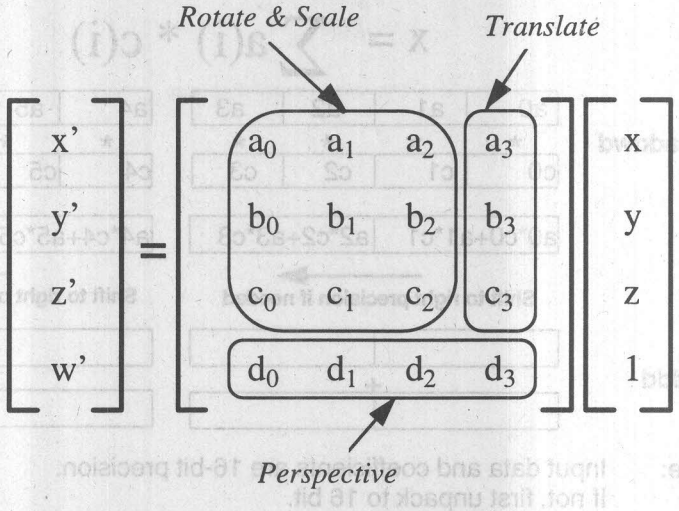
	Number of Instructions without MMX™ Technology	Number of MMX Instructions
Load	16	4
Multiply	8	2
Shift	8	2
Add	7	1
Miscellaneous	-	3
Store	1	1
Total	40	13

With MMX technology, one third of the number of instructions is needed.

Most MMX instructions can be executed in one clock cycle, so the performance improvement will be more dramatic than the simple ratio of instruction counts.

Matrix Multiply

Exciting new 3D games are coming to market every day. Typically, computations that manipulate 3D objects are based on 4-by-4 matrices that are multiplied with four element vectors many times. The vector has the X,Y, Z and perspective corrective information for each pixel. The 4-by-4 matrix is used to rotate, scale, translate and update the perspective corrective information for each pixel. This 4-by-4 matrix is applied to many vectors.



$$x' = a_0x + a_1y + a_2z + a_3$$

Applications which already use 16-bit integer or fixed-point data are able to make extensive use of the PMADD instruction. There would be one PMADD instruction per row in the matrix, for a total of four. Comparing instruction counts with and without MMX technology for this operation yields the following:

	Number of Instructions without MMX™ Technology	Number of MMX instructions
Load	32	6
Multiply	16	4
Add	12	2
Miscellaneous	8	12
Store	4	4
Total	72	28

With MMX technology, less than one half of the number of instructions without MMX technology is needed.

24-Bit Color

The MMX instruction set offers graphical applications the opportunity to move from 8-bit or 16-bit color lookup table to 24-bit, or "true" color, a feature which will greatly enhance the realism of a game's graphics. In many cases, this can be done in the same amount of time that is currently required for 8-bit graphics. For 24-bit and 32-bit colors, red, green and blue are each represented by 8-bit values. There are eight additional bits in 32-bit color for alpha value.

Image compositing and alpha blending are operations that can be performed on 24-bit color images.

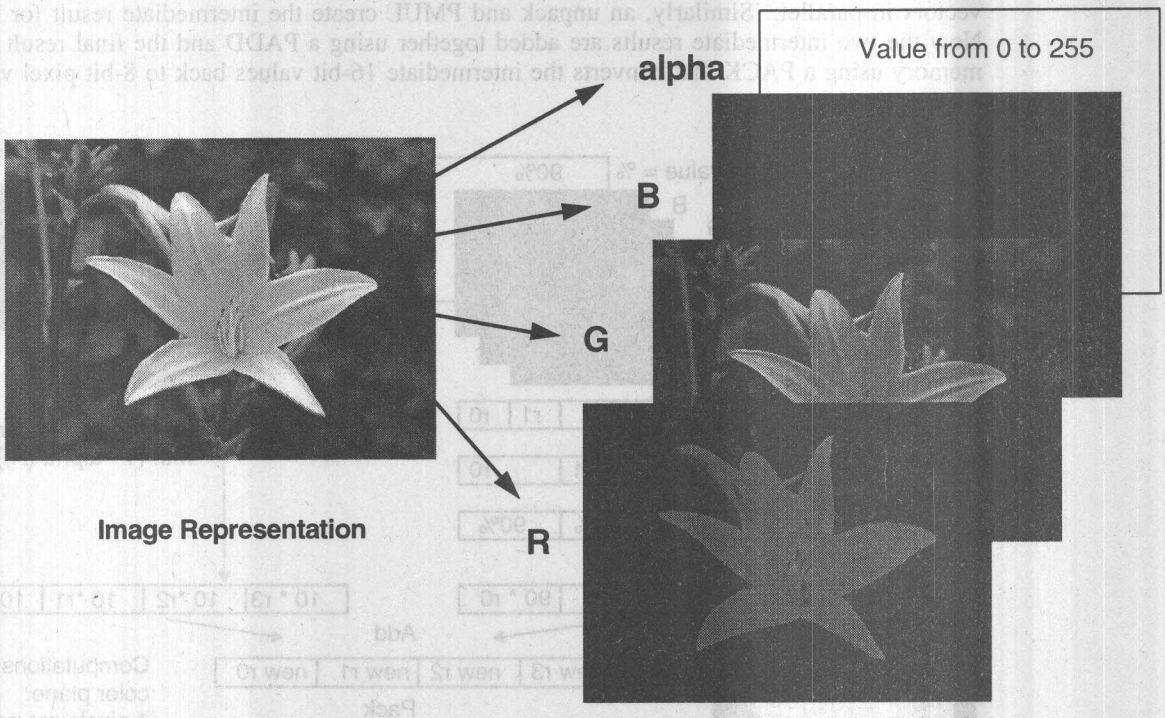


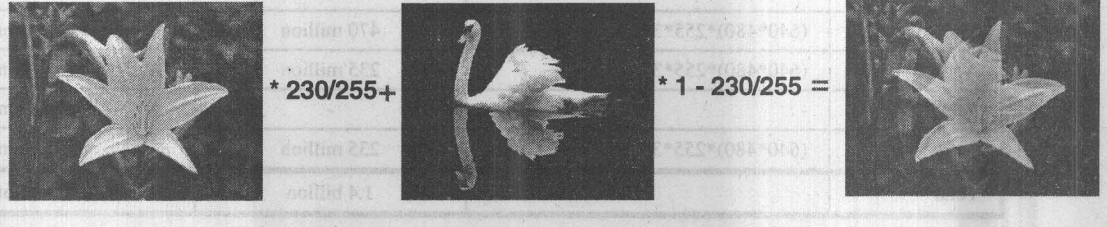
Image Dissolve Using Alpha Blending

This example shows how the MMX instruction set will speed up image compositing. In this example, a flower will dissolve into a swan. The screen starts with a picture of the flower. As the flower gradually fades away, the swan gradually appears.

The math for the dissolve is a straight-forward function. Alpha determines the intensity of the flower. At full intensity, the flower's 8-bit alpha value is FFH, or 255. By plugging 255 in the dissolve equation, each flower pixel is 100 percent and each swan pixel is 0 percent. The equation below calculates each pixel:

Result_pixel = Flower_pixel * (alpha/255) + Swan_pixel * [1 - (alpha/255)]

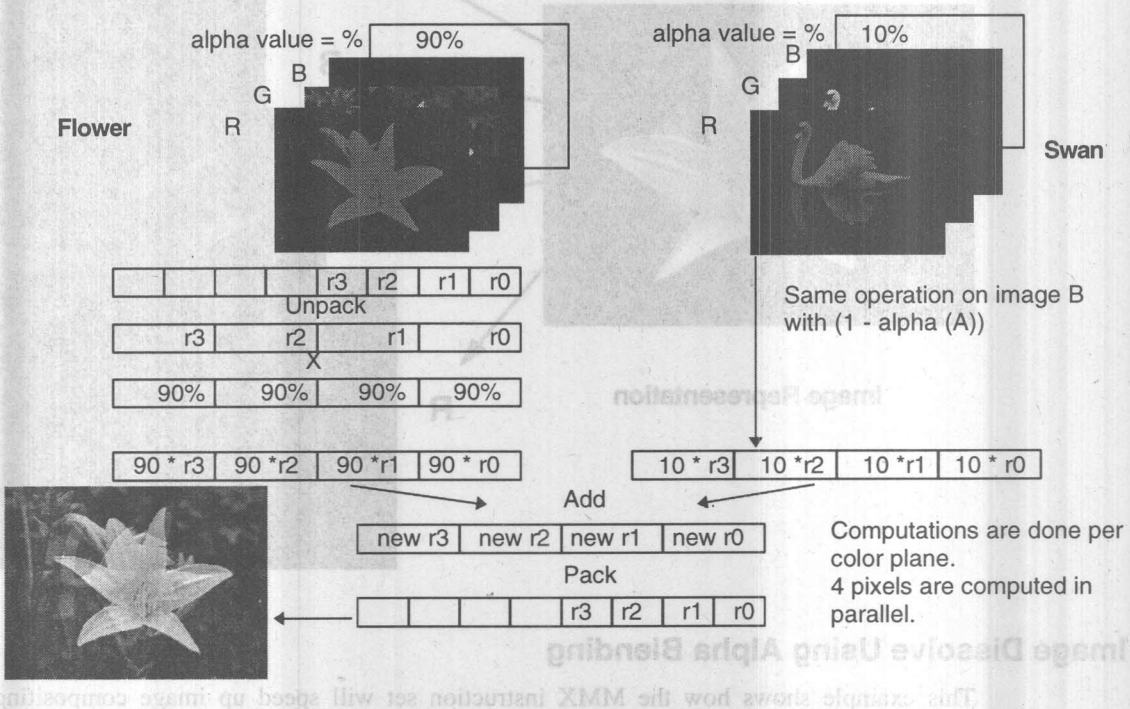
Illustrated below are the flower and swan when alpha = 230:



When the alpha value is 230, the resulting picture is 90 percent flower and 10 percent swan. On close examination, some of the swan image appears in the picture to the right of the equal sign.

This example assumes that the 24-bit color data is organized so that four pixels at a time are processed from one color plane, that is, the image is separated into individual color planes: one for red, one for green, one for blue. The first four red values from the flower and the swan will be processed first. After finishing the red plane, the processing moves to the green and blue planes.

The unpack instruction takes the first four bytes of the red data that are represented in 8-bit values and unpacks each pixel into 16-bit elements, putting them into a 64-bit MMX register. The alpha value, which is computed once per frame, is the other operand. The PMUL multiplies the two vectors in parallel. Similarly, an unpack and PMUL create the intermediate result for the swan. Now the two intermediate results are added together using a PADD and the final result is sent to memory using a PACK that converts the intermediate 16-bit values back to 8-bit pixel values that can be stored.



If these images use 640X480 resolution, and the dissolve technique uses all 255 steps of the alpha value, then 117 million PUNPCKs and PMULs, and 58 million PADDs and PACKs are used. Comparing instruction counts with and without MMX technology for this operation yields the following:

Operation	Calculation without MMX™ Technology	Number of Instructions without MMX Technology	Number of MMX Instructions
Load	(640*480)*255*3*2	470 million	117 million
Unpack	-	-	117 million
Multiply	(640*480)*255*3*2	470 million	117 million
Add	(640*480)*255*3	235 million	58 million
Pack	-	-	58 million
Store	(640*480)*255*3	235 million	58 million
Total		1.4 billion	525 million

Almost 1 billion fewer instructions are used in this example.

The dissolve technique, sometimes called combine, is one of several commonly used image compositing techniques used in multimedia applications and can be sped up substantially with MMX technology.

A XOR B	(B * (1 - alpha(A))) + (A * (1 - alpha(B)))

Alpha blending is a technique used by game developers that is similar to image compositing. Alpha blending allows race cars to drive realistically through fog or smoke, allows a more realistic view of fish in water, or a rabbit in a translucent tube. In these examples, the alpha values wouldn't necessarily be the same for the whole frame, but the basic concept remains the same.

SUMMARY

MMX technology brings more power to multimedia and communication applications. MMX technology adds new data types and instructions that can process data in parallel. MMX technology is fully compatible with existing operating systems and application software.

MMX technology brings a step improvement to the PC platform and enables new applications and usage of PCs. It helps establish a new paradigm in the industry with the PC as an improved communications and multimedia device. Systems enabled with MMX technology will ramp in high volume in 1997 as Intel incorporates the technology in multiple processor generations.

RELATED DOCUMENTATION

Refer to the following documentation for more information on MMX technology.

- *Intel Architecture MMX™ Technology Developers' Manual* (Order Number 243013)
- *Intel Architecture MMX™ Technology Programmer's Reference Manual* (Order Number 243007)

Refer to Intel's corporate website for the latest information on related documentation:

http://www.intel.com/

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Intel Architecture MMX™ Technology in Business Applications

June 1997

Order Number 243367-002

intel

Intel Architecture MMX™ Technology in Business Applications

June 1997

Order Number 243367-002

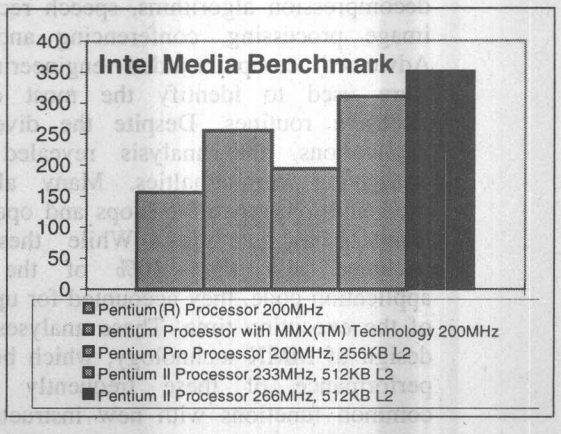
EXECUTIVE SUMMARY

MMX™ technology is Intel's most significant enhancement to the Intel Architecture in the last 10 years, and will enhance the performance of complex media-intensive and communications applications and enable new features and capabilities. MMX technology will have a long-term effect on mainstream business applications, especially as they continue to provide richer content. This trend will continue, and is being accelerated in large part by the mass move to Internet and Intranet technologies, and the inherently rich graphics- and media-intensive nature of these environments.

MMX technology embodies new instructions and data types. These instructions and data types can be used by any type of software, not just multimedia applications. Compression and decompression of files and/or rich content, graphical editing and manipulation, and complex file conversions are examples of common software functionality that will benefit from MMX technology. MMX technology will improve file transfer rates and network performance by enabling faster compression, decompression and smaller file sizes. Intel disclosed details about MMX technology over a year ago. Microsoft, Adobe, and other leading developers have invested significant resources optimizing applications[1] with MMX technology. Existing mainstream business applications are being revised with MMX technology additions and several announcements are expected shortly.

The benefits of MMX technology will continue to become widespread as more applications are designed to take advantage of this technology. MMX technology provides more productive environments, the ability to run more applications at one time, and prevents users from being bandwidth-limited on their systems, saving money in the long run. Software ranging from office applications to Internet/Intranet applications will run faster. For small businesses, MMX technology increases productivity with higher performance systems for in-house development, reducing the need for expensive outsourcing. Across the board, for large corporations and small businesses, purchasing MMX technology-based systems today prepares your user base for the future, extends the lifecycle of PCs by providing the performance headroom for future applications, and reduces long-term capital costs.

By accelerating basic underlying operations (details below), MMX technology can yield a significant performance improvement, as in the 7x improvement[2] experienced by image processing applications. Intel first introduced the Pentium® processor with MMX technology and will continue to incorporate MMX technology into **all** future Intel Architecture microprocessors. The Pentium II processor, targeted at business desktop users, combines the Pentium Pro processor's 32-bit architecture with MMX media enhancement technology and systems are expected in the second quarter of 1997. Overall scores on the Intel Media Benchmark with the 266 MHz Pentium II processor with MMX technology show a 225%[3] increase over the 200 MHz Pentium processor.



Those in a position to specify and purchase systems for use with Internet technology need to look forward as they deploy the next wave of information systems. By mid-1998, **all** Intel microprocessors for PCs will incorporate MMX technology. To provide the most performance headroom for the future, corporations should

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1 Microsoft Internet Explorer*, Netshow*, NetMeeting* and Adobe Photoshop*, PhotoDeluxe* and several other MMX™ technology-optimized examples are discussed ahead.

2 Based on the score improvement for Image Processing in the Intel Media Benchmark. See Appendix A for details.

3 See Appendix A for details and selected individual scores.

evaluate and qualify new MMX technology-based systems.

Although this white paper cannot cover all software vendor efforts underway, it discusses:

- *How* MMX™ technology delivers higher performance
- *Where* this technology applies to business applications, and
- *Examples* of optimized applications available today.

Three appendices detail **tools**, **performance benchmarks** and additional **technical details**.

INTEL MMX™ TECHNOLOGY OVERVIEW

The definition of MMX technology resulted from a focused joint effort between Intel's microprocessor architects and developers from leading software companies. A wide range of software applications were analyzed, including graphics, audio and video, compression and decompression algorithms, speech recognition, image processing, conferencing and others. Advanced computer-aided engineering tools were used to identify the most compute-intensive routines. Despite the diversity of applications, the analysis revealed several underlying commonalties. Many algorithms used multiple repetitive loops and operated on small data quantities. While these loops occupied less than 10% of the overall application code, they accounted for up to 90% of the execution time. These analyses fed the design of MMX technology, which boosts the performance of these frequently executed common functions with new instructions and enhanced hardware execution capabilities.

New MMX technology instructions allow several small data quantities to be concatenated into a single larger quantity, permitting rapid, parallel computations on multiple data quantities at once. For example, graphics information is commonly represented in small, 8-bit, byte-sized quantities. Previously, manipulating 8 bytes of graphics data required 8 repetitions of a single instruction. The same manipulation can now be performed with a single MMX technology instruction, operating on all 8 bytes simultaneously. The result: an 8x improvement in execution time. This speedy, parallel processing of combined data quantities is termed the Single Instruction Multiple Data (SIMD) model, in contrast to the older, less-efficient scheme where a single instruction operated on a single piece of data. To provide maximum flexibility, 57 new 'MMX technology instructions' and 4 new data types were added[4]. These features result in many more calculations performed for each clock cycle of the processor, yielding faster execution times and higher performance[5].

To accelerate the adoption of this advanced technology, the Intel Architecture MMX technology instruction set was designed and implemented in a transparent way that requires no changes to existing operating systems.

NOTE

All existing software continues to run correctly, without modification, on Intel microprocessors that incorporate MMX technology.

MMX™ TECHNOLOGY'S KEY BUSINESS BENEFITS: PERFORMANCE AND APPLICATION VIABILITY

MMX technology brings several tangible benefits to business users. These benefits span the spectrum of increasing overall application, system, and network performance, to expanding and bringing more power to the Internet/Intranet, to making innovative new media-rich and communications applications viable in mainstream business.

MMX™ Technology Benefits Application, System and Network Performance

The powerful parallelism inherent in MMX technology permits highly efficient processing and reduced processor utilization for compute-intensive tasks on large data files (common in image, audio/video data, etc.) without sacrificing system performance. This unleashes processing power for other concurrent or

[4] See Appendix B for more technical details.

[5] See Appendix A for performance benchmark details.

background activities like network operations. For example, while an image is being decompressed with the aid of MMX technology, or downloaded from the web, other applications can execute in parallel without degraded performance. Not only does this increase application and overall system performance, but network performance is enhanced, since the processor now has more time to service network requests while executing multiple host or server (and therefore network-serviced) applications.

Rapid compression and smaller file sizes due to improved compression ratios combine to reduce network traffic even further, benefiting all network users. This also benefits mobile laptop users using modems by reducing file transfer time, connect-time and storage space requirements. Reduced processor utilization by an application lets all users experience faster system and network response times. As a result, users become more productive since they spend less time waiting on compute-intensive tasks. In the future, Accelerated Graphics Port (AGP) technology will further enhance MMX technology-based 3D graphics performance.

MMX™ Technology Makes New Business Applications Viable

MMX technology benefits were never intended to be restricted to a handful of applications. Instead, Intel designers focused on accelerating the basic 'nuts and bolts' functions required by a very wide array of software. This allows MMX technology to improve the performance of a diverse range of applications. Many of these applications are directly tied to new capabilities in business software, especially in Internet/ Intranet applications. Some examples where MMX technology is expected to have the greatest impact are:

- Audio and video-enabled applications in web plug-ins, interactive training, customer self-service, real-time audio and video streaming and videoconferencing
- High-performance image processing, 3D graphics and data visualization, web publishing and content creation
- Intelligent content-based searches of large graphics, audio and video databases
- CAD/CAM model viewing and manipulation
- Security applications, video scene detection, face/fingerprint recognition and watermarking technology

Intranet-based employee training, for example, a natural extension of traditional computer-based training, is enhanced by audio and video components where MMX technology vastly improves the performance of underlying compression, decompression and playback algorithms. The resulting richer training content keeps audiences interested, leading to more effective training and retention.

Standard office suites and presentation software will benefit from MMX technology when integrating high quality graphic images or audio/video components into documents and presentations for greater impact. Industry analysts often point to the proliferation of media-rich business applications, which is precisely where MMX technology will best be applied.

MMX™ TECHNOLOGY IN BUSINESS APPLICATIONS: CATEGORIES AND EXAMPLES

Imaging Application Acceleration with MMX™ Technology

The Intel Media Benchmark[6] shows that MMX technology-optimized imaging applications experience exceptional gains in performance: a 266 MHz Pentium II processor delivers over seven times the performance of a 200 MHz Pentium processor on the imaging component of this benchmark. The exploding use of images in business presentations, sales collateral, product catalogs, brochures, newsletters and publishing requires efficient image management and manipulation tools. Existing tools can efficiently search, sort and operate on alphanumeric data, but graphic images can only be treated as binary large objects. As such,

[6] See Appendix A for details and selected individual scores.

print drivers require a great deal of data manipulation which can be accelerated by MMX technology. Image manipulation functions like filtering, compositing, alpha-blending, chroma-keying, anti-aliasing and color space conversion algorithms are compute-hungry functions suited for coding with MMX technology instructions. Popular applications like Adobe Premiere*, Photoshop*, PhotoDeluxe*, and AfterEffects* applications are all optimized for MMX technology. Adobe's PhotoDeluxe delivers performance gains of up to 200% when working with large images and adding special effects to photographs[7]. Microsoft's Picture It!* incorporates MMX technology to allow high quality photo imaging on desktop systems.

By improving the performance and reducing the execution time for complex filters, MMX technology reduces the number of iterations and thus, the amount of time spent achieving a desired result. For example, a 50-second reduction in manipulating an image seems trivial by itself, but quickly becomes significant for typical users who may make such manipulations numerous times. The acceleration provided by MMX technology allows trial-and-error by novice users, making advanced capabilities possible for non-specialists and small businesses. For experts, this performance allows the creative process to not be interrupted, allows the flow of ideas to continue, and hastens and improves the end-results.

How MMX™ Technology Benefits Compression and Decompression

Media-intensive data is typically quite large and requires compression for practical storage and network or web transmission. Compression and decompression algorithms are broadly used in underlying algorithms with MMX technology enables a performance increase of up to 3x for JPEG compression and up to 5x for JPEG decompression[8]. These optimizations are being widely proliferated into various business applications currently in development. Pegasus' PICTOOLs* toolkits use MMX technology for faster image compression and decompression and see up to a 2x to 3x performance improvement over non-optimized versions.

Video, Communications and Conferencing Applications

MMX technology addresses some of the barriers to real-time video streaming over the Internet and corporate Intranets. Real-time streaming media permits viewing and/or listening while files download from the web, instead of waiting for complete file transfers. For example, Microsoft's NetShow* 2.0 is an easy, powerful application for streaming multimedia across the Internet and Intranet. Netshow 2.0 supports a wide variety of industry standard codecs which demonstrate significant gains with the use of MMX technology.

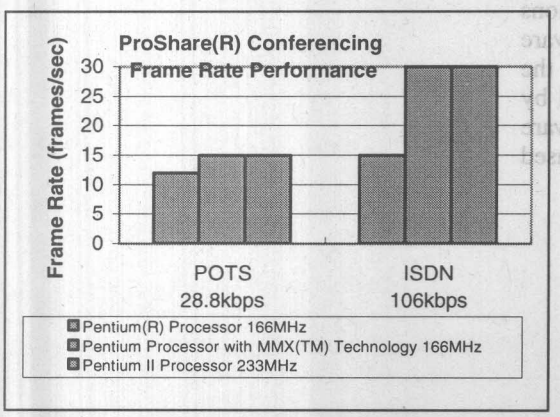
Effective, practical video communications require high quality image transmission and frame rates which can be difficult to achieve over low bandwidth communication infrastructures. MMX technology enhances software-only compression optimized for delivering high-quality video over existing networks and corporate LANs. High compression ratios further reduce the burden on limited network bandwidth. Businesses that deliver video to the desktop extend the

[7] Adobe Press Release, 1/27/97.

[8] Intel Architecture Laboratory measurements of the effects of MMX™ technology optimizations on underlying algorithms on a 200 MHz Pentium processor with MMX technology.

training, web-based computer help desks, and Internet communications. Video-enabled Intranet-based training with MMX technology eliminates the high production and distribution costs of hundreds of hours of videotape-based content to offices worldwide. This scheme permits central content management and ensures employees access only the most up-to-date information, and eliminates the need for experts to travel internationally to deliver live training at each site.

Videoconferencing naturally benefits from MMX technology's ability to accelerate communication, compression, and decompression of audio and video data streams. MMX technology enables professional quality videoconferencing by *doubling* frame rates previously achievable. The graph below illustrates the impact of MMX technology on Intel ProShare® conferencing frame rates for QCIF[9] image sizes over Plain Old Telephone Service (POTS) vs. ISDN.



The improved frame rate due to MMX technology shown in the graph above is achieved concurrent with a reduction in processor utilization, increasing the available processor bandwidth for use by other applications or network activity.

Microsoft's collaboration and videoconferencing NetMeeting* software uses specialized codecs with MMX technology to provide enhanced performance for audio/video compression and decompression. These result in lower processor utilization and improved audio/video quality during a call.

[9] Quarter Common Interchange Format (QCIF) image size.

Web Browsers and MMX™ Technology

The Gartner[10] Group estimates that 80% of 'knowledge workers' will access the Internet from within PC applications *daily* to do their jobs in the next couple of years. The user's interface to the web via browsers and new plug-ins for viewing graphics and video/audio playback can be significantly improved with MMX technology. Static HTML web sites have already given way to dynamic multimedia interfaces that directly benefit from MMX technology. Microsoft will take advantage of MMX technology using Dynamic HTML's multimedia effects, which will be delivered in Microsoft Internet Explorer* 4.0. MMX technology-enhanced Direct3D* will also be included as an ActiveX* control in Internet Explorer to view 3D Internet content. The binary-to-ASCII text conversion in email and browser-based web interactions via *uuencoding* and *uudecoding* are basic functions which occur very frequently during normal web usage that are greatly sped up by MMX technology. Netscape is expected to include discussion and conferencing clients with audio streaming via plug-ins or Java applets. The Netscape Live3D* plug-in for Navigator* takes full advantage of Intel's MMX technology, giving users the ability to view more complex objects through increased texture and alpha blending, with increased performance.

Accelerating Database Applications with MMX™ Technology

Managing large databases of mixed media assets can be slow or inefficient with traditional databases because searches on complex data are based on textual file descriptions. MMX technology can improve the performance of hybrid object relational databases, which store more types of media data and perform faster complex queries. The Informix content management platform manages both complex and simple data types. Informix Universal Server and Illustra* Server* allow non-traditional data to be stored and manipulated by special MMX technology-optimized database modules called DataBlades*. These modules deliver efficient management of text, image, 2D/3D spatial,

[10] Gartner Group, Symposium/ITxpo 96.

2D/3D spatial, HTML, time-series, audio, video and other complex data types. 'Snap-in' DataBlades extend the core database server and client capabilities, permitting dynamic content management via custom indexing, pattern matching on complex data types, graphics, images, video, etc.

CONCLUSION

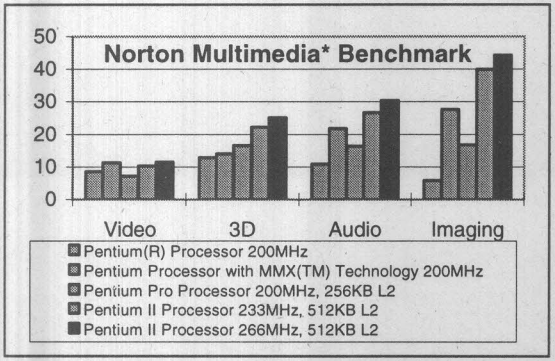
MMX technology will have a long-term beneficial effect on mainstream business applications and increases system, application and network performance while making innovative new applications viable for wide-scale deployment.

The mass move to Internet/Intranet technologies with rich content will continue, perhaps affecting the workplace as profoundly as word processing and desktop publishing. MMX technology will help remove the complexity and cost associated with sophisticated applications by reducing the need for custom hardware solutions. The industry acknowledges the benefits of MMX technology, demonstrated by the appearance of new and optimized software applications, tools and MMX technology-based systems.

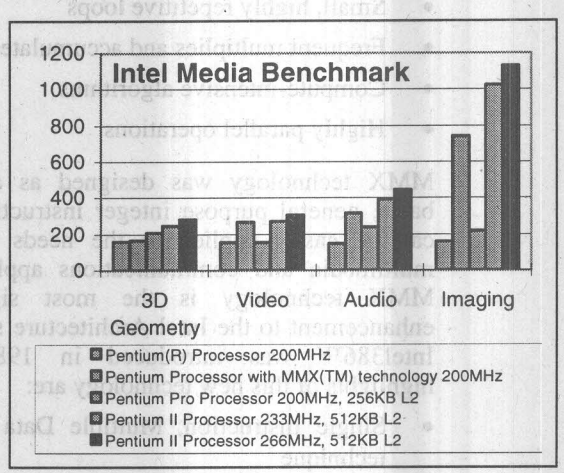
The Pentium II processor extends the performance of the Pentium Pro processor and adds the capabilities of MMX technology. Pentium II processor-based systems will arrive in the second quarter of 1997 as the high-performance business systems of choice. Intel will promote the continued success of MMX technology by continuing to provide extensive developer support, and by incorporating MMX technology in all future microprocessor offerings. Collectively, these activities will proliferate higher quality applications and platforms to business users worldwide, enabling enhanced communications and higher productivity for employees who take advantage of MMX technology. By mid-1998, **all** Intel Architecture microprocessors will incorporate MMX technology. To take maximum advantage of this direction, and to prepare the installed base and provide the most headroom for high-performance applications, ensure that new systems contain microprocessors with Intel MMX technology.

performance acceleration via routines optimized for MMX technology will only be apparent on platforms with microprocessors that incorporate MMX technology. MMX technology-optimized software performs 'processorID' checks to verify Intel Architecture MMX technology instruction set support by the underlying microprocessor, allowing the execution of higher performance optimized routines. Otherwise, older, non-optimized routines must be executed. **Users cannot realize the performance benefits of MMX technology from software upgrades alone:** the client PC **must** be MMX technology-enabled to take advantage of the optimizations. The following benchmarks help quantify the benefits of executing MMX technology-optimized software on PCs with Intel MMX technology microprocessors.

The Norton Multimedia* Benchmark[11] compares a system's multimedia capabilities against the basic Multimedia PC (MPC) Level 2 specification.



Windows* 95.



[11] See Appendix D for selected individual component scores and system configurations.

[12] See Appendix D for selected individual component scores and system configurations.

APPENDIX B: ADDITIONAL MMX™ TECHNOLOGY DETAILS

As mentioned in the 'Intel Architecture MMX Technology Overview' above, a wide array of applications were analyzed to determine how new instructions could enhance the performance of the most basic, compute intensive functions. The key attributes of these applications were:

- Small integer data types (for example: 8-bit graphics pixels, 16-bit audio samples)
- Small, highly repetitive loops
- Frequent multiplies and accumulates
- Compute-intensive algorithms
- Highly parallel operations

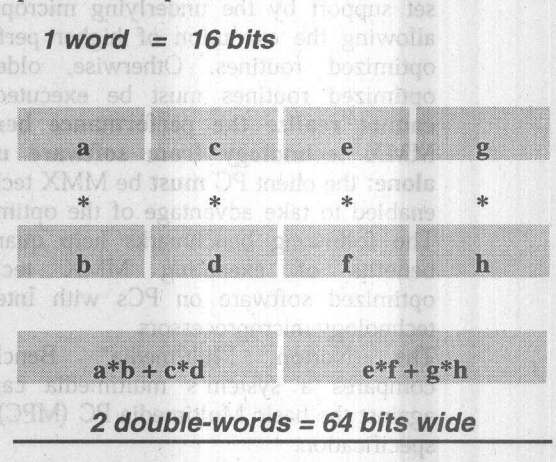
MMX technology was designed as a set of basic, general purpose integer instructions that can be easily applied to the needs of most multimedia and communications applications. MMX technology is the most significant enhancement to the Intel Architecture since the Intel386™ was introduced in 1985. The highlights of this new technology are:

- Single Instruction, Multiple Data (SIMD) technique
- Fifty-seven new instructions
- Eight 64-bit wide MMX registers overlayed on existing registers
- Four new data types

SIMD Techniques

The Single Instruction Multiple Data (SIMD) technique vastly speeds up software performance by using a single instruction to process multiple data elements in parallel. This parallelism greatly increases performance. The MMX technology supports parallel operations on byte (8-bit), word (16-bit), and double-word (32-bit) data elements, and also the new quad-word (64-bit) integer data type. SIMD is analogous to using a central power switch to turn on 64 lights in an office complex instead of turning on each bank of 8 lights one by one.

For example, the `pmaddwd` instruction allows a 'packed multiply and `add` of 4 words into 2 double-words' as visually represented below. Four multiplications and 2 summations are performed in parallel with one instruction:



APPENDIX C: TOOLS FOR BUILDING AND TESTING NEW MMX™ TECHNOLOGY APPLICATIONS

Since March 1996, when Intel publicly released the details of MMX technology, ISVs have participated in Intel Developer Support Programs, implemented coding enhancements, and used examples, libraries and software performance analysis tools provided by Intel. As a result, tool vendors are prepared with optimized offerings now.

Compiler and debugger support for MMX technology are available in: Microsoft's Visual C++*, Powersoft's Watcom C++ and NuMega Technologies' SoftICE*. Microsoft also takes advantage of MMX technology in the Direct3D addition to the DirectX* family of interactive media APIs. Direct3D, currently shipping with Windows 95 and planned to ship with Windows NT, offers a highly optimized software-only rendering engine with transparent, high-performance, device-independent services. Superscape's implementation of Direct3D with it's own rendering technology offers new features to application and content developers using Superscape real time 3D authoring tools. Use of the new features (smooth shading, lighting, Z-buffering and transparency) are all greatly accelerated by MMX technology up to 8x over Pentium processor systems without MMX technology.

MMX technology-enhanced authoring tools are available from Macromedia, Inc. Director*, provides timing and interactivity for media elements such as 2D and 3D graphics, animation, sound, and digital video from a wide variety of sources and can create stand-alone runtime applications. Macromedia expects animation and multimedia playback performance to increase by up to 50% and MMX technology provides a speed-up of up to 40% in 256 color mode using ink bitmap images and animations.

The Intel Signal Processing Library with MMX technology code allows signal processing functions previously requiring DSPs (Digital Signal Processors) to be performed natively on a host Intel Architecture processor with MMX technology. The Intel Recognition Primitive Library provides developers of speech and character-recognition software a set of generic MMX technology-enhanced functions. Intel's web site shows several coding examples of common data manipulation functions accelerated by MMX technology. VTune*, a unique visual performance analysis and software tuning tool for the Intel Architecture locates trouble spots, and offers advice and suggestions on how to maximize code performance using MMX technology.

ADDITIONAL INFORMATION

For more information on MMX technology, please consult the following sources, or your system or software vendor.

- World Wide Web:
  http://www.intel.com
  http://mmx.com
  http://developer.intel.com/drg/mmx
- Intel Literature Center: 1-800-879-4683
- Intel Customer Support: 1-800-628-8686

Benchmarks	200 MHz	200 MHz	256 KB L2	512 KB L2	512 KB L2
Intel Media Benchmark/ Windows* 95	**156.00**	**255.43**	**194.38**	**310.40**	**350.77**
Video	155.52	268.70	158.34	271.98	307.24
Image Processing	159.03	743.92	220.75	1026.55	1129.01
3D Geometry	161.52	166.44	209.24	247.68	281.61
Audio	149.80	318.90	240.82	395.79	446.72
Norton Media Benchmark	**9.6**	**13.8**	**11.6**	**17.2**	**19.4**
Video	8.5	11.4	7.2	10.4	11.6
3D Graphics	12.8	14.0	16.6	22.2	25.2
Audio	10.9	21.9	16.4	26.7	30.4
CD-ROM	4.1	4.1	4.1	4.1	4.1
Imaging	5.8	27.7	16.8	40.0	44.3

	MMX Technology – 32 kB (16 kB I + 16 kB D)		
Secondary Cache	512 kB WB Burst	256 kB WB Burst	512 kB WB Burst
Memory Size/Speed	Windows* 95 – 32 MB SDRAM		
Hard Disk Controller/Bus	Adaptec 2940UW* SCSI/PCI		
Hard Disk	Seagate ST32550W		
Video Controller/Bus	Matrox Millennium*/PCI		
Video Memory Size/Type	2 MB WRAM		
Operating System	Windows 95		
Video Driver Revision	Matrox 3.22 with Microsoft DirectX* 3.0a		
Graphics	1024x768 Resolution, 16-bit color		
CD-ROM Drive	Pioneer SCSI DR-433		
Sound Card	Creative Labs Sound Blaster* 16		

Intel Architecture Optimization Manual

Order Number 242816-003

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in other geographies, please contact your local sales office

1

Introduction to the Intel Architecture Optimization Manual

1

Introduction to the Intel Architecture Optimization Manual

CHAPTER 1
INTRODUCTION TO THE INTEL ARCHITECTURE OPTIMIZATION MANUAL

In general, developing fast applications for Intel Architecture (IA) processors is not difficult. An understanding of the architecture and good development practices make the difference between a fast application and one that runs significantly slower than its full potential. Of course, applications developed for the 8086/8088, 80286, Intel386™ (DX or SX), and Intel486™ processors will execute on the Pentium®, Pentium Pro and Pentium II processors without any modification or recompilation. However, the following code optimization techniques and architectural information will help you tune your application to its greatest potential.

1.1 TUNING YOUR APPLICATION

Tuning an application to execute fast across the Intel Architecture (IA) is relatively simple when the programmer has the appropriate tools. To begin the tuning process, you need the following:

- Knowledge of the Intel Architecture. See Chapter 2.
- Knowledge of critical stall situations that may impact the performance of your application. See Chapters 3, 4 and 5.
- Knowledge of how good your compiler is at optimization and an understanding of how to help the compiler produce good code.
- Knowledge of the performance bottlenecks within your application. Use the VTune performance monitoring tool described in this document.
- Ability to monitor the performance of the application. Use VTune.

VTune, Intel's Visual Tuning Environment Release 2.0 is a useful tool to help you understand your application and where to begin tuning. The Pentium and Pentium Pro processors provide the ability to monitor your code with performance event counters. These performance event counters can be accessed using VTune. Within each section of this document the appropriate performance counter for measurement will be noted with additional tuning information. Additional information on the performance counter events and programming the counters can be found in Chapter 7. Section 1.4 contains order information for VTune.

1.2 ABOUT THIS MANUAL

It is assumed that the reader is familiar with the Intel Architecture software model and assembly language programming.

This manual describes the software programming optimizations and considerations for IA processors with and without MMX technology. Additionally, this document describes the implementation differences of the processor members and the optimization strategy that gives the best performance for all members of the family.

This manual is organized into seven chapters, including this chapter (Chapter 1), and four appendices.

Chapter 1 — Introduction to the Intel Architecture Optimization Manual

Chapter 2 — Overview of Processor Architecture and Pipelines: This chapter provides an overview of IA processor architectures and an overview of IA MMX technology.

Chapter 3 — Optimization Techniques for Integer Blended Code: This chapter lists the integer optimization rules and provides explanations of the optimization techniques for developing fast integer applications.

Chapter 4 — Guidelines for Developing MMX™ Technology Code: This chapter lists the MMX technology optimization rules, with an explanation of the optimization techniques and coding examples specific to MMX technology.

Chapter 5 — Optimization Techniques for Floating-Point Applications: This chapter contains a list of rules, optimization techniques, and code examples specific to floating-point code.

Chapter 6 — Suggestions for Choosing a Compiler: This section includes an overview of the architectural differences and a recommendation for blended code.

Chapter 7 — Intel Architecture Performance Monitoring Extensions: This chapter details the performance monitoring counters and their functions.

Appendix A — Integer Pairing Tables: This appendix lists the IA integer instructions with pairing information for the Pentium processor.

Appendix B — Floating-Point Pairing Tables: This appendix lists the IA floating-point instructions with pairing information for the Pentium processor.

Appendix C — Instruction to Micro-op Breakdown

Appendix D — Pentium® Pro Processor Instruction to Decoder Specification: This appendix summarizes the IA macro instructions with Pentium Pro processor decoding information to enable scheduling for the decoder.

1.3 RELATED DOCUMENTATION

Refer to the following documentation for more information on the Intel Architecture and specific techniques referred to in this manual:

- *Intel Architecture MMX™ Technology Programmer's Reference Manual,* Order Number 243007.
- *Pentium® Processor Family Developer's Manual*, Volumes 1, 2 and 3, Order Numbers 241428, 241429 and 241430.
- *Pentium® Pro Processor Family Developer's Manual*, Volumes 1, 2 and 3, Order Numbers 242690, 242691 *and* 242692.

1.4 VTune ORDER INFORMATION

Refer to the VTune home page on the World Wide Web for current order information:

http://www.intel.com/ial/vtune

To place an order in the USA and Canada call 1-800-253-3696 or call Programmer's Paradise at 1-800-445-7899.

International Orders can be placed by calling 503-264-2203.

intel®

AP-578

APPLICATION NOTE

Software and Hardware Considerations for FPU Exception Handlers for Intel Architecture Processors

February 1997

Order Number: 243291-002

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APPLICATION
NOTE

Software and Hardware Considerations for FPU Exception Handlers for Intel Architecture Processors

February 1997

Order Number: 243329-002

1.0 INTRODUCTION AND READING GUIDE

The primary purpose of this application note is to provide information to help software engineers write the most robust Floating-Point Unit (FPU) exception handlers possible. This note also provides the basic hardware information needed to design the MS-DOS* compatible interface[1] for the most recent generations of Intel Architecture processors, starting with the Intel486™ processor. (Because of the small amount of new design activity, the hardware interfaces for the 8086 through the Intel386™ processors are treated only briefly.) The third purpose is to provide a compendium of the history of the development and variations of the Intel Architecture Floating-Point Units (FPUs) as relevant to their exception handling. Following is a list of Intel Architecture processors and math coprocessors in chronological order.

- 8086 processor
- 8087 math coprocessor
- 80286 processor
- 80287 math coprocessor
- Intel386™ processor
- Intel387 math coprocessor
- Intel486™ DX processor (with integrated FPU)
- Intel486 SX processor
- Intel487 math coprocessor
- Pentium® processor (with integrated FPU)
- Pentium Pro processor (with integrated FPU)

Much of this material is in various sections of the *Pentium® Processor Family Developer's Manual,* Volume 3. There is also some material in this application note that is not published elsewhere. On the other hand, there is much additional material on the FPU from the *Pentium® Processor Family Developer's Manual,* Volume 3 which has not been reproduced here, including the details on each of its specific exceptions. Much of this will be useful in writing FPU exception handlers, so Volume 3 should be used as an essential reference along with this appliction note.

NOTE

The following manuals referenced in this document are archived and are available on Intel's web site at http://www.intel.com: *Pentium® Processor Family Developer's Manual, Volume 1: Pentium Processor* (Order Number 241428-004) and the *Pentium® Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual* (Order Number 241430-004).

The materials are presented in a mostly chronological order, which supports the history preservation purpose, and also minimizes forward references. Thus the main body of this application note begins with Section 2 which covers the six presently available generations of Intel Architecture FPUs in chronological order starting with the 8087. The history of the FPU exception handling has been complicated both by Intel's successful efforts to improve the performance and flexibility of the FPU through the generations, and by the decision to support upward compatibility for a large customer base which was implementing FPU exception handling in a way compatible with the first 8088 Personal Computers (PCs) and major Operating Systems (OSs). This second complication has resulted in two different systems or modes for FPU exception handling starting with the 80286 and 80287.

Beginning with the 80286 and 80287, Intel provided a dedicated input pin (ERROR#) on the 80286, to be connected to the ERROR# output pin on the 80287, for the FPU exceptions. When asserted, the ERROR# input triggers interrupt 16. The use of this dedicated interrupt for the FPU exception handler is referred to as the "native mode", and is recommended by Intel. However, for reasons explained in Sections 2.1 and 2.2, the majority of the Intel Architecture (IA) customer base has not been using the native mode, but rather the "MS-DOS compatible mode" for FPU exception handling. Since the MS-DOS compatible mode has the largest customer base, is the more complicated mode, and has changed the most between generations, it is the main focus of Section 2. In addition to the history of the architecture and interfaces for FPU exception

Footnotes

[1] WINDOWS* 95 and WINDOWS 3.1 (and earlier versions) use almost the same interface as MS-DOS*, and the recommendations herein for an MS-DOS compatable system apply to all three operating systems.

handling, Section 2 provides the basic hardware information needed to design the MS-DOS compatible interface for the most recent generations of IA processors, and discusses in detail several important system implications.

Section 3 describes the recommended protocol for writing MS-DOS compatible FPU exception handlers, with various options, along with discussions of several problems and how to avoid them. Most of the material is also applicable to native mode handlers.

Although the native mode of FPU exception handling was available from the second generation of the six presently available generations of the Intel Architecture FPUs (and brief discussions of it are provided in Section 2), we give the main presentation of it last, in Section 4. This is more chronologically consistent than it would seem because it has not become widely used until recently.

A software engineer who needs to write an MS-DOS compatible FPU exception handler but does not want to review the FPU history (or read any more about hardware than necessary) may skip Section 2 and begin reading Section 3. Then some subsections of Section 2 should be read as needed when referenced in Section 3. Someone writing a native mode exception handler that wants to read only what's necessary should start with Section 4, but then should also read Section 3, as most of the recommended protocol for FPU exception handling is the same for MS-DOS compatible and native modes and is not repeated in Section 4. Studying Section 4 first will allow this reader more easily to skip references back into Section 2 which are not relevant to the native mode.

A note on TERMINOLOGY: There are many variations of the words which are used to label an (unmasked) FPU error condition, and also the code which handles it. "Error", "exception" and "fault" are used to refer to the condition. Such a condition results in an interrupt, if no mask or block is in effect along the interrupt pathway. The code which handles the interrupt can be referred to as an error or exception or fault handler, or an interrupt or exception service routine, etc. The phrase "**exception handler**" has been used consistently (as much as possible) in this application note, for several reasons: "Exception" is less general than interrupt (which includes external hardware interrupts and software interrupts, as well as the processor problem conditions called exceptions or faults), but correctly **more** general than error or fault (because e.g. a precision exception caused by the fact that the number 1/3 cannot be exactly represented in the 80 bit FPU format is not really due to any mistake or error!). However, the reader should be aware that a number of the variations given above can be found in the literature, and that when applied to the FPU, they all mean the same thing.

2.0 MS-DOS* COMPATIBLE HANDLERS AND THEIR ISSUES OVER GENERATIONS

2.1 Origin of MS-DOS* Mode: 8088 and 8087

The 8087 has an output pin, INT, which it asserts when an unmasked exception occurs. There is no dedicated pin or interrupt vector number in the 8088 or 8086 specific for an FPU error assertion. Intel recommended that the FPU INT be routed to the 8088 or 8086 INTR pin through an 8259A Programmable Interrupt Controller (PIC), and not to the NMI input. However, the original PC design attached INT to NMI anyway, because by the time the 8087 was available, the original PC had already assigned other functions to the 8 inputs of the single PIC used in that design.

2.2 Development of MS-DOS* Mode with 80286 and 80287; Intel386™ Processor and Intel387 Math Coprocessor

The 80286 and 80287 and Intel386 processor and Intel387 math coprocessor pairs are each provided with ERROR# pins that are recommended to be connected between the processor and FPU. If this is done, when an unmasked FPU exception occurs, the FPU records the exception, and asserts its ERROR# pin. The processor recognizes this active condition of the ERROR# status line at the next WAIT or ESC instruction in its instruction stream, and branches to the FPU exception handler at interrupt vector 16. This is the native mode.

However, it was important to maintain maximum compatibility with the already significant 8088 and 8086 PC software base, where the NMI vector (#2) was used for FPU exceptions and vector 16 was used for the BIOS video software interrupt. So the

original IBM PC-AT* design for the 80286 and 80287 maintained Vector #16 for the BIOS video, and vector 2 was shared between the FPU exception and the new parity checking feature. A parity error detected by external hardware directly triggered vector 2 through the NMI pin. The FPU exception was handled by tying the 80286 RROR# input permanently high, and the 80287 ERROR# output was tied to the IRQ13 interrupt input on the second (cascaded) PIC in the PC-AT design. The PIC was programmed to issue vector 75H when IRQ13 was triggered.[2] But to maintain compatibility with older PC software that expected to access its own FPU exception handler by changing vector 2, the BIOS routine activated by INT 75H branches to INT 2. The standard INT 2 routine tests to see if the signal is due to the NMI pin (in which case it branches to the Parity Error handler) or an FPU exception.

2.2.1 SPECIAL HARDWARE FOR THE 80287 INTERFACE

It is necessary to guarantee, in the case of an 80287 exception, that the exception will be handled through the external loop using IRQ13 in the cascaded PIC before other 80287 instructions are sent over from the 80286. This is done by asserting BUSY# to the 80286, which normally means that the 80287 is still busy with a previous instruction, and so blocks the 80286 from sending another until BUSY# is de-asserted. This additional use of BUSY# is implemented by an edge triggered flip-flop which latches BUSY# using ERROR# from the 80287 as a clock. The output of this latch is OR'ed with the BUSY# output of the 80287 and drives the BUSY# input of the 80286. This PC-AT scheme effectively delays

deactivation of BUSY# at the 80286 whenever an 80287 ERROR# is signaled.

Since the BUSY# signal to the 80286 remains active after an exception, the IRQ13 interrupt (exception) handler (accessed through interrupt vector 75H) is guaranteed to execute before any other 80287 instruction can begin (except for some special control instructions).The IRQ13 handler clears the BUSY# latch (by writing to a special I/O port defined at 0F0H), thus allowing execution of 80287 instructions to proceed. The handler then branches to the NMI handler (interrupt vector 2), where the user defined numeric exception handler resides in PC compatible systems. Thus the PC-AT scheme approximates the exception reporting scheme between the 8087 and 8088 in the original PC.

2.2.2 SPECIAL HARDWARE FOR THE INTEL387™ MATH COPROCESSOR INTERFACE

The Intel386 processor can use a PC-AT compatible interface to communicate with an Intel387 math coprocessor, that is similar to the one in the 80286 and 80287 system above. As with the 80286, the Intel386 processor ERROR# pin should be tied permanently inactive (high), and the Intel387 ERROR# output used both to drive IRQ13, and to latch BUSY# in a flip-flop. The IRQ13 handler (vector 75H) should clear the BUSY# latch and branch to the NMI handler, as in the 80286 case.

However, an additional hardware feature is needed to manage the PEREQ signal to the Intel386 processor. After the Intel387 math coprocessor asserts ERROR#, and then its BUSY# signal has gone inactive, external hardware must re-assert the PEREQ signal to the Intel386 processor. This is needed for store instructions (for example, FST *mem*) because the Intel387 math coprocessor drops PEREQ once it

Footnotes

[2] WINDOWS 95 and WINDOWS 3.1 (and earlier versions) use interrupt 5DH instead of 75H, but the recommendations herein apply to systems using these WINDOWS operating systems, as well as MS-DOS.

signals an exception. While the Intel386 processor has not yet recognized the occurrence of the exception, it still expects the data transfers to complete via PEREQ re-activation. It is permissible for the Intel386 processor to receive undefined data during such I/O read cycles. Disabling the Intel387 math coprocessor is not necessary, because the dummy data transfer cycles directed to the Intel387 math co processor when PEREQ is externally reactivated for the Intel386 processor will not disturb the operation of the Intel387math coprocessor. The IRQ13 interrupt handler should remove the extension of BUSY# and also the re-activation of PEREQ via a write to PC/AT compatible hardware at I/O port 0F0H.

An Intel387 math coprocessoroffers significant performance improvements over the 80287, but because the Intel386 processor was ready for production before the Intel387math coprocessor, the Intel386 processor was designed to work with either the 80287 or Intel387 math coprcoessors. The Intel386 processor automatically configures itself for the attached FPU on reset by testing the ERROR# pin, and setting or clearing bit 4 in CR0 (see Section 10.1.3 in the *Pentium® Processor Family Developer's Manual,* Volume 3). This bit is the ET (Extension Type) bit, and it will be set if ERROR# is low (meaning an Intel387 is attached) and cleared if ERROR# is high (meaning there is an 80287 or no FPU attached). The MS-DOS compatible hardware interface is similar to that for the Intel386 processor and Intel387 math coprocessor combination.

2.3 FERR# & IGNNE# with Intel486™ and Pentium® Processors with CR0.NE=0

In the Intel486 and Pentium® processors, more enhancements and speedup features have been added to the corresponding FPUs. Also, the FPU is built into the same chip as the processor, which allows further increases in speed. MS-DOS compatibility for exception handling has also been built in, with the NE bit in control register CR0 selecting the MS-DOS compatible mode if made zero. (NE=1 selects the native or internal mode, which generates Interrupt 16, which is the same as the native version of exception handling for the 80286 and 80287 and the Intel386 processors and Intel 387 math coprocessor.)

In MS-DOS compatible mode, the FERR# (Floating-point ERRor) output replaces the ERROR# signal from the previous generations, and is connected to a PIC. A new input signal, IGNNE# (**IGN**ore **N**umeric **E**rror), is provided to allow the FPU exception handler to execute FPU instructions, if desired, without first clearing the error condition and without triggering the interrupt a second time. This IGNNE# feature is needed to replicate the capability that was provided on MS-DOS compatible Intel 80286 and 80287 and the Intel386 processors and INtel 387 math coprocessor-based systems by turning off the BUSY# signal, when inside the FPU exception handler, before clearing the error condition.

Note that Intel, in order to provide Intel486 processors for market segments which had no need for an FPU, created the "SX" versions. These Intel486 SX processors did not contain the floating-point unit. Intel also produced Intel487 SX math coprocessors for end users who later decided to upgrade to a system with an FPU. These Intel487 SX math coprocessors are similar to standard Intel486 processors with a working FPU on board. Thus the external circuitry necessary to support the MS-DOS compatible mode for Intel487 SX math coprocessors is the same as for standard Intel486 DX processors.

Note that the special DP (Dual Processing) mode for Pentium processors, and also the more general Intel MultiProcessor Specification for systems with multiple Pentium or Pentium Pro processors, support FPU exception handling only in the native mode. Intel does not recommend using the MS-DOS compatible FPU mode for systems using more than one processor.

2.3.1 BASIC RULES: WHEN FERR# IS GENERATED

- Assume the following conditions: NE=0, the IGNNE# input is de-asserted, and then an FPU instruction causes an unmasked FPU exception. Then in most cases, deferred error reporting occurs. This means that the processor does not respond immediately, but rather freezes just before executing the *next* WAIT or FPU instruction (except for "No-Wait" instructions, which the FPU executes regardless of an error condition).
- At the same time that the processor freezes, it also asserts the FERR# output.
- The frozen processor waits for an external interrupt, which must be supplied by external

hardware in response to the FERR# assertion.

- In MS-DOS compatible systems, FERR# is fed to the IRQ13 input in the cascaded PIC, which generates interrupt 75H, which then branches to interrupt 2, as described above for the 80286and 80287 and Intel386 processor and Intel387 processor-based systems.

These cases in which FERR# is not asserted at the time of the error, but rather at the next FPU or WAIT instruction, include all exceptions caused by the basic arithmetic instructions (including FADD, FSUB, FMUL, FDIV, FSQRT, FCOM and FUCOM), precision exceptions caused by all types of FPU instructions, and numeric underflow and overflow on all types of FPU instructions except stores to memory. We will refer to these cases as deferred (error reporting).

On the other hand, there are some exceptions, which when caused by some instructions, drive FERR# at the time that the exception occurs. These include FPU stack fault, invalid operation and denormal exceptions caused by all transcendental instructions, FSCALE, FXTRACT, FPREM and others, and all exceptions (except precision) when caused by FPU store instructions. These cases are called immediate (error reporting). (These cases will, like the deferred, cause the processor to freeze just before executing the next WAIT or FPU instruction if the error condition has not been cleared by that time.) Note that in general, whether an FPU exception case is deferred or immediate depends both on which exception occurred, and which instruction caused that exception. A complete specification of these cases, which applies also to the Intel486, is given in Section 5.1.21 in the *Pentium® Processor Family Developer's Manual,* Volume 1.

If NE=0 but the IGNNE# input is active while an unmasked FPU exception is in effect, the processor disregards the exception, does not assert FERR#, and continues. If IGNNE# is then de-asserted and the FPU exception has not been cleared, the processor will respond as described

above. (That is, an immediate exception case will assert FERR# immediately. A deferred exception case will assert FERR# and freeze just before the next FPU or WAIT instruction.) The assertion of IGNNE# is intended for use only inside the FPU exception handler, where it is needed if one wants to execute non-control FPU instructions for diagnosis, before clearing the exception condition. When IGNNE# is asserted inside the exception

handler, a preceding FPU exception has already caused FERR# to be asserted, and the external interrupt hardware has responded, but IGNNE# assertion still prevents the freeze at FPU instructions. Note that if IGNNE# is left active outside of the FPU exception handler, additional FPU instructions may be executed after a given instruction has caused an FPU exception. In this case, if the FPU exception handler ever did get invoked, it could not determine which instruction caused the exception.

To properly manage the interface between the processor's FERR# output, its IGNNE# input, and the IRQ13 input of the PIC, additional external hardware is needed. A recommended configuration is described below.

2.3.2 RECOMMENDED EXTERNAL HARDWARE TO SUPPORT MS-DOS* COMPATIBILITY

Figure 1 below provides an external circuit which will assure proper handling of FERR# and IGNNE# when an FPU exception occurs. In particular, it assures that IGNNE# will be active only inside the FPU exception handler without depending on the order of actions by the exception handler. Some hardware implementations have been less robust because they have depended on the exception handler to clear the FPU exception interrupt request to the PIC (FP_IRQ signal) *before* the handler causes FERR# to be de-asserted by clearing the exception from the FPU itself. Figure 2 below shows the details of how IGNNE# will behave when the circuit in Figure 1 is implemented. The temporal regions within the FPU exception handler activity are described as follows:

1. The FERR# signal is activated by an FPU exception and sends an interrupt request through the PIC to the processor's INTR pin.
2. During the FPU interrupt service routine (exception handler) the processor will need to clear the interrupt request latch (Flip Flop #1). It may also want to execute non-control FPU instructions before the exception is cleared from the FPU. For this purpose the IGNNE# must be driven low. Typically in the PC environment an I/O access to Port 0F0H

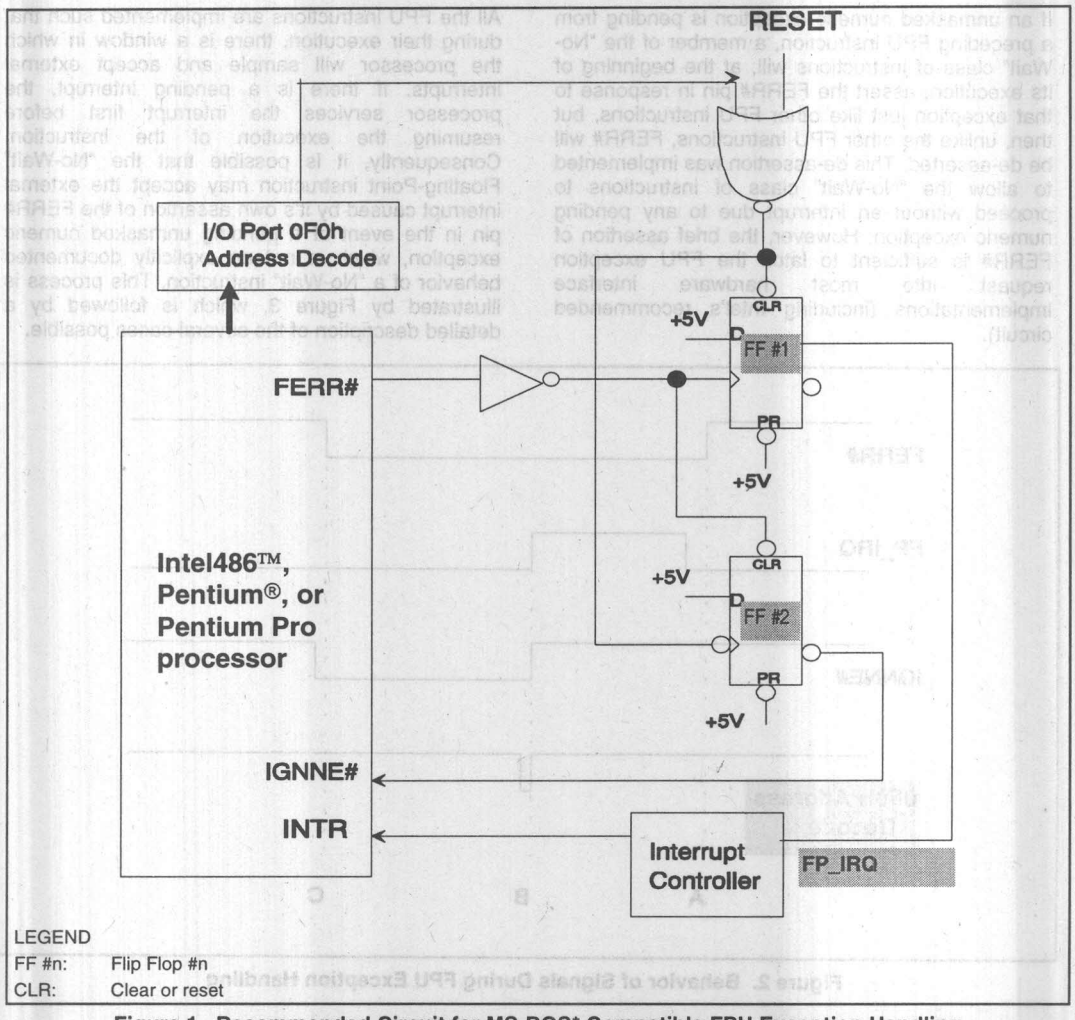


Figure 1. Recommended Circuit for MS-DOS* Compatible FPU Exception Handling

the FPU exception condition (which de-asserts FERR#). However, the circuit does not depend on the order of actions by the FPU exception handler to guarantee the correct hardware state upon exit from the handler. The flip flop which drives IGNNE# to the processor has its CLEAR input attached to the inverted FERR#. This ensures that IGNNE# can never be active when FERR# is inactive. So if the handler clears the FPU exception condition *before* the 0F0H access, IGNNE# does not get activated and left on after exit from the handler.

2.3.3 "NO-WAIT" FPU INSTRUCTIONS CAN GET FPU INTERRUPT IN WINDOW

The Pentium and the Intel486 processors implement the "No-Wait" Floating-Point instructions (FNINIT, FNCLEX, FNSTENV, FNSAVE, FNSTSW, FNSTCW, FNENI, FNDISI or FNSETPM - See Section 6.3.7 in the *Pentium® Processor Family Developer's Manual*, Volume 3) in the MS-DOS Compatibility mode (CR0.NE = 0) in the following manner:

If an unmasked numeric exception is pending from a preceding FPU instruction, a member of the "No-Wait" class of instructions will, at the beginning of its execution, assert the FERR# pin in response to that exception just like other FPU instructions, but then, unlike the other FPU instructions, FERR# will be de-asserted. This de-assertion was implemented to allow the "No-Wait" class of instructions to proceed without an interrupt due to any pending numeric exception. However, the brief assertion of FERR# is sufficient to latch the FPU exception request into most hardware interface implementations (including Intel's recommended circuit).

All the FPU instructions are implemented such that during their execution, there is a window in which the processor will sample and accept external interrupts. If there is a pending interrupt, the processor services the interrupt first before resuming the execution of the instruction. Consequently, it is possible that the "No-Wait" Floating-Point instruction may accept the external interrupt caused by it's own assertion of the FERR# pin in the event of a pending unmasked numeric exception, which is not an explicitly documented behavior of a "No-Wait" instruction. This process is illustrated by Figure 3, which is followed by a detailed description of the several cases possible.

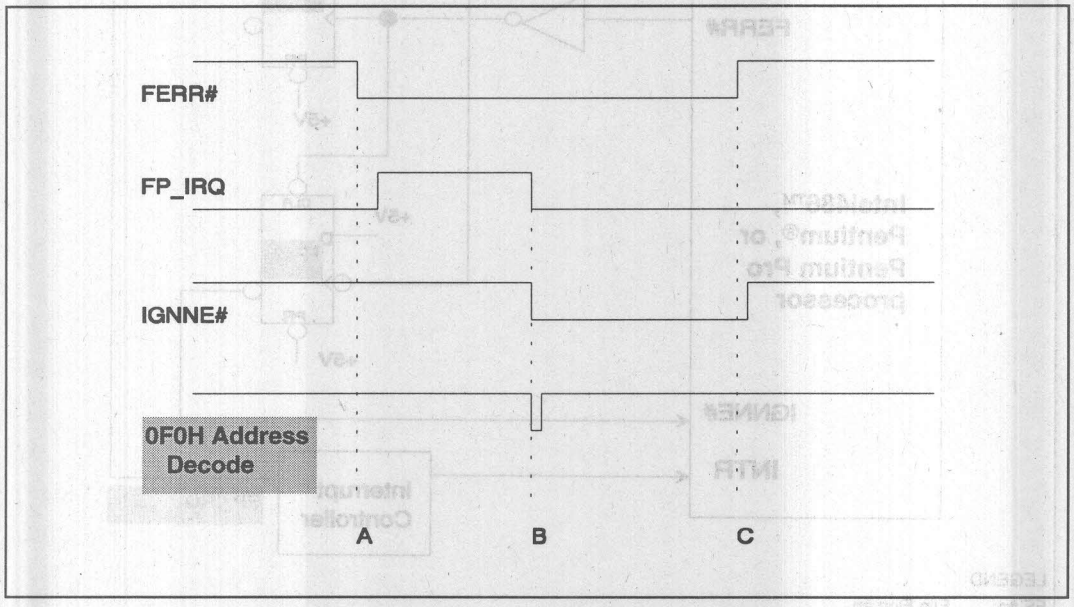


Figure 2. Behavior of Signals During FPU Exception Handling

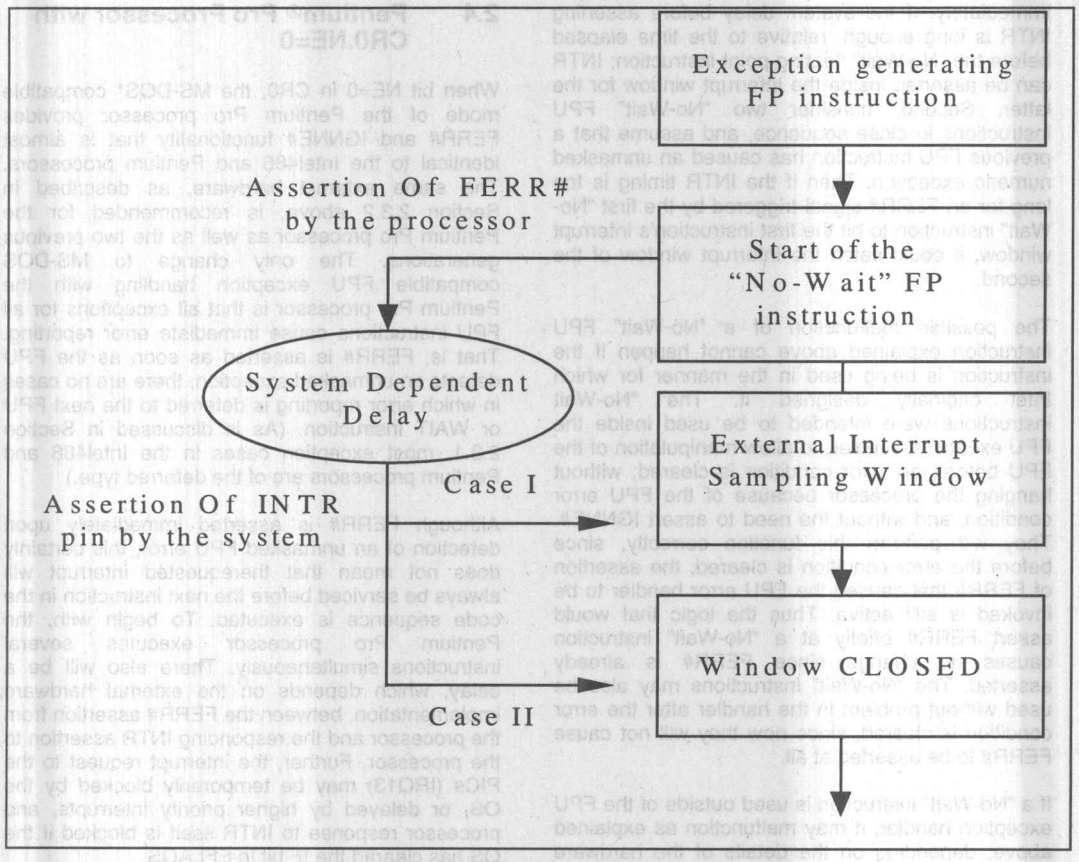


Figure 3: Timing of Receipt of External Interrupt

Figure 3 assumes that a floating-point instruction which generates a "deferred" error (as defined above in the Section 2.3.1), which asserts the FERR# pin only on encountering the next floating-point instruction, causes an unmasked numeric exception. Assume that the next floating-point instruction following this instruction is one of the "No-Wait" floating-point instructions. The FERR# pin is asserted by the processor to indicate the pending exception on encountering the "No-Wait" floating-point instruction. After the assertion of the FERR# pin the "No-Wait" floating-point instruction opens a window where the pending external interrupts are sampled.

Then there are two cases possible depending on the timing of the receipt of the interrupt via the INTR pin (asserted by the system in response to the FERR# pin) by the processor.

Case 1
If the system responds to the assertion of FERR# pin by the "No-Wait" floating-point instruction via the INTR pin during this window then the interrupt is serviced first, before resuming the execution of the "No-Wait" floating-point instruction.

Case 2
If the system responds via the INTR pin after the window has closed then the interrupt is recognized only at the next instruction boundary.

There are two other ways, in addition to Case I above, in which a "No-Wait" floating-point instruction can service a numeric exception inside its interrupt window. First, the first floating-point error condition could be of the "immediate" category (as defined in Section 2.3.1) that assert FERR#

immediately. If the system delay before asserting INTR is long enough, relative to the time elapsed before the "No-Wait" floating-point instruction, INTR can be asserted inside the interrupt window for the latter. Second, consider two "No-Wait" FPU instructions in close sequence, and assume that a previous FPU instruction has caused an unmasked numeric exception. Then if the INTR timing is too long for an FERR# signal triggered by the first "No-Wait" instruction to hit the first instruction's interrupt window, it could catch the interrupt window of the second.

The possible malfunction of a "No-Wait" FPU instruction explained above cannot happen if the instruction is being used in the manner for which Intel originally designed it. The "No-Wait instructions were intended to be used inside the FPU exception handler, to allow manipulation of the FPU before the error condition is cleared, without hanging the processor because of the FPU error condition, and without the need to assert IGNNE#. They will perform this function correctly, since before the error condition is cleared, the assertion of FERR# that caused the FPU error handler to be invoked is still active. Thus the logic that would assert FERR# briefly at a "No-Wait" instruction causes no change since FERR# is already asserted. The "No-Wait" instructions may also be used without problem in the handler after the error condition is cleared, since now they will not cause FERR# to be asserted at all.

If a "No-Wait" instruction is used outside of the FPU exception handler, it may malfunction as explained above, depending on the details of the hardware interface implementation and which particular processor is involved. The actual interrupt inside the window in the "No-Wait" instruction may be blocked by surrounding it with the instructions: PUSHFD, CLI, "No-Wait", then POPFD. (CLI blocks interrupts, and the push and pop of flags preserves and restores the original value of the interrupt flag.) However, if FERR# was triggered by the "No-Wait", its latched value and the PIC response will still be in effect. Further code can be used to check for and correct such a condition, if needed. Section 3.6 (Considerations When FPU Shared Between Tasks) discusses an important example of this type of problem and gives a solution.

2.4 Pentium® Pro Processor with CR0.NE=0

When bit NE=0 in CR0, the MS-DOS* compatible mode of the Pentium Pro processor provides FERR# and IGNNE# functionality that is almost identical to the Intel486 and Pentium processors. The same external hardware, as described in Section 2.3.2 above, is recommended for the Pentium Pro processor as well as the two previous generations. The only change to MS-DOS compatible FPU exception handling with the Pentium Pro processor is that all exceptions for all FPU instructions cause immediate error reporting. That is, FERR# is asserted as soon as the FPU detects an unmasked exception; there are no cases in which error reporting is deferred to the next FPU or WAIT instruction. (As is discussed in Section 2.3.1, most exception cases in the Intel486 and Pentium processors are of the deferred type.)

Although FERR# is asserted immediately upon detection of an unmasked FPU error, this certainly does not mean that therequested interrupt will always be serviced before the next instruction in the code sequence is executed. To begin with, the Pentium Pro processor executes several instructions simultaneously. There also will be a delay, which depends on the external hardware implementation, between the FERR# assertion from the processor and the responding INTR assertion to the processor. Further, the interrupt request to the PICs (IRQ13) may be temporarily blocked by the OS, or delayed by higher priority interrupts, and processor response to INTR itself is blocked if the OS has cleared the IF bit in EFLAGS.

However, just as with the Intel486 and Pentium processors, if the IGNNE# input is inactive, a floating-point exception which occurred in the previous FPU instruction and is unmasked causes the processor to freeze immediately when encountering the next WAIT or FPU instruction (except for "No-Wait" instructions). This means that if the FPU exception handler has not already been invoked due to the earlier exception (and therefore the handler has not cleared that exception state from the FPU), the processor is forced to wait for the handler to be invoked and handle the exception, before the processor can execute another WAIT or FPU instruction.

As explained in Section 2.3.3, if a "No-Wait" instruction is used outside of the FPU exception handler, in the Intel486 and Pentium processors, it may accept an unmasked exception from a previous FPU instruction which happens to fall within the external interrupt sampling window that is opened near the beginning of execution of all FPU instructions. This will not happen in the Pentium Pro processor, because this sampling window has been removed from the "No-Wait" group of FPU instructions.

3.0 RECOMMENDED PROTOCOL FOR MS-DOS™ AND WINDOWS* 95 COMPATIBLE HANDLERS[3]

The activities of numeric programs can be split into two major areas: program control and arithmetic. The program control part performs activities such as deciding what functions to perform, calculating addresses of numeric operands, and loop control. The arithmetic part simply adds, subtracts, multiplies, and performs other operations on the numeric operands. The processor is designed to handle these two parts separately and efficiently. An FPU exception handler, if a system chooses to implement one, is often one of the most complicated parts of the program control code.

3.1 Numeric Exceptions and their Defaults

The FPU can recognize six classes of numeric exception conditions while executing numeric instructions:

1. #I — Invalid operation
   #IS—Stack fault
   #IA—IEEE standard invalid operation
2. #Z—Divide-by-zero
3. #D—Denormalized operand
4. #O—Numeric overflow
5. #U—Numeric underflow
6. #P—Inexact result (precision)

For complete details on these exceptions and their defaults, see the *Pentium® Processor Family Developer's Manual,* Volume 3, Sections 7.1.7 through 7.1.13.

3.1.1 TWO OPTIONS FOR HANDLING NUMERIC EXCEPTIONS

Depending on options determined by the software system designer, the processor takes one of two possible courses of action when a numeric exception occurs:

1. The FPU can handle selected exceptions itself, producing a default fix-up that is reasonable in most situations. This allows the numeric program execution to continue undisturbed. Programs can mask individual exception types to indicate that the FPU should generate this safe, reasonable result whenever the exception occurs. The default exception fix-up activity is treated by the FPU as part of the instruction causing the exception; no external indication of the exception is given (except that the instruction takes longer to execute when it handles a masked exception.) When masked exceptions are detected, a flag is set in the numeric status register, but no information is preserved regarding where or when it was set.

Footnotes

[3] Although there are some differences in the way FPU exceptions are handled between MS-DOS, and WINDOWS 95 and WINDOWS 3.1 (and earlier versions), the WINDOWS operating systems operate the processor in the MS-DOS compatable mode, and the recommended protocol given here applies to all these systems. On the other hand, current versions of WINDOWS NT use the FPU native mode.

2. Alternatively, a software exception handler can be invoked to handle the exception. When a numeric exception is unmasked and the exception occurs, the FPU stops further execution of the numeric instruction and causes a branch to a software exception handler. The exception handler can then implement any sort of recovery procedures desired for any numeric exception detectable by the FPU.

3.1.2 AUTOMATIC EXCEPTION HANDLING: USING MASKED EXCEPTIONS

Each of the six exception conditions described above has a corresponding flag bit in the FPU status word and a mask bit in the FPU control word. If an exception is masked (the corresponding mask bit in the control word = 1), the processor takes an appropriate default action and continues with the computation. The processor has a default fix-up activity for every possible exception condition it may encounter. These masked-exception responses are designed to be safe and are generally acceptable for most numeric applications.

For example, if the Inexact result (Precision) exception is masked, the system can specify whether the FPU should handle a result that cannot be represented exactly by one of four modes of rounding: rounding it normally, chopping it toward zero, always rounding it up, or always down. If the Underflow exception is masked, the FPU will store a number that is too small to be represented in normalized form as a denormal (or zero if it's smaller than the smallest denormal). Note that when exceptions are masked, the FPU may detect multiple exceptions in a single instruction, because it continues executing the instruction after performing its masked response. For example, the FPU could detect a denormalized operand, perform its masked response to this exception, and then detect an underflow.

As an example of how even severe exceptions can be handled safely and automatically using the default exception responses, consider a calculation of the parallel resistance of several values using only the standard formula (Figure 4). If R1 becomes zero, the circuit resistance becomes zero. With the divide-by-zero and precision exceptions masked, the processor will produce the correct result. FDIV of R1 into 1 gives infinity, and then FDIV of (infinity +R2 +R3) into 1 gives zero.

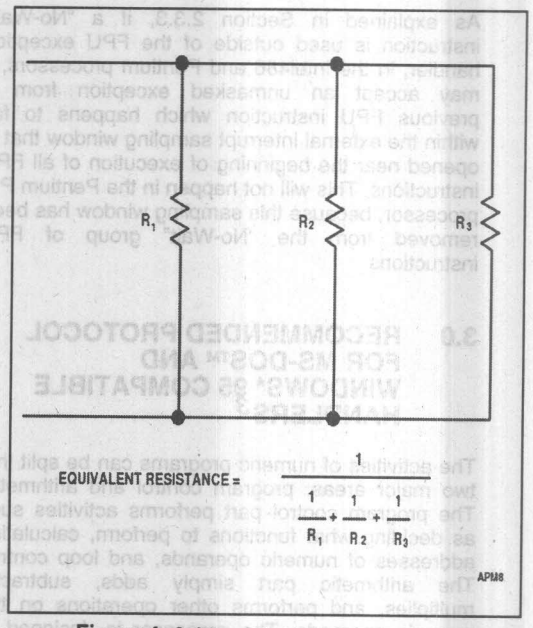


Figure 4. Arithmetic Example Using Infinity

By masking or unmasking specific numeric exceptions in the FPU control word, programmers can delegate responsibility for most exceptions to the processor, reserving the most severe exceptions for programmed exception handlers. Exception-handling software is often difficult to write, and the masked responses have been tailored to deliver the most reasonable result for each condition. For the majority of applications, masking all exceptions yields satisfactory results with the least programming effort. Certain exceptions can usefully be left unmasked during the debugging phase of software development, and then masked when the clean software is actually run. An invalid-operation exception for example, typically indicates a program error that must be corrected.

The exception flags in the FPU status word provide a cumulative record of exceptions that have occurred since these flags were last cleared. Once set, these flags can be cleared only by executing the FCLEX/FNCLEX (clear exceptions) instruction, by reinitializing the FPU with FINIT/FNINIT or FSAVE/FNSAVE, or by overwriting the flags with an FRSTOR or FLDENV instruction. This allows a programmer to mask all exceptions, run a calculation, and then inspect the status word to see

if any exceptions were detected at any point in the calculation.

3.2 Software Exception Handling

If the FPU in or with an Intel family processor (80286 and onwards) encounters an unmasked exception condition, with the system operated in the MS-DOS compatible mode and with IGNNE# not asserted, a software exception handler is invoked through a PIC and the processor's INTR pin. The FERR# (or ERROR#) output from the FPU that begins the process of invoking the exception handler may occur when the error condition is first detected, or when the processor encounters the next WAIT or FPU instruction. Which of these two cases occurs depends on the processor generation and also on which exception and which FPU instruction triggered it, as discussed earlier in Section 2. The elapsed time between the initial error signal and the invocation of the FPU exception handler depends of course on the external hardware interface, and also on whether the external interrupt for FPU errors is enabled. But the architecture ensures that the handler will be invoked before execution of the next WAIT or floating-point instruction since an unmasked floating-point exception causes the processor to freeze just before executing such an instruction (unless the IGNNE# input is active, or it is a "No-Wait" FPU instruction).

The frozen processor waits for an external interrupt, which must be supplied by external hardware 'in response to the FERR# (or ERROR#) output of the processor (or coprocessor), usually through IRQ13 on the "slave" PIC, and then through INTR. Then the external interrupt invokes the exception handling routine. Note that if the external interrupt for FPU errors is disabled when the processor executes an FPU instruction, the processor will freeze until some other (enabled) interrupt occurs if an unmasked FPU exception condition is in effect. If NE = 0 but the IGNNE# input is active, the processor disregards the exception and continues. Error reporting via an external interrupt is supported for MS-DOS compatibility. Chapter 23 of the *Pentium® Processor Family Developer's Manual,* Volume 3 contains further discussion of compatibility issues.

The references above to the ERROR# output from the FPU apply to the Intel387 and 80287 math coprocessors (NPX chips). If one of these coprocessors encounters an unmasked exception condition, it signals the exception to the 80286 or Intel386 processor using the ERROR# status line between the processor and the coprocessor. See Section 2.2 above, and Chapter 23 of the *Pentium® Processor Family Developer's Manual,* Volume 3 for differences in FPU exception handling.

The exception-handling routine is normally a part of the systems software. The routine must clear (or disable) the active exception flags in the FPU status word before executing any FP instructions that cannot complete execution when there is a pending FP exception. Otherwise, the FP instruction will trigger the FPU interrupt again, and the system will be caught in an endless loop of nested FP exceptions, and hang. In any event, the routine must clear (or disable) the active exception flags in the FPU status word after handling them, and before IRET(D). Typical exception responses may include:

- Incrementing an exception counter for later display or printing
- Printing or displaying diagnostic information (e.g., the FPU environment and registers)
- Aborting further execution, or using the exception pointers to build an instruction that will run without exception and executing it

Applications programmers should consult their operating system's reference manuals for the appropriate system response to numerical exceptions. For systems programmers, some details on writing software exception handlers are provided in Chapter 14 of the *Pentium® Processor Family Developer's Manual,* Volume 3, as well as in this application note.

As discussed in Section 2.3.2, some early FERR# to INTR hardware interface implementations are less robust than the recommended circuit. This is because they depended on the exception handler to clear the FPU exception interrupt request to the PIC (by accessing port 0F0H) *before* the handler causes FERR# to be de-asserted by clearing the exception from the FPU itself. To eliminate the chance of a

produce a numeric exception.

3.3.1 EXCEPTION SYNCHRONIZATION: WHAT, WHY AND WHEN

Exception synchronization means that the exception handler inspects and deals with the exception in the context in which it occurred. If concurrent execution is allowed, the state of the processor when it recognizes the exception is often *not* in the context in which it occurred. The processor may have changed many of its internal registers and be executing a totally different program by the time the exception occurs. If the exception handler cannot recapture the original context, it cannot reliably determine the cause of the exception or to recover successfully from the exception. To handle this situation, the FPU has special registers updated at the start of each numeric instruction to describe the state of the numeric program when the failed instruction was attempted. This provides tools to help the exception handler recapture the original context, but the application code must also be written with synchronization in mind. Overall, exception synchronization must ensure that the FPU and other relevant parts of the context are in a well defined state when the handler is invoked after an unmasked numeric exception occurs.

When the FPU signals an unmasked exception condition, it is requesting help. The fact that the exception was unmasked indicates that further numeric program execution under the arithmetic and programming rules of the FPU will probably yield invalid results. Thus the exception must be handled, and with proper synchronization, or the program will not operate reliably.

For programmers in higher-level languages, all required synchronization is automatically provided as described in Section 3.1.1, depending on options determined by the software system designer, the processor can perform one of two possible courses of action when a numeric exception occurs.

- The FPU can provide a default fix-up for selected numeric exceptions. If the FPU performs its default action for all exceptions, then the need for exception synchronization is not manifest. However, code is often ported to contexts and operating systems for which it was not originally designed. The example below illustrates that it is safest to always consider exception synchronization when designing code that uses the FPU.
- Alternatively, a software exception handler can be invoked to handle the exception. When a numeric exception is unmasked and the exception occurs, the FPU stops further execution of the numeric instruction and causes a branch to a software exception handler. When an FPU exception handler will be invoked, synchronization must always be considered to assure reliable performance.

The following examples illustrate the need to always consider exception synchronization when writing numeric code, even when the code is initially intended for execution with exceptions masked.

3.3.2 EXCEPTION SYNCHRONIZATION: EXAMPLES

In the following examples, three instructions are shown to load an integer, calculate its square root, then increment the integer. The synchronous execution of the FPU will allow both of these

Incorrect Error Synchronization:

```
FILD    COUNT       ; FPU instruction
INC     COUNT       ; integer instruction alters operand
FSQRT               ; subsequent FPU instruction -- error
        ; from previous FPU instruction detected here
```

Proper Error Synchronization:

```
FILD    COUNT           ; FPU instruction
FSQRT                   ; subsequent FPU instruction -- error from
                        ; previous FPU instruction detected here
INC COUNT               ; integer instruction alters operand
```

programs to execute correctly, with INC COUNT being executed in parallel in the processor, as long as no exceptions occur on the FILD instruction. However, if the code is later moved to an environment where exceptions are unmasked, the code in the first example will not work correctly:

In some operating systems supporting the FPU, the numeric register stack is extended to memory. To extend the FPU stack to memory, the invalid exception is unmasked. A push to a full register or pop from an empty register sets SF (Stack Fault flag) and causes an invalid operation exception. The recovery routine for the exception must recognize this situation, fix up the stack, then perform the original operation. The recovery routine will not work correctly in the first example shown in the figure. The problem is that the value of COUNT is incremented before the exception handler is invoked, so that the recovery routine will load an incorrect value of COUNT, causing the program to fail or behave unreliably.

3.3.3 PROPER EXCEPTION SYNCHRONIZATION IN GENERAL

As explained before (see Section 3.2), if the FPU encounters an unmasked exception condition a software exception handler is invoked *before* execution of the *next* WAIT or floating-point instruction. This is because an unmasked floating-point exception causes the processor to freeze immediately before executing such an instruction (unless the IGNNE# input is active, or it is a "No-Wait" FPU instruction). Exactly when the exception handler will be invoked (in the interval between when the exception is detected and the next WAIT or FPU instruction) is dependent on the processor generation, the system, and which FPU instruction and exception is involved.

To be safe in exception synchronization, one should assume the handler will be invoked at the end of the interval. Thus the program should not change any value that might be needed by the handler (such as COUNT in the above example) until *after* the *next* FPU instruction following an FPU instruction that could cause an error. If the program needs to modify such a value before the next FPU instruction (or if the next FPU instruction could also cause an error), then a WAIT instruction should be inserted before the value is modified. This will force the handling of any exception before the value is modified. A WAIT instruction should also be placed after the last floating-point instruction in an application so that any unmasked exceptions will be serviced before the task completes.

3.4 FPU Exception Handling Examples

There are many approaches to writing exception handlers. One useful technique is to consider the exception handler procedure as consisting of "prologue," "body," and "epilogue" sections of code.

In the transfer of control to the exception handler due to an INTR, NMI, or SMI, external interrupts have been disabled by hardware. The prologue performs all functions that must be protected from possible interruption by higher-priority sources. Typically, this involves saving registers and transferring diagnostic information from the FPU to memory. When the critical processing has been completed, the prologue may re-enable interrupts to allow higher-priority interrupt handlers to preempt the exception handler. The standard "prologue" not only saves the registers and transfers diagnostic information from the FPU to memory but also clears the FP exception flags in the status word. Alternatively, when it is not necessary for the

handler to be re-entrant, another technique may also be used. In this technique, the exception flags are not cleared in the "prologue" and the body of the handler must not contain any FP instructions that cannot complete execution when there is a pending FP exception. (The "No-Wait" instructions are discussed in Section 6.3.7 of the *Pentium® Processor Family Developer's Manual*, Volume 3). Note that the handler must still clear the exception flag(s) before executing the IRET. If the exception handler uses neither of these techniques the system will be caught in an endless loop of nested FP exceptions, and hang.

The body of the exception handler examines the diagnostic information and makes a response that is necessarily application-dependent. This response may range from halting execution, to displaying a message, to attempting to repair the problem and proceed with normal execution. The epilogue essentially reverses the actions of the prologue, restoring the processor so that normal execution can be resumed. The epilogue must not load an unmasked exception flag into the FPU or another exception will be requested immediately.

The following code examples show the ASM386 and ASM486 coding of three skeleton exception handlers, with the save spaces given as correct for 32 bit protected mode. They show how prologues and epilogues can be written for various situations, but the application dependent exception handling body is just indicated by comments showing where it should be placed.

The first two are very similar; their only substantial difference is their choice of instructions to save and restore the FPU. The tradeoff here is between the increased diagnostic information provided by FNSAVE and the faster execution of FNSTENV. (Also, after saving the original contents, FNSAVE re-initializes the FPU, while FNSTENV only masks all FPU exceptions.) For applications that are sensitive to interrupt latency or that do not need to examine register contents, FNSTENV reduces the duration of the "critical region," during which the processor does not recognize another interrupt request. (See the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 6.2.1.6 for a complete description of the FPU save image.)

After the exception handler body, the epilogues prepare the processor to resume execution from the point of interruption (i.e., the instruction following the one that generated the unmasked exception). Notice that the exception flags in the memory image that is loaded into the FPU are cleared to zero prior to reloading (in fact, in these examples, the entire status word image is cleared).

Example 1 and Example 2 assume that the exception handler itself will not cause an unmasked exception. Where this is a possibility, the general approach shown in 3 can be employed. The basic technique is to save the full FPU state and then to load a new control word in the prologue. Note that considerable care should be taken when designing an exception handler of this type to prevent the handler from being reentered endlessly.

Example 1. Full-State Exception Handler

```
SAVE_ALL    PROC
;
; SAVE REGISTERS, ALLOCATE STACK SPACE FOR FPU STATE IMAGE
      PUSH  EBP
      .
      .
      MOV   EBP, ESP
      SUB   ESP, 108 ; ALLOCATES 108 BYTES (32-bit PROTECTED MODE SIZE)
;SAVE FULL FPU STATE, RESTORE INTERRUPT ENABLE FLAG (IF)
      FNSAVE      [EBP-108]
      PUSH [EBP + OFFSET_TO_EFLAGS] ; COPY OLD EFLAGS TO STACK TOP
      POPFD       ; RESTORE IF TO VALUE BEFORE FPU EXCEPTION
;
; APPLICATION-DEPENDENT EXCEPTION HANDLING CODE GOES HERE
;
; CLEAR EXCEPTION FLAGS IN STATUS WORD (WHICH IS IN MEMORY)
```

```
; RESTORE MODIFIED STATE IMAGE
      MOV         BYTE PTR [EBP-104], 0H
      FRSTOR      [EBP-108]
; DE-ALLOCATE STACK SPACE, RESTORE REGISTERS
      MOV         ESP, EBP
      .
      .
      POP         EBP
;
; RETURN TO INTERRUPTED CALCULATION
      IRETD
SAVE_ALL    ENDP
```

Example 2. Reduced-Latency Exception Handler

```
SAVE_ENVIRONMENT  PROC
;
; SAVE REGISTERS, ALLOCATE STACK SPACE FOR FPU ENVIRONMENT
      PUSH        EBP
      .
      .
      MOV         EBP, ESP
      SUB         ESP, 28 ; ALLOCATES 28 BYTES (32-bit PROTECTED MODE SIZE)
;SAVE ENVIRONMENT, RESTORE INTERRUPT ENABLE FLAG (IF)
      FNSTENV     [EBP-28]
      PUSH [EBP + OFFSET_TO_EFLAGS] ; COPY OLD EFLAGS TO STACK TOP
      POPFD       ; RESTORE IF TO VALUE BEFORE FPU EXCEPTION

;
; APPLICATION-DEPENDENT EXCEPTION HANDLING CODE GOES HERE
;
; CLEAR EXCEPTION FLAGS IN STATUS WORD (WHICH IS IN MEMORY)
; RESTORE MODIFIED ENVIRONMENT IMAGE
      MOV         BYTE PTR [EBP-24], 0H
      FLDENV      [EBP-28]
; DE-ALLOCATE STACK SPACE, RESTORE REGISTERS
      MOV         ESP, EBP
      .
      .
      POP         EBP
;
; RETURN TO INTERRUPTED CALCULATION
      IRETD
SAVE_ENVIRONMENT  ENDP
```

Example 3. Reentrant Exception Handler

```
LOCAL_CONTROL DW ?      ; ASSUME INITIALIZED
      .
      .
REENTRANT   PROC
;
; SAVE REGISTERS, ALLOCATE STACK SPACE FOR FPU STATE IMAGE
```

```
        PUSH  EBP
        .
        .
        MOV         EBP, ESP
        SUB         ESP, 108 ; ALLOCATES 108 BYTES (32-bit PROTECTED MODE SIZE)

; SAVE STATE, LOAD NEW CONTROL WORD, RESTORE INTERRUPT ENABLE FLAG (IF)
        FNSAVE      [EBP-108]
        FLDCW       LOCAL_CONTROL
        PUSH [EBP + OFFSET_TO_EFLAGS] ; COPY OLD EFLAGS TO STACK TOP
        POPFD       ; RESTORE IF TO VALUE BEFORE FPU EXCEPTION

        .
        .
;
; APPLICATION-DEPENDENT EXCEPTION HANDLING CODE GOES HERE. AN UNMASKED EXCEPTION
; GENERATED HERE WILL CAUSE THE EXCEPTION HANDLER TO BE REENTERED.
; IF LOCAL STORAGE IS NEEDED, IT MUST BE ALLOCATED ON THE STACK.
;
        .
        .
; CLEAR EXCEPTION FLAGS IN STATUS WORD (WHICH IS IN MEMORY)
; RESTORE MODIFIED STATE IMAGE
        MOV         BYTE PTR [EBP-104], 0H
        FRSTOR      [EBP-108]
; DE-ALLOCATE STACK SPACE, RESTORE REGISTERS
        MOV         ESP, EBP
        .
        .
        POP         EBP
;
; RETURN TO POINT OF INTERRUPTION
        IRETD
REENTRANT   ENDP
```

3.5 Need for Preserving the State of IGNNE# Circuit if Use FPU and SMM

In Section 2.3.2 the recommended circuit (Figure 2) for MS-DOS compatible FPU exception handling for Intel486 processors and beyond contains two flip flops. When the FPU exception handler accesses I/O port 0F0H it clears the IRQ13 interrupt request output from Flip Flop #1 and also clocks out the IGNNE# signal (active) from Flip Flop #2. The assertion of IGNNE# may be used by the handler if needed to execute any FPU instruction while ignoring the pending FPU errors. The problem here is that the state of Flip Flop #2 is effectively an additional (but hidden) status bit that can affect processor behavior, and so ideally should be saved upon entering SMM, and restored before resuming to normal operation. If this is not done, and also the SMM code saves the FPU state, AND an FPU error handler is being used which relies on IGNNE# assertion, then (very rarely) the FPU handler will nest inside itself and malfunction. The following example shows how this can happen.

The problem will only occur if the processor enters SMM between the OUT and the FLDCW instructions. But if that happens, AND the SMM code saves the FPU state using FNSAVE, then the IGNNE# Flip Flop will be cleared (because FNSAVE clears the FPU errors and thus de-asserts FERR#). When the processor returns from SMM it will restore the FPU state with FRSTOR, which will re-assert FERR#, but the IGNNE# Flip Flop will not get set. Then when the FPU error handler executes the FLDCW instruction, the active error condition will cause the processor to re-enter the FPU error handler from the beginning. This may cause the handler to malfunction.

Note that NMI (or any interrupt through INTR that is enabled inside the FPU exception handler) will cause this same problem, if the interrupt routine saves and restores the FPU state, and it happens to occur between the OUT and the FLDCW instructions. SMI is the main focus here because it is much more likely to invoke FNSAVE/FRSTOR than other interrupts because of 0V suspend (see below). The problem can easily be eliminated from all interrupts besides SMI and NMI by not enabling INTR inside the FPU exception handler.

To avoid this problem, Intel recommends two measures:

1. Do not use the FPU for calculations inside SMM code (or code for NMI, or any other interrupts enabled inside the FPU exception handler). (The normal power management, and sometimes security, functions provided by SMM have no need for FPU calculations; if they are needed for some special case, use scaling or emulation instead.) This eliminates the need to do FNSAVE/FRSTOR inside SMM code, *except* when going into an 0V suspend state (in which, in order to save power, the processor is turned off completely, requiring its complete state to be saved).
2. The system should not call upon SMM code to put the processor into 0V suspend while the processor is running FPU calculations, or just after an interrupt has occurred. Normal power management protocol avoids this by going into power down states only after timed intervals in which no system activity occurs.

3.6 Considerations When FPU Shared Between Tasks

The Intel Architecture allows speculative deferral of floating-point state swaps on task switches. This feature allows postponing an FPU state swap until an FPU instruction is actually encountered in another task. Since kernel tasks rarely use floating-point, and some applications do not use floating-point or use it infrequently, the amount of time saved by avoiding unnecessary stores of the floating-point state is significant. Speculative deferral of FPU saves does, however, place an extra burden on the kernel in three key ways:

1. The kernel must keep track of which thread owns the FPU, which may be different from the currently executing thread.
2. The kernel must associate any floating-point exceptions with the generating task. This requires special handling since floating-point exceptions are delivered asynchronous with other system activity.
3. There are conditions under which spurious floating-point exception interrupts are generated, which the kernel must recognize and discard.

Suppose that the FPU exception handler includes the following sequence:

```
FNSTSW save_sw          ; save the FPU status word using a "No-Wait" FPU instruction
OUT 0F0H, AL            ; clears IRQ13 & activates IGNNE#
....
FLDCW new_cw ; loads new CW ignoring FPU errors, since IGNNE# is assumed active; or any
             ; other FPU instruction that is not a "No-Wait" type will cause the
same problem
....
FCLEX                   ; clear the FPU error conditions & thus turn off FERR# & reset the
IGNNE# FF
```

3.6.1 SPECULATIVELY DEFERRING FPU SAVES, GENERAL OVERVIEW

In order to support multi-tasking, each thread in the system needs a save area for the general purpose registers, and each task that is allowed to use floating-point needs an FPU save area large enough to hold the entire FPU stack and associated FPU state such as the control word and status word. (See the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 6.2.1.6 for a complete description of the FPU save image.)

On a task switch, the general purpose registers are swapped out to their save area for the suspending thread, and the registers of the resuming thread are loaded. The FPU state does not need to be saved at this point. If the resuming thread does not use the FPU before it is itself suspended, then both a save and a load of the FPU state has been avoided. It is often the case that several threads may be executed without any usage of the FPU.

The processor supports speculative deferral of FPU saves via interrupt 7 "Device Not Available" (DNA), used in conjunction with CR0 bit 3, the "Task Switched" bit (TS). (See the *Pentium® Processor Family Developer's Manual*, Volume 3, Sections 10.1.3 & 14.9.7) Every task switch via the hardware supported task switching mechanism (see Section 13.5 of the *Pentium® Processor Family Developer's Manual*, Volume 3) sets TS. Multi-threaded kernels that use software task switching[4] can set the TS bit by reading CR0, ORing a '1' into bit 3, and writing back CR0[5]. Any subsequent floating-point instructions (now being executed in a new thread context) will fault via interrupt 7 before execution.

Footnotes

[4] In a software task switch, the operating system uses a sequence of instructions to save the suspending thread's state and restore the resuming thread's state instead of the single long, noninterruptable task switch operation provided by the Intel Architecture.

[5] Although CR0, bit 2, the emulation flag (EM), also causes a DNA exception, *do not* use the EM bit as a surrogate for TS. EM means that no floating-point unit is available and that FP instructions must be emulated. Using EM to trap on task switches is not compatible with Intel Architecture MMX™ Technology. If the EM flag is set, MMX instructions raise the invalid opcode exception.

This allows the DNA handler to save the old floating-point context and reload the FPU state for the current thread. The handler should clear the TS bit before exit using the CLTS instruction. On return from the handler the faulting thread will proceed with its floating-point computation.

Some operating systems save the FPU context on every task switch, typically because they also change the linear address space between tasks. The problem and its solution discussed below apply to these operating systems also.

3.6.2 TRACKING FPU OWNERSHIP

Since the contents of the FPU may not belong to the currently executing thread, the thread identifier for the last FPU user needs to be tracked separately. This is not complicated -- the kernel should simply provide a variable to store the thread identifier of the FPU owner, separate from the variable that stores the identifier for the currently executing thread. This variable is updated in the DNA exception handler, and is used by the DNA exception handler to find the FPU save areas of the old and new threads. A simplified flow for a DNA exception handler is then:

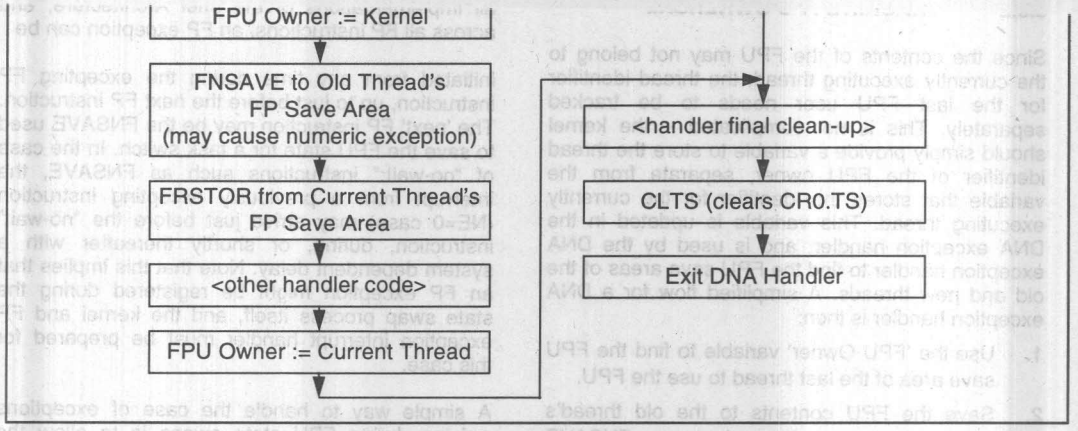
1. Use the 'FPU Owner' variable to find the FPU save area of the last thread to use the FPU.
2. Save the FPU contents to the old thread's save area, typically using an FNSAVE instruction.
3. Set the 'FPU Owner' variable to the identify the currently executing thread.
4. Reload the FPU contents from the new thread's save area, typically using an FRSTOR instruction.
5. Clear TS using the CLTS instruction and exit the DNA exception handler.

While this flow covers the basic requirements for speculatively deferred FPU state swaps, there are some additional subtleties that need to be handled in a robust implementation.

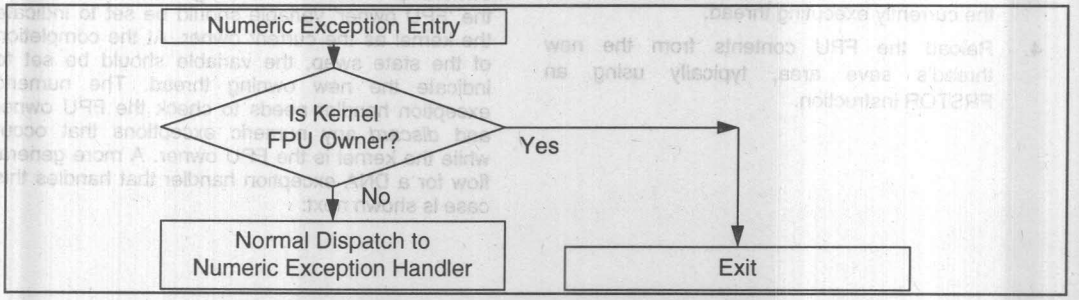
3.6.3 INTERACTION OF FPU STATE SAVES AND FP EXCEPTION ASSOCIATION

Recall these key points from earlier in this document: When considering FP exceptions across all implementations of the Intel Architecture, and across all FP instructions, an FP exception can be initiated from any time during the excepting FP instruction, up to just before the next FP instruction. The 'next' FP instruction may be the FNSAVE used to save the FPU state for a task switch. In the case of "no-wait:" instructions such as FNSAVE, the interrupt from a previously excepting instruction (NE=0 case) may arrive just before the "no-wait" instruction, during, or shortly thereafter with a system dependent delay. Note that this implies that an FP exception might be registered during the state swap process itself, and the kernel and FP exception interrupt handler must be prepared for this case.

A simple way to handle the case of exceptions arriving during FPU state swaps is to allow the kernel to be one of the FPU owning threads. A reserved thread identifier is used to indicate kernel ownership of the FPU. During an FP state swap, the 'FPU owner' variable should be set to indicate the kernel as the current owner. At the completion of the state swap, the variable should be set to indicate the new owning thread. The numeric exception handler needs to check the FPU owner and *discard* any numeric exceptions that occur while the kernel is the FPU owner. A more general flow for a DNA exception handler that handles this case is shown next:



Numeric exceptions received while the kernel owns the FPU for a state swap must be discarded in the kernel without being dispatched to a handler. A flow for a numeric exception dispatch routine is shown below:



It may at first glance seem that there is a possibility of FP exceptions being lost because of exceptions that are discarded during state swaps. This is not the case, as the exception will be re-issued when the FP state is reloaded. Walking through state swaps both with and without pending numeric exceptions will clarify the operation of these two handlers.

Case 1: FPU State Swap Without Numeric Exception

Assume two threads 'A' and 'B', both using the floating-point unit. Let A be the thread to have most recently executed a FP instruction, with no pending numeric exceptions. Let B be the currently executing thread. CR0.TS was set when thread A was suspended. When B starts to execute a FP instruction the instruction will fault with the DNA exception because TS is set.

At this point the handler is entered, and eventually it finds that the current FPU Owner is not the currently executing thread. To guard the FPU state swap from extraneous numeric exceptions, the FPU Owner is set to be the kernel. The old owner's FPU state is saved with FNSAVE, and the current thread's FPU state is restored with FRSTOR. Before exiting, the FPU owner is set to thread B, and the TS bit is cleared.

On exit, thread B resumes execution of the faulting FP instruction and continues.

Case 2: FPU State Swap with Discarded Numeric Exception

Again, assume two threads 'A' and 'B', both using the floating-point unit. Let A be the thread to have most recently executed a FP instruction, but this time let there be a pending numeric exception. Let B be the currently executing thread. When B starts to execute a FP instruction the instruction will fault with the DNA exception and enter the DNA handler. (If both numeric and DNA exceptions are pending, the DNA exception takes precedence, in order to support handling the numeric exception in its own context.)

When the FNSAVE starts, it will trigger an interrupt via FERR# because of the pending numeric exception. After some system dependent delay, the numeric exception handler is entered. It may be entered before the FNSAVE starts to execute, or it may be entered shortly after execution of the FNSAVE. Since the FPU Owner is the kernel, the numeric exception handler simply exits, discarding the exception. The DNA handler resumes execution, completing the FNSAVE of the old FP context of thread A and the FRSTOR of the FP context for thread B.

Thread A eventually gets an opportunity to handle the exception that was discarded during the task switch. After some time, thread B is suspended, and thread A resumes execution. When thread A starts to execute an FP instruction, once again the DNA exception handler is entered. B's FPU state is FNSAVE'ed, and A's FPU state is FRSTOR'ed. Note that in restoring the FPU state from A's save area, the pending numeric exception flags are reloaded in to the FP status word. Now when the DNA exception handler returns, thread A resumes execution of the faulting FP instruction just long enough to immediately generate a numeric exception, which now gets handled in the normal way. The net result is that the task switch and resulting FPU state swap via the DNA exception handler causes an 'extra' numeric exception which can be safely discarded.

3.6.4 INTERRUPT ROUTING FROM THE KERNEL

In MS-DOS, an application that wishes to handle numeric exceptions hooks interrupt 2 by placing its handler address in the interrupt vector table, and exiting via a jump to the previous interrupt 2 handler. Protected mode systems that run MS-DOS programs under a subsystem can emulate this exception delivery mechanism. For example, assume a protected mode O.S. that runs with CR.NE = 1, and that runs MS-DOS programs in a virtual machine subsystem. The MS-DOS program is set up in a virtual machine that provides a virtualized interrupt table. The MS-DOS application hooks interrupt 2 in the virtual machine in the normal way. A numeric exception will trap to the kernel via the real INT 16 residing in the kernel at ring 0. The INT 16 handler in the kernel then locates the correct MS-DOS virtual machine, and reflects the interrupt to the virtual machine monitor. The virtual machine monitor then emulates an interrupt by jumping through the address in the virtualized interrupt table, eventually reaching the application's numeric exception handler.

4.0 DIFFERENCES FOR HANDLERS USING NATIVE MODE

The 8087 has a pin INT which it asserts when an unmasked exception occurs. But there is no interrupt input pin in the 8086 or 8088 dedicated to its attachment, nor an interrupt vector number in the 8086 or 8088 specific for an FPU error assertion. But beginning with the Intel 80286 and 80287, hardware connections were dedicated to support the FPU exception, and interrupt vector 16 assigned to it.

4.1 Origin with 80286 and 80287; Intel386™ Processor and Intel387 Math Coprocessor

The 80286 and 80287 and Intel386 processor and Intel387 math coprocessor pairs are each provided with ERROR# pins that are recommended to be connected between the processor and FPU. If this is done, when an unmasked FPU exception occurs, the FPU records the exception, and asserts its ERROR# pin. The processor recognizes this active condition of the ERROR# status line immediately before execution of the next WAIT or FPU instruction (except for the "N0-Wait" type) in its instruction stream, and branches to the routine at interrupt vector 16. Thus an FPU exception will be handled before any other FPU instruction (after the one causing the error) is executed (except for "No-Wait" instructions, which will be executed without triggering the FPU exception interrupt, but it will remain pending).

Using the dedicated interrupt 16 for FPU exception handling is referred to as the native mode. It is the simplest approach, and the one recommended most highly by Intel.

4.2 Changes with Intel486™, Pentium® and Pentium Pro Processors with CR0.NE=1

With these latest three generations of the Intel Architecture, more enhancements and speedup features have been added to the corresponding FPUs. Also, the FPU is now built into the same chip as the processor, which allows further increases in the speed at which the FPU can operate as part of the integrated system. This also means that the native mode of FPU exception handling, selected by setting bit NE of register CR0 to 1, is now entirely internal.

If an unmasked exception occurs during an FPU instruction, the FPU records the exception internally, and triggers the exception handler through interrupt 16 immediately before execution of the next WAIT or FPU instruction (except for "No-Wait" instructions, which will be executed as described in Section 4.1 above).

An unmasked numerical exception causes the FERR# output to be activated even with NE=1, and at exactly the same point in the program flow as it would have been asserted if NE were zero. However, the system would not connect FERR# to a PIC to generate INTR when operating in the native, internal mode. (If the hardware of a system has FERR# connected to trigger IRQ13 in order to support MS-DOS, but an OS using the native mode is actually running the system, it is the OSs responsibility to make sure that IRQ13 is not enabled in the slave PIC.) With this configuration a system is immune to the problem discussed in Section 2.3.3, where for Intel486 and Pentium processors a "No-Wait" FPU instruction can get an FPU exception.

4.3 Considerations When FPU Shared Between Tasks Using Native Mode

The protocols recommended in Section 3.6 for MS-DOS compatible FPU exception handlers that are shared between tasks may be used without change with the native mode. However, the protocols for a handler written specifically for native mode can be simplified, because the problem of a spurious floating-point exception interrupt occurring while the kernel is executing cannot happen in native mode.

The problem as actually found in practical code in a MS-DOS compatible system happens when the DNA handler uses FNSAVE to switch FPU contexts. If an FPU exception is active, then FNSAVE triggers FERR# briefly, which usually will cause the FPU exception handler to be invoked inside the DNA handler. In native mode, neither FNSAVE nor any other "No-Wait" instructions can trigger interrupt 16. (As discussed above, FERR# gets asserted independent of the value of the NE bit, but when NE=1, the OS should not enable its path through the PIC.) Another possible (very rare) way a floating-point exception interrupt could occur while the kernel is executing is by an FPU immediate exception case having its interrupt delayed by the external hardware until execution has switched to the kernel. This also cannot

happen in native mode because there is no delay through external hardware.

Thus the native mode FPU exception handler can omit the test to see if the kernel is the FPU owner, and the DNA handler for a native mode system can omit the step of setting the kernel as the FPU owner at the handler's beginning. Since however these simplifications are minor and save little code, it would be a reasonable and conservative habit (as long as the MS-DOS compatible mode is widely used) to include these steps in all systems.

Note that the special DP (Dual Processing) mode for Pentium processors, and also the more general Intel MultiProcessor Specification for systems with multiple Pentium or Pentium Pro processors, support FPU exception handling only in the native mode. Intel does not recommend using the MS-DOS compatible FPU mode for systems using more than one processor.

intel®

AP-485

APPLICATION NOTE

Intel Processor Identification and the CPUID Instruction

January 1998

Order Number: 241618-007

Intel Processor Identification and the CPUID Instruction

REVISION HISTORY

Revision	Revision History	Date
-001	Original Issue.	05/93
-002	Modified Table 2, Intel486™ and Pentium® Processor Signatures.	10/93
-003	Updated to accommodate new processor versions. Program examples modified for ease of use, section added discussing BIOS recognition for OverDrive® processors, and feature flag information updated.	09/94
-004	Updated with Pentium Pro and OverDrive processors information. Modified Tables1, 3 and 5. Inserted Tables 6, 7 and 8. Inserted Sections 3.4. and 3.5.	12/95
-005	Added Figures 1 and 3. Added Footnotes 1 and 2. Modified Figure 2. Added Assembly code example in Section 4. Modified Tables 3, 5 and 7. Added two bullets in Section 5.0. Modified cpuid3b.ASM and cpuid3b.C programs to determine if processor features MMX™ technology. Modified Figure 6.0.	11/96
-006	Modified Table 3. Added reserved for future member of P6 family of processors entry. Modified table header to reflect Pentium II processor family. Modified Table 5. Added SEP bit definition. Added Section 3.5. Added Section 3.7 and Table 9. Corrected references of P6 family to reflect correct usage. Modified cpuid3a.asm, cpuid3b.asm and cpuid3.c example code sections to check for SEP feature bit and to check for, and identify, the Pentium II processor. Added additional disclaimer related to designers and errata.	3/97
-007	Modified Table 2. Added Pentium II processor, model 5 entry. Modified existing Pentium II processor entry to read "Pentium II processor, model 3". Modified Table 5. Added additional feature bits, PAT and FXSR. Modified Table 7. Added entries 44h and 45h. Removed the note "Do not assume a value of 1 in a feature flag indicates that a given feature is present. For future feature flags, a value of 1 may indicate that the specific feature is not present" in Section 4.0. Modified cpuid3b.asm and cpuid3.c example code section to check for, and identify, the Pentium II processor, model 5. Modified existing Pentium II processor code to print Pentium II processor, model 3.	1/98

1.0. INTRODUCTION

As the Intel Architecture evolves with the addition of new generations and models of processors (8086, 8088, Intel286, Intel386™, Intel486™, Pentium® processors, Pentium OverDrive® processors, Pentium processors with MMX™ technology, Pentium OverDrive processors with MMX technology, Pentium Pro processors and Pentium II processors), it is essential that Intel provide an increasingly sophisticated means with which software can identify the features available on each processor. This identification mechanism has evolved in conjunction with the Intel Architecture as follows:

1. Originally, Intel published code sequences that could detect minor implementation or architectural differences to identify processor generations.
2. Later, with the advent of the Intel386™ processor, Intel implemented processor signature identification which provided the processor family, model, and stepping numbers to software, but only upon reset.
3. As the Intel Architecture evolved, Intel extended the processor signature identification into the CPUID instruction. The CPUID instruction not only provides the processor signature, but also provides information about the features supported by and implemented on the Intel processor.

The evolution of processor identification was necessary because, as the Intel Architecture proliferates, the computing market must be able to tune processor functionality across processor generations and models that have differing sets of features. Anticipating that this trend will continue with future processor generations, the Intel Architecture implementation of the CPUID instruction is extensible.

This application note explains how to use the CPUID instruction in software applications, BIOS implementations, and various processor tools. By taking advantage of the CPUID instruction, software developers can create software applications and tools that can execute compatibly across the widest range of Intel processor generations and models, past, present, and future.

1.1. Update Support

You can obtain new Intel processor signature and feature bits information from the developer's manual, programmer's reference manual or appropriate documentation for a processor. In addition, you can receive updated versions of the programming examples included in this application note; contact your Intel representative for more information.

2.0. DETECTING THE CPUID INSTRUCTION

Starting with the Intel486 family and subsequent Intel processors, Intel provides a straightforward method for determining whether the processor's internal architecture is able to execute the CPUID instruction. This method uses the ID flag in bit 21 of the EFLAGS register. If software can change the value of this flag, the CPUID instruction is executable. See Figure 1.

NOTE

Only in some Intel486 and succeeding processors. Bit 21 in the Intel386 processor's Eflag register cannot be changed by software, and the Intel386 processor cannot execute the CPUID instruction. Execution of CPUID on a processor that does not support this instruction will result in an invalid opcode exception.

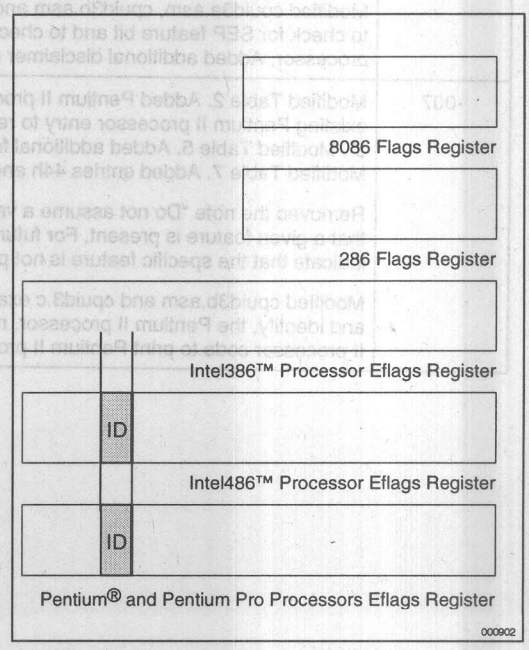


Figure 1. Flag Register Evolution

The POPF, POPFD, PUSHF, and PUSHFD instructions are used to access the Flags, Eflags register. The program examples at the end of this application note show how you use the PUSHFD instruction to read and the POPFD instruction to change the value of the ID flag.

3.0. OUTPUT OF THE CPUID INSTRUCTION

Figure 2 summarizes the outputs of the CPUID instruction. The function of the CPUID instruction is fully dependent upon the contents of the EAX register. This means, by placing different values in the EAX register and then executing CPUID, the CPUID instruction will perform a specific function dependent upon whatever value is resident in the EAX register (see Table 1). In order to determine the highest acceptable value for the EAX register input and CPUID operation, the program should set the EAX register parameter value to "0" and then execute the CPUID instruction as follows:

```
MOV EAX, 00H
CPUID
```

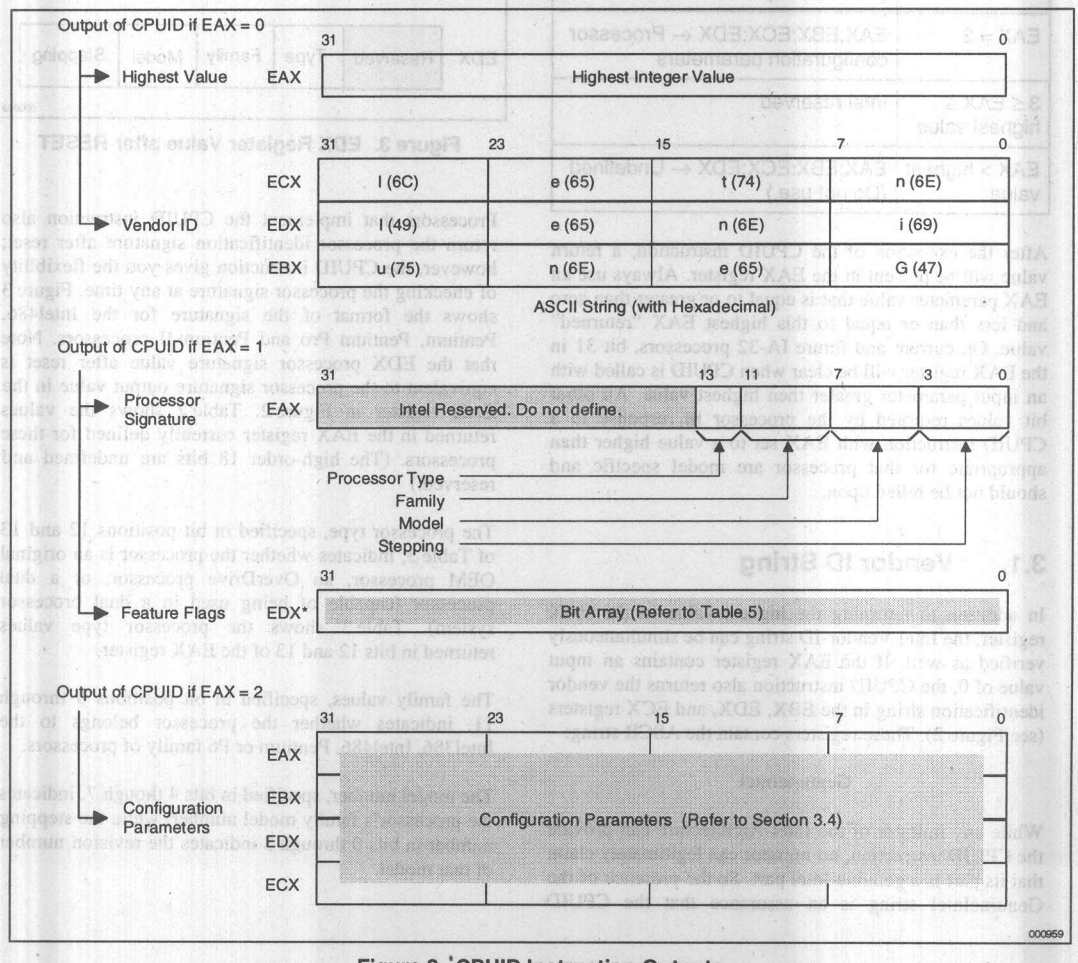


Figure 2. CPUID Instruction Outputs

EAX = 2	EAX:EBX:ECX:EDX ← Processor configuration parameters
3 ≤ EAX ≤ highest value	Intel reserved
EAX > highest value	EAX:EBX:ECX:EDX ← Undefined (Do not use.)

After the execution of the CPUID instruction, a return value will be present in the EAX register. Always use an EAX parameter value that is equal to or greater than zero and less than or equal to this highest EAX "returned" value. On current and future IA-32 processors, bit 31 in the EAX register will be clear when CPUID is called with an input parameter greater then highest value. All other bit values returned by the processor in response to a CPUID instruction with EAX set to a value higher than appropriate for that processor are model specific and should not be relied upon.

3.1. Vendor ID String

In addition to returning the highest value in the EAX register, the Intel Vendor-ID string can be simultaneously verified as well. If the EAX register contains an input value of 0, the CPUID instruction also returns the vendor identification string in the EBX, EDX, and ECX registers (see Figure 2). These registers contain the ASCII string:

GenuineIntel

While any imitator of the Intel Architecture can provide the CPUID instruction, no imitator can legitimately claim that its part is a genuine Intel part. So the presence of the GenuineIntel string is an assurance that the CPUID

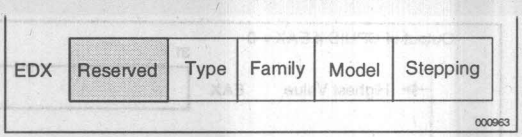


Figure 3. EDX Register Value after RESET

Processors that implement the CPUID instruction also return the processor identification signature after reset; however, the CPUID instruction gives you the flexibility of checking the processor signature at any time. Figure 3 shows the format of the signature for the Intel486, Pentium, Pentium Pro and Pentium II processors. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register in Figure 2. Table 2 shows the values returned in the EAX register currently defined for these processors. (The high-order 18 bits are undefined and reserved.)

The processor type, specified in bit positions 12 and 13 of Table 3, indicates whether the processor is an original OEM processor, an OverDrive processor, or a dual processor (capable of being used in a dual processor system). Table 3 shows the processor type values returned in bits 12 and 13 of the EAX register.

The family values, specified in bit positions 8 through 11, indicates whether the processor belongs to the Intel386, Intel486, Pentium or P6 family of processors.

The model number, specified in bits 4 though 7, indicates the processor's family model number, while the stepping number in bits 0 through 3 indicates the revision number of that model.

Table 2. Intel486™, Pentium® Processor Family, OverDrive®, Pentium Pro Processor and Pentium II Processor Signatures

Type	Family	Model	Stepping	Description
00	0100	0000 and 0001	xxxx (1)	Intel486™ DX processors
00	0100	0010	xxxx (1)	Intel486 SX processors
00	0100	0011	xxxx (1)	Intel 487 processors
00	0100	0011	xxxx (1)	IntelDX2™ processors
00	0100	0011	xxxx (1)	IntelDX2 OverDrive® processors
00	0100	0100	xxxx (3)	Intel486 SL processor
00	0100	0101	xxxx (1)	IntelSX2™ processors
00	0100	0111	xxxx (3)	Write-Back Enhanced IntelDX2 processors
00	0100	1000	xxxx (3)	IntelDX4™ processors
00, 01	0100	1000	xxxx (3)	IntelDX4 OverDrive processors
00	0101	0001	xxxx (2)	Pentium® processors (60, 66)
00	0101	0010	xxxx (2)	Pentium processors (75, 90, 100, 120, 133, 150, 166, 200)
00	0101	0001	xxxx (2)	Pentium OverDrive processor for Pentium processor (60, 66)
01 (4)	0101	0010	xxxx (2)	Pentium OverDrive processor for Pentium processor (75, 90, 100, 120, 133)
01	0101	0011	xxxx (2)	Pentium OverDrive processors for Intel486 processor-based systems
00	0101	0100	xxxx (2)	Pentium processor with MMX™ technology (166, 200)
01	0101	0100	xxxx (2)	Reserved for a future OverDrive processor for Pentium processor (75, 90, 100, 120, 133)
00	0110	0001	xxxx (2)	Pentium Pro processor
00	0110	0011	xxxx (2)	Pentium II processor, model 3
00	0110	0101	xxxx (2)	Pentium II processor, model 5
01	0110	0011	xxxx (2)	Reserved for a future OverDrive processor for Pentium Pro processor

NOTES:

1. This processor does not implement the CPUID instruction.
2. Refer to the Intel486™ documentation, the *Pentium® Processor Specification Update* (Order Number 242480), the *Pentium® Pro Processor Specification Update* (Order Number 242689), or the *Pentium® II Processor Specification Update* (Order Number 243337) for the latest list of stepping numbers.
3. Stepping 3 implements the CPUID instruction.
4. The definition of the type field for the OverDrive® processor is 01h. An errata on the Pentium OverDrive processor will always return 00h as the type.

Table 3. Processor Type (Bit Positions 13 and 12)

Value	Description
00	Original OEM processor
01	OverDrive® processor
10	Dual processor
11	Intel reserved (Do not use.)

Older versions of Intel486 SX, Intel486 DX and IntelDX2™ processors do not support the CPUID instruction, so they can only return the processor signature at reset. Refer to Table 2 to determine which processors support the CPUID instruction.

NOTE

All Intel486 SL-enhanced and Write-Back enhanced processors are capable of executing the CPUID instruction. See Table 2.

Figure 4 shows the format of the processor signature for Intel386 processors, which are different from other processors. Table 4 shows the values currently defined for these Intel386 processors.

3.3. Feature Flags

When the EAX register contains a value of 1, the CPUID instruction (in addition to loading the processor signature in the EAX register) loads the EDX register with the feature flags. The current feature flags (when Flag = 1) indicate what features the processor supports. Table 5 lists the currently defined feature flag values.

For future processors, refer to the programmer's reference manual, user's manual, or the appropriate documentation for the latest feature flag values.

Use the feature flags in your applications to determine which processor features are supported. By using the CPUID feature flags to predetermine processor features, your software can detect and avoid incompatibilities.

3.4. Cache Size and Format Information

When the EAX register contains a value of 2, the CPUID instruction loads the EAX, EBX, ECX and EDX registers with descriptors that indicate the processor's cache characteristics. The lower 8 bits of the EAX register (AL) contain a value that identifies the number of times the CPUID has to be executed to obtain a complete image of the processor's caching systems. For example, the Pentium Pro processor returns a value of 1 in the lower 8 bits of the EAX register to indicate that the CPUID instruction need only be executed once (with EAX = 2) to obtain a complete image of the processor configuration.

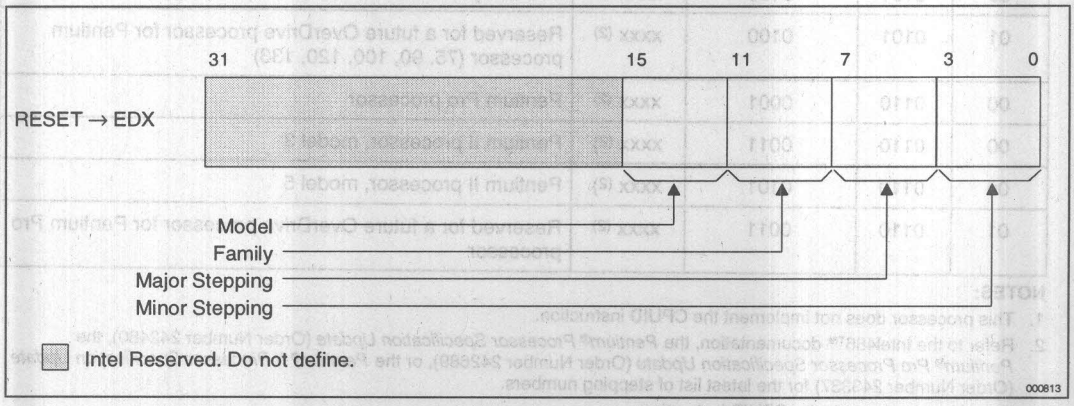


Figure 4. Processor Signature Format on Intel386™ Processors

Table 4. Intel386™ Processor Signatures

Type	Family	Major Stepping	Minor Stepping	Description
0000	0011	0000	xxxx	Intel386™ DX processor
0010	0011	0000	xxxx	Intel386 SX processor
0010	0011	0000	xxxx	Intel386 CX processor
0010	0011	0000	xxxx	Intel386 EX processor
0100	0011	0000 and 0001	xxxx	Intel386 SL processor
0000	0011	0100	xxxx	RapidCAD™ coprocessor

Table 5. Feature Flag Values

Bit	Name	Description when Flag = 1	Comments
0	FPU	Floating-point unit on-chip	The processor contains an FPU that supports the Intel 387 floating-point instruction set.
1	VME	Virtual Mode Extension	The processor supports extensions to virtual-8086 mode.
2	DE	Debugging Extension	The processor supports I/O breakpoints, including the CR4.DE bit for enabling debug extensions and optional trapping of access to the DR4 and DR5 registers.
3	PSE	Page Size Extension	The processor supports 4-Mbyte pages.
4	TSC	Time Stamp Counter	The RDTSC instruction is supported including the CR4.TSD bit for access/privilege control.
5	MSR	Model Specific Registers	Model Specific Registers are implemented with the RDMSR, WRMSR instructions
6	PAE	Physical Address Extension	Physical addresses greater than 32 bits are supported.
7	MCE	Machine Check Exception	Machine Check Exception, Exception 18, and the CR4.MCE enable bit are supported
8	CX8	CMPXCHG8 Instruction Supported	The compare and exchange 8 bytes instruction is supported.
9	APIC	On-chip APIC Hardware Supported (1)	The processor contains a local APIC.
10	MTRR	Reserved	Do not count on their value.
11	SEP	Fast System Call	Indicates whether the processor supports the Fast System Call instructions, SYSENTER and SYSEXIT. NOTE: Refer to Section 3.5 for further information regarding SYSENTER/ SYSEXIT feature and SEP feature bit.
12	MTRR	Memory Type Range Registers	The Processor supports the Memory Type Range Registers specifically the MTRR_CAP register.
13	PGE	Page Global Enable	The global bit in the PDEs and PTEs and the CR4.PGE enable bit are supported.
14	MCA	Machine Check Architecture	The Machine Check Architecture is supported, specifically the MCG_CAP register.

23	MMX Technology	Intel Architecture MMX technology supported	The processor supports the MMX technology instruction set extensions to Intel Architecture.
24	FXSR	Fast floating point save and restore	Indicates whether the processor supports the FXSAVE and FXRSTOR instructions for fast save and restore of the floating point context. Presence of this bit also indicates that CR4.OSFXSR is available for an operating system to indicate that it uses the fast save/restore instructions.
25 – 31		Reserved	Do not count on their value.

NOTE:

1. The processor contains a software-accessible Local APIC.

The remainder of the EAX register, and the EBX, ECX, and EDX registers, contain valid 8 bit descriptors. Table 6 shows that a most significant bit of zero indicates a valid 8-bit descriptor. To decode descriptors, move sequentially from the most significant byte of the register down through the least significant byte of the register. Table 7 lists the current descriptor values and their respective cache characteristics. This list will be extended in the future as necessary.

Table 6. Descriptor Formats

Register MSB	Descriptor Type	Description
1	Reserved	Reserved for future use.
0	8 bit descriptors	Descriptors point to a parameter table to identify cache characteristics. The descriptor is null if it has a 0 value.

Table 7. Descriptor Decode Values

Descriptor Value	Cache Description
00h	Null
01h	Instruction TLB, 4K pages, 4-way set associative, 32 entries
02h	Instruction TLB, 4M pages, fully associative, 2 entries
03h	Data TLB, 4K pages, 4-way set associative, 64 entries
04h	Data TLB, 4M pages, 4-way set associative, 8 entries
06h	Instruction cache, 8K, 4-way set associative, 32 byte line size
08h	16KB instruction cache, 4-way set associative, 32 byte line size
0Ah	Data cache, 8K, 2-way set associative, 32 byte line size
0Ch	16KB data cache, 2-way set associative, 32 byte line size
40h	No L2 cache
41h	Unified cache, 32 byte cache line,4-way set associative, 128K
42h	Unified cache, 32 byte cache line, 4-way set associative, 256K
43h	Unified cache, 32 byte cache line, 4-way set associative, 512K
44h	Unified cache, 32 byte cache line, 4-way set associative, 1M
45h	Unified cache, 32 byte cache line, 4-way set associative, 2M

Table 8. Pentium® Pro Processor, with 256K L2 Cache, CPUID (EAX=2) Example Return Values

	31	23	15	7	0
EAX	03h	02h	01h	01h	
EBX	0	0	0	0	
ECX	0	0	0	0	
EDX	06h	04h	0Ah	42h	

3.5. SYSENTER/SYSEXIT – SEP Features Bit

The presence of this facility is indicated by the SYSENTER Present (SEP) bit 11 of CPUID. An operating system that detects the presence of the SEP bit must also qualify the processor family and model to ensure that the SYSENTER/SYSEXIT instructions are actually present:

```
If (CPUID SEP bit is set) {
If (Family == 6) AND (Model < 3) AND
        (Stepping < 3) {
                THEN
Fast System Call is NOT supported
                }
                ELSE Fast System Call is
        supported
}
```

The Pentium Pro processor (Model = 1) returns a set SEP CPUID feature bit, but should not be used by software.

3.6. Pentium® Pro Processor Output Example

The Pentium Pro processor returns the values shown in Table 8. As the value of AL = 1, it is valid to interpret the remainder of the registers according to Table 7. Table 8 also shows that the MSB of the EAX register is 0. This indicates that the upper 8 bits constitute an 8 bit descriptor. The remaining register values in Table 8 show that the Pentium Pro processor has the following cache characteristics:

- A data TLB that maps 4K pages, is 4 way set associative, and has 64 entries.
- An instruction TLB that maps 4M pages, is fully associative, and has 2 entries.
- An instruction TLB that maps 4K pages, is 4 way set associative, and has 32 entries.
- An instruction cache that is 8K, is 4 way set associative, and has a 32 byte line size.
- A data TLB that maps 4M pages, is 4 way set associative, and has 8 entries.
- A data cache that is 8K, is 2 way set associative, and has a 32 byte line size.
- A unified cache that is 256K, is 4 way set associative, and has a 32 byte line size.

3.7. Pentium® II Processor, Model 3 Output Example

The Pentium II processor, model 3 returns the values shown in Table 9. If the value of AL=1, it is valid to interpret the remainder of the registers according to Table 7. Table 9 also shows the MSB of EAX register is 0. As with the Pentium Pro processor this indicates the upper 8 bits constitute an 8 bit descriptor. The remaining register values in Table 9 shows the Pentium II processor has the following cache characteristics:

- A data TLB that maps 4K pages, is 4 way set associative, and has 64 entries.
- An instruction TLB that maps 4M pages, is fully associative, and has 2 entries.
- An instruction TLB that maps 4K pages, is 4 way set associative, and has 32 entries.
- A data cache that is 16K, is 4 way set associative, and has a 32 byte line size.
- A data TLB that maps 4M pages, is 4 way set associative, and has 8 entries.
- An instruction cache that is 16K, is 4 way set associative, and has a 32 byte line size.
- A unified cache that is 512K, is 4 way set associative, and has a 32 byte line size.

Table 9. Pentium® II Processor, model 3 with 512K L2 Cache, CPUID (EAX=2) Example Return Values

	31	23	15	7	0
EAX	03h	02h	01h	01h	
EBX	0	0	0	0	
ECX	0	0	0	0	
EDX	0Ch	04h	08h	43h	

4.0. USAGE GUIDELINES

This document presents Intel-recommended feature-detection methods. Software should not try to identify features by exploiting programming tricks, undocumented features, or otherwise deviating from the guidelines presented in this application note.

The following guidelines are intended to help programmers maintain the widest range of compatibility for their software.

- Do not depend on the absence of an invalid opcode trap on the CPUID opcode to detect the CPUID instruction. Do not depend on the absence of an invalid opcode trap on the PUSHFD opcode to detect a 32-bit processor. Test the ID flag, as described in Section 2.0. and shown in Section 5.0.
- Do not assume that a given family or model has any specific feature. For example, do not assume the family value 5 (Pentium® processor) means there is a floating-point unit on-chip. Use the feature flags for this determination.
- Do not assume processors with higher family or model numbers have all the features of a processor with a lower family or model number. For example, a processor with a family value of 6 (Pentium Pro processor) may not necessarily have all the features of a processor with a family value of 5.
- Do not assume that the features in the OverDrive® processors are the same as those in the OEM version of the processor. Internal caches and instruction execution might vary.
- Do not use undocumented features of a processor to identify steppings or features. For example, the Intel386™ processor A-step had bit instructions that were withdrawn with B-step. Some software attempted to execute these instructions and depended on the invalid-opcode exception as a signal that it was not running on the A-step part. The software failed to work correctly when the Intel486™ processor used the same opcodes for different instructions. The software should have used the stepping information in the processor signature.
- Test feature flags individually and do not make assumptions about undefined bits. For example, it would be a mistake to test the FPU bit by comparing the feature register to a binary 1 with a compare instruction.
- Do not assume the clock of a given family or model runs at a specific frequency, and do not write clock-dependent code, such as timing loops. For instance, an OverDrive processor could operate at a higher internal frequency and still report the same family and/or model. Instead, use the system's timers to measure elapsed time. For processors that support the TSC (Time Stamp Counter) functionality, system timers can more directly calibrate the processor core block.
- Processor model-specific registers may differ among processors, including in various models of the Pentium processor. Do not use these registers unless identified for the installed processor. This is particularly important for systems upgradeable with an OverDrive processor. Only use Model Specific registers that are defined in the BIOS writers guide for that processor.
- Do not rely on the result of CPUID algorithm when executed in virtual 8086 mode.
- Do not assume any ordering of stepping numbers. They are assigned arbitrarily.

5.0. PROPER IDENTIFICATION SEQUENCE

The cpuid3a.asm program example demonstrates the correct use of the CPUID instruction. (See Example 1.) It also shows how to identify earlier processor generations that do not implement the processor signature or CPUID instruction. (See Figure 5.) This program example contains the following two procedures:

`get_cpu_type` identifies the processor type. Figure 5 illustrates the flow of this procedure.

`get_fpu_type` determines the type of floating-point unit (FPU) or math coprocessor (MCP).

This procedure has been tested with 8086, 80286, Intel386, Intel486, Pentium processor, Pentium processor with MMX technology, OverDrive processor with MMX technology, Pentium Pro processors and Pentium II processors with MMX technology. This program example is written in assembly language and is suitable for inclusion in a run-time library, or as system calls in operating systems.

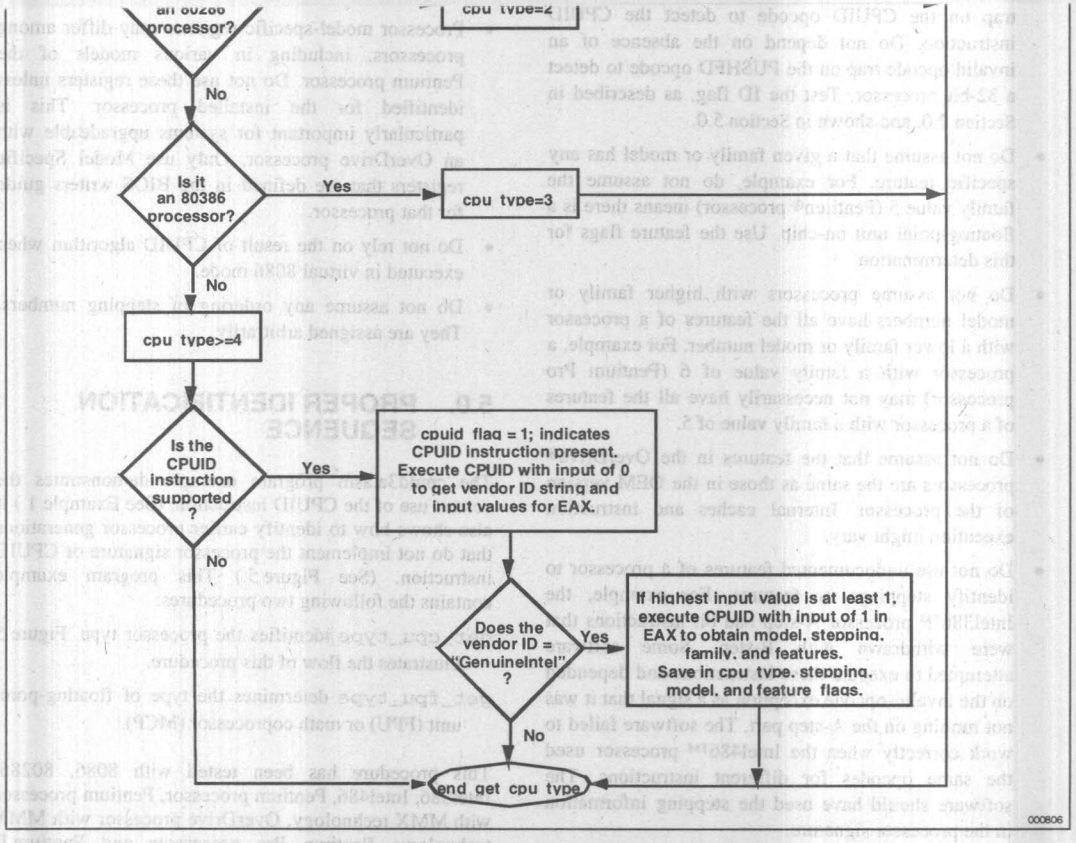


Figure 5. Flow of Processor `get_cpu_type` Procedure

6.0. USAGE PROGRAM EXAMPLES

The cpuid3b.asm or cpuid3.c program examples demonstrate applications that call `get_cpu_type` and `get_fpu_type` procedures and interpret the returned information. This code is shown in Example 2 and Example 3. The results, which are displayed on the monitor, identify the installed processor and features. The cpuid3b.asm example is written in assembly language and demonstrates an application that displays the returned information in the DOS environment. The cpuid3.c example is written in the C language (see Example 2 and Example 3). Figure 6 presents an overview of the relationship between the three program examples.

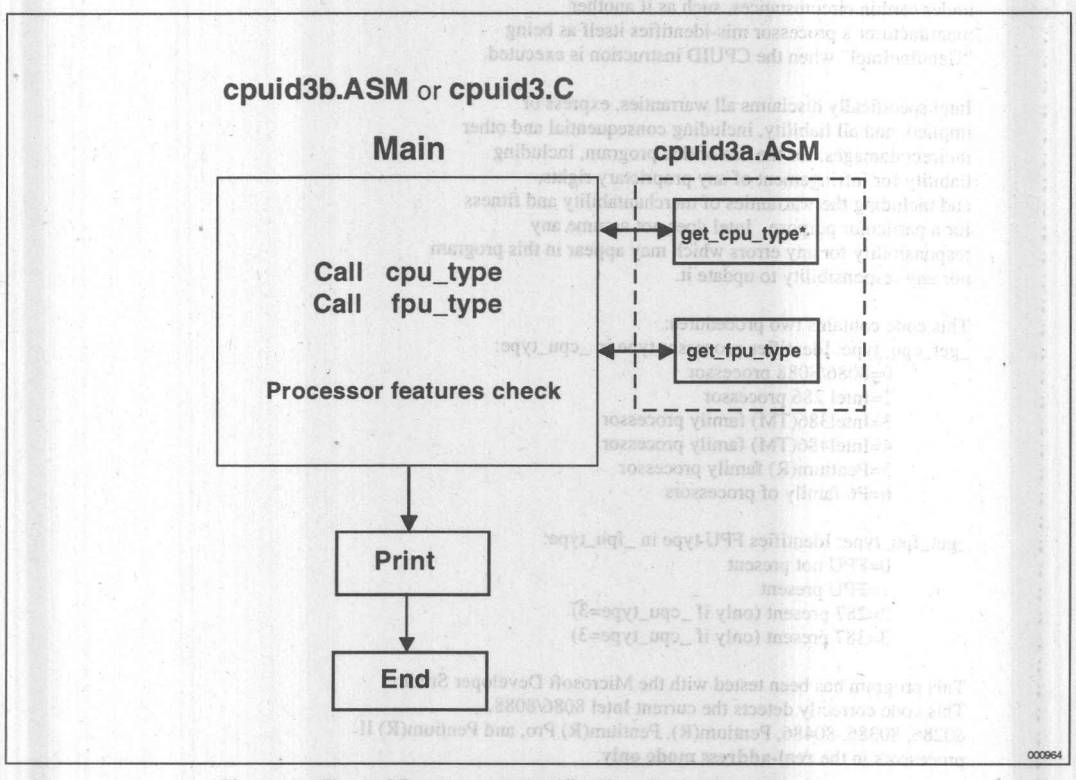


Figure 6. Flow of Processor Identification Extraction Procedure

Example 1. Processor Identification Extraction Procedure

```
;       Filename:       cpuid3a.asm
;       Copyright 1993, 1994, 1995, 1996, 1997 by Intel Corp.
;
;       This program has been developed by Intel Corporation.  Intel
;       has various intellectual property rights which it may assert
;       under certain circumstances, such as if another
;       manufacturer's processor mis-identifies itself as being
;       "GenuineIntel" when the CPUID instruction is executed.
;
;       Intel specifically disclaims all warranties, express or
;       implied, and all liability, including consequential and other
;       indirect damages, for the use of this program, including
;       liability for infringement of any proprietary rights,
;       and including the warranties of merchantability and fitness
;       for a particular purpose.  Intel does not assume any
;       responsibility for any errors which may appear in this program
;       nor any responsibility to update it.
;
;       This code contains two procedures:
;       _get_cpu_type: Identifies processor type in _cpu_type:
;               0=8086/8088 processor
;               2=Intel 286 processor
;               3=Intel386(TM) family processor
;               4=Intel486(TM) family processor
;               5=Pentium(R) family processor
;               6=P6 family of processors
;
;       _get_fpu_type: Identifies FPU type in _fpu_type:
;               0=FPU not present
;               1=FPU present
;               2=287 present (only if _cpu_type=3)
;               3=387 present (only if _cpu_type=3)
;
;       This program has been tested with the Microsoft Developer Studio.
;       This code correctly detects the current Intel 8086/8088,
;       80286, 80386, 80486, Pentium(R), Pentium(R) Pro, and Pentium(R) II
;       processors in the real-address mode only.
;
;       To assemble this code with TASM, add the JUMPS directive.
;       jumps                                   ; Uncomment this line for TASM


        TITLE   cpuid3a
;
;       comment this line for 32-bit segments
;
        DOSSEG
;
;       uncomment the following 2 lines for 32-bit segments
;
;       .386
;       .model  flat
;
```

```
;       comment this line for 32-bit segments
;
        .model  small

CPU_IDMACRO
        db      0fh                             ; Hardcoded CPUID instruction
        db      0a2h
ENDM

        .data
        public  _cpu_type
        public  _fpu_type
    public      _v86_flag
        public  _cpuid_flag
        public  _intel_CPU
        public  _vendor_id
        public  _cpu_signature
        public  _features_ecx
        public  _features_edx
        public  _features_ebx
    public      _sep_flag

        _cpu_type               db      0
        _fpu_type               db      0
        _v86_flag               db      0
        _cpuid_flag             db      0
        _intel_CPU              db      0
        _sep_flag               db      0
        _vendor_id              db      "------------"
        intel_id        db      "GenuineIntel"
        _cpu_signature  dd      0
        _features_ecx   dd      0
        _features_edx   dd      0
        _features_ebx   dd      0
        fp_status               dw      0

        .code
;
;       comment this line for 32-bit segments
;
        .8086
;
;       uncomment this line for 32-bit segments
;
;       .386

;*************************************************************************

        public  _get_cpu_type
_get_cpu_type   proc

;       This procedure determines the type of processor in a system
;       and sets the _cpu_type variable with the appropriate
;       value.  If the CPUID instruction is available, it is used
;       to determine more specific details about the processor.
;       All registers are used by this procedure, none are preserved.
```

```
        mov     cx, ax                  ; save original FLAGS
        and     ax, 0fffh               ; clear bits 12-15 in FLAGS
        push    ax                              ; save new FLAGS value on stack
        popf                            ; replace current FLAGS value
        pushf                           ; get new FLAGS
        pop     ax                      ; store new FLAGS in AX
        and     ax, 0f000h              ; if bits 12-15 are set, then
        cmp     ax, 0f000h              ;   processor is an 8086/8088
        mov     _cpu_type, 0            ; turn on 8086/8088 flag
        jne     check_80286             ; go check for 80286
        push    sp                      ; double check with push sp
        pop     dx                      ; if value pushed was different
        cmp     dx, sp                  ;   means it's really not an 8086
        jne     end_cpu_type            ; jump if processor is 8086/8088
        mov     _cpu_type, 10h          ; indicate unknown processor
        jmp     end_cpu_type

;       Intel 286 processor check
;       Bits 12-15 of the FLAGS register are always clear on the
;       Intel 286 processor in real-address mode.

        .286
check_80286:
        smsw    ax                              ; save machine status word
        and     ax, 1                           ; isolate PE bit of MSW
        mov     _v86_flag, al           ; save PE bit to indicate V86

        or      cx, 0f000h                      ; try to set bits 12-15
        push    cx                              ; save new FLAGS value on stack
        popf                                    ; replace current FLAGS value
        pushf                                   ; get new FLAGS
        pop     ax                              ; store new FLAGS in AX
        and     ax, 0f000h                      ; if bits 12-15 are clear
        mov     _cpu_type, 2            ; processor=80286, turn on 80286 flag
        jz      end_cpu_type            ; jump if processor is 80286

;       Intel386 processor check
;       The AC bit, bit #18, is a new bit introduced in the EFLAGS
;       register on the Intel486 processor to generate alignment
;       faults.
;       This bit cannot be set on the Intel386 processor.

        .386
```

```
;
;       "STOP"
;
;                                               ; it is safe to use 386 instructions
check_80386:
        pushfd                                  ; push original EFLAGS
        pop     eax                                     ; get original EFLAGS
        mov     ecx, eax                        ; save original EFLAGS
        xor     eax, 40000h                             ; flip AC bit in EFLAGS
        push    eax                                     ; save new EFLAGS value on stack
        popfd                                           ; replace current EFLAGS value
        pushfd                                  ; get new EFLAGS
        pop     eax                                     ; store new EFLAGS in EAX
        xor     eax, ecx                        ; can't toggle AC bit, processor=80386
        mov     _cpu_type, 3                    ; turn on 80386 processor flag
        jz      end_cpu_type                    ; jump if 80386 processor

        push    ecx
        popfd                                           ; restore AC bit in EFLAGS first

;       Intel486 processor check
;       Checking for ability to set/clear ID flag (Bit 21) in EFLAGS
;       which indicates the presence of a processor with the CPUID
;       instruction.

        .486
check_80486:
        mov     _cpu_type, 4            ; turn on 80486 processor flag
        mov     eax, ecx                        ; get original EFLAGS
        xor     eax, 200000h                    ; flip ID bit in EFLAGS
        push    eax                                     ; save new EFLAGS value on stack
        popfd                                           ; replace current EFLAGS value
        pushfd                                  ; get new EFLAGS
        pop     eax                                     ; store new EFLAGS in EAX
        xor     eax, ecx                        ; can't toggle ID bit,
        je      end_cpu_type                    ; processor=80486

;       Execute CPUID instruction to not determine vendor, family,
;       model, stepping and features.  For the purpose of this
;       code, only the initial set of CPUID information is saved.

        mov     _cpuid_flag, 1                  ; flag indicating use of CPUID inst.
        push    ebx                                     ; save registers
        push    esi
        push    edi
        mov     eax, 0                          ; set up for CPUID instruction
        CPU_ID                                  ; get and save vendor ID

        mov     dword ptr _vendor_id, ebx
        mov     dword ptr _vendor_id[+4], edx
        mov     dword ptr _vendor_id[+8], ecx

        cmp     dword ptr intel_id, ebx
        jne     end_cpuid_type
        cmp     dword ptr intel_id[+4], edx
        jne     end_cpuid_type
```

```
        cmp     dword ptr intel_id[+8], ecx
        jne     end_cpuid_type                  ; if not equal, not an Intel processor

        mov     _intel_CPU, 1                   ; indicate an Intel processor
        cmp     eax, 1                          ; make sure 1 is valid input for CPUID
        jl      end_cpuid_type                  ; if not, jump to end
        mov     eax, 1
        CPU_ID                                  ; get family/model/stepping/features
        mov     _cpu_signature, eax
        mov     _features_ebx, ebx
        mov     _features_edx, edx
        mov     _features_ecx, ecx

        shr     eax, 8                          ; isolate family
        and     eax, 0fh
        mov     _cpu_type, al                   ; set _cpu_type with family

end_cpuid_type:
        pop     edi                             ; restore registers
        pop     esi
        pop     ebx
;
;       comment this line for 32-bit segments
;
        .8086
end_cpu_type:
        ret
_get_cpu_type           endp

;*************************************************************************

        public  _get_fpu_type
_get_fpu_type   proc

;       This procedure determines the type of FPU in a system
;       and sets the _fpu_type variable with the appropriate value.
;       All registers are used by this procedure, none are preserved.

;       Coprocessor check
;       The algorithm is to determine whether the floating-point
;       status and control words are present.  If not, no
;       coprocessor exists.  If the status and control words can
;       be saved, the correct coprocessor is then determined
;       depending on the processor type.  The Intel386 processor can
;       work with either an Intel287 NDP or an Intel387 NDP.
;       The infinity of the coprocessor must be checked to determine
;       the correct coprocessor type.

        fninit                          ; reset FP status word
        mov     fp_status, 5a5ah        ; initialize temp word to non-zero
        fnstsw  fp_status               ; save FP status word
        mov     ax, fp_status           ; check FP status word
        cmp     al, 0                           ; was correct status written
        mov     _fpu_type, 0            ; no FPU present
        jne     end_fpu_type
```

```
check_control_word:
        fnstcw  fp_status               ; save FP control word
        mov     ax, fp_status           ; check FP control word
        and     ax, 103fh                       ; selected parts to examine
        cmp     ax, 3fh                 ; was control word correct
        mov     _fpu_type, 0
        jne     end_fpu_type            ; incorrect control word, no FPU
        mov     _fpu_type, 1

;       80287/80387 check for the Intel386 processor

check_infinity:
        cmp     _cpu_type, 3
        jne     end_fpu_type
        fld1                                    ; must use default control from FNINIT
        fldz                                    ; form infinity
        fdiv                                    ; 8087/Intel287 NDP say +inf = -inf
        fld     st                              ; form negative infinity
        fchs                                    ; Intel387 NDP says +inf <> -inf
        fcompp                          ; see if they are the same
        fstsw   fp_status                       ; look at status from FCOMPP
        mov     ax, fp_status
        mov     _fpu_type, 2            ; store Intel287 NDP for FPU type
        sahf                                    ; see if infinities matched
        jz      end_fpu_type            ; jump if 8087 or Intel287 is present
        mov     _fpu_type, 3            ; store Intel387 NDP for FPU type
end_fpu_type:
        ret
_get_fpu_type           endp
        end
```

Example 2. Processor Identification Procedure in Assembly Language

```
;       Filename:  cpuid3b.asm
;       Copyright 1993, 1994, 1995, 1996, 1997 by Intel Corp.
;
;       This program has been developed by Intel Corporation.  Intel
;       has various intellectual property rights which it may assert
;       under certain circumstances, such as if another
;       manufacturer's processor mis-identifies itself as being
;       "GenuineIntel" when the CPUID instruction is executed.
;
;       Intel specifically disclaims all warranties, express or
;       implied, and all liability, including consequential and
;       other indirect damages, for the use of this program,
;       including liability for infringement of any proprietary
;       rights, and including the warranties of merchantability and
;       fitness for a particular purpose.  Intel does not assume any
;       responsibility for any errors which may appear in this
;       program nor any responsibility to update it.
;
;       This program contains three parts:
;       Part 1:  Identifies processor type in the variable
;                       _cpu_type:
;
```

```
;       jumps                                   ; Uncomment this line for TASM
;
        TITLE   cpuid3b
;
;       comment this line for 32-bite segments
;
        DOSSEG
;
;       uncomment the following 2 lines for 32-bit segments
;
;       .386
;       .model  flat
;
;       comment the following line for 32-bit segments
;
        .model  small
        .stack  100h

        .data
        extrn           _cpu_type:              byte
        extrn           _fpu_type:              byte
        extrn           _cpuid_flag:    byte
        extrn           _intel_CPU:     byte
        extrn           _vendor_id:     byte
    extrn               _sep_flag:              byte
        extrn           _cpu_signature: dword
        extrn           _features_ecx:  dword
        extrn           _features_edx:  dword
        extrn           _features_ebx:  dword

;       The purpose of this code is to identify the processor and
;       coprocessor that is currently in the system.  The program
;       first determines the processor type.  Then it determines
;       whether a coprocessor exists in the system.  If a
;       coprocessor or integrated coprocessor exists, the program
;       identifies the coprocessor type.  The program then prints
;       the processor and floating point processors present and type.

        .code
;   comment this line for 32-bit segments
        .8086
start:
;   comment the next three lines for 32-bit segments
```

```
        mov     ax, @data
        mov     ds, ax                          ; set segment register
        mov     es, ax                          ; set segment register
        and     sp, not 3                       ; align stack to avoid AC fault
        call    _get_cpu_type                   ; determine processor type
        call    _get_fpu_type
        call    print
        mov     ax, 4c00h                       ; terminate program
        int     21h
;*************************************************************************

        extrn   _get_cpu_type: proc

;*************************************************************************

        extrn   _get_fpu_type: proc

;*************************************************************************

FPU_FLAG            equ 0001h
VME_FLAG            equ 0002h
DE_FLAG             equ 0004h
PSE_FLAG            equ 0008h
TSC_FLAG            equ 0010h
MSR_FLAG            equ 0020h
PAE_FLAG            equ 0040h
MCE_FLAG            equ 0080h
CX8_FLAG            equ 0100h
APIC_FLAG           equ 0200h
SEP_FLAG            equ 0800h
MTRR_FLAG           equ 1000h
PGE_FLAG            equ 2000h
MCA_FLAG            equ 4000h
CMOV_FLAG           equ 8000h
PAT_FLAG            equ 10000h
MMX_FLAG            equ 800000h
FXSR_FLAG           equ 1000000h

        .data
id_msg          db      "This system has a$"
cp_error        db      "n unknown processor$"
cp_8086                 db      "n 8086/8088 processor$"
cp_286          db      "n 80286 processor$"
cp_386          db      "n 80386 processor$"

cp_486          db      "n 80486DX, 80486DX2 processor or"
                db      " 80487SX math coprocessor$"
cp_486sx                db      "n 80486SX processor$"

fp_8087         db      " and an 8087 math coprocessor$"
fp_287          db      " and an 80287 math coprocessor$"
fp_387          db      " and an 80387 math coprocessor$"

intel486_msg    db      " Genuine Intel486(TM) processor$"
intel486dx_msg  db      " Genuine Intel486(TM) DX processor$"
```

```
intel486sx_msg  db      " Genuine Intel486(TM) SX processor$"
inteldx2_msg    db      " Genuine IntelDX2(TM) processor$"
intelsx2_msg    db      " Genuine IntelSX2(TM) processor$"
inteldx4_msg    db      " Genuine IntelDX4(TM) processor$"
inteldx2wb_msg db       " Genuine Write-Back Enhanced"
                        db      " IntelDX2(TM) processor$"
pentium_msg             db      " Genuine Intel Pentium(R) processor$"
pentiumpro_msg db       " Genuine Intel Pentium(R) Pro processor$"
pentiumiimodel3_msg     db      " Genuine Intel Pentium(R) II processor, model 3$"
pentiumiimodel5_msg     db      " Genuine Intel Pentium(R) II processor, model 5$"
unknown_msg             db      "n unknown Genuine Intel processor$"

; The following 16 entries must stay intact as an array
intel_486_0             dw      offset intel486dx_msg
intel_486_1             dw      offset intel486dx_msg
intel_486_2             dw      offset intel486sx_msg
intel_486_3             dw      offset inteldx2_msg
intel_486_4             dw      offset intel486_msg
intel_486_5             dw      offset intelsx2_msg
intel_486_6             dw      offset intel486_msg
intel_486_7             dw      offset inteldx2wb_msg
intel_486_8             dw      offset inteldx4_msg
intel_486_9             dw      offset intel486_msg
intel_486_a             dw      offset intel486_msg
intel_486_b             dw      offset intel486_msg
intel_486_c             dw      offset intel486_msg
intel_486_d             dw      offset intel486_msg
intel_486_e             dw      offset intel486_msg
intel_486_f             dw      offset intel486_msg
;
;   comment the above entries for the array & uncomment the entries below for
;   for 32-bit segments
;
;intel_486_0            dd      offset intel486dx_msg
;intel_486_1            dd      offset intel486dx_msg
;intel_486_2            dd      offset intel486sx_msg
;intel_486_3            dd      offset inteldx2_msg
;intel_486_4            dd      offset intel486_msg
;intel_486_5            dd      offset intelsx2_msg
;intel_486_6            dd      offset intel486_msg
;intel_486_7            dd      offset inteldx2wb_msg
;intel_486_8            dd      offset inteldx4_msg
;intel_486_9            dd      offset intel486_msg
;intel_486_a            dd      offset intel486_msg
;intel_486_b            dd      offset intel486_msg
;intel_486_c            dd      offset intel486_msg
;intel_486_d            dd      offset intel486_msg
;intel_486_e            dd      offset intel486_msg
;intel_486_f            dd      offset intel486_msg

; end of array

family_msg              db      13,10,"Processor Family:  $"
model_msg               db      13,10,"Model:           $"
stepping_msg    db      13,10,"Stepping:        "
cr_lf                   db      13,10,"$"
```

```
turbo_msg       db      13,10,"The processor is an OverDrive(R)"
                db      " upgrade processor$"
dp_msg      db  13,10,"The processor is the upgrade"
                db      " processor in a dual processor system$"
fpu_msg         db      13,10,"The processor contains an on-chip"
                db      " FPU$"
vme_msg         db      13,10,"The processor supports Virtual"
                db      " Mode Extensions$"
de_msg      db  13,10,"The processor supports Debugging"
                db      " Extensions$"
pse_msg         db      13,10,"The processor supports Page Size"
                db      " Extensions$"
tsc_msg     db  13,10,"The processor supports Time Stamp"
                db      " Counter$"
msr_msg         db      13,10,"The processor supports Model"
                db      " Specific Registers$"
pae_msg         db      13,10,"The processor supports Physical"
                db      " Address Extensions$"
mce_msg         db      13,10,"The processor supports Machine"
                db      " Check Exceptions$"
cx8_msg         db      13,10,"The processor supports the"
                db      " CMPXCHG8B instruction$"
apic_msg        db      13,10,"The processor contains an on-chip"
                db      " APIC$"
sep_msg         db  13,10,"The processor supports Fast System"
                db      " Call$"
no_sep_msg      db      13,10,"The processor does not support Fast"
                db      " System Call$"
mtrr_msg        db      13,10,"The processor supports Memory Type"
                db      " Range Registers$"
pge_msg         db      13,10,"The processor supports Page Global"
                db      " Enable$"
mca_msg         db      13,10,"The processor supports Machine"
                db      " Check Architecture$"
cmov_msg        db      13,10,"The processor supports Conditional"
                db      " Move Instruction$"
pat_msg         db      13,10,"The processor supports Page  Attribute"
                db      " Table$"
mmx_msg         db      13,10,"The processor supports Intel Architecture"
                db      " MMX(TM) Technology$"
fxsr_msg        db      13,10,"The processor supports Fast floating point"
                db      "save and restore$"

not_intel       db      "t least an 80486 processor."
                db      13,10,"It does not contain a Genuine"
                db      "Intel part and as a result,"
                db      "the",13,10,"CPUID"
                db      " detection information cannot be"
                db      "determined at this time.$"

ASC_MSG     MACRO       msg
        LOCAL ascii_done                        ; local label
        add     al, 30h
        cmp     al, 39h                         ; is it 0-9?
        jle     ascii_done
        add     al, 07h
```

```
ascii_done:
        mov     byte ptr msg[20], al
        mov     dx, offset msg
        mov     ah, 9h
        int     21h
ENDM

        .code
;
;       comment the following line for 32-bit segments
;
        .8086
;
;   uncomment the following line for 32-bit segments
;
;       .386
;
print   proc

;       This procedure prints the appropriate cpuid string and
;       numeric processor presence status.  If the CPUID instruction
;       was used, this procedure prints out the CPUID info.
;       All registers are used by this procedure, none are
;       preserved.
;
;       In the balance of the assembly code there are lines that are required for
;       tools that support 32-bit segments only.  If problems occur during the
;       build process, try uncommenting the lines that are near duplicates of the
;       lines following them.  These will be the necessary changes to get code for
;       32-bit segments.

;       mov     edx, offset id_msg
        mov     dx, offset id_msg           ; print initial message
        mov     ah, 9h
        int     21h

        cmp     _cpuid_flag, 1              ; if set to 1, processor
                                            ;   supports CPUID instruction
        je      print_cpuid_data            ; print detailed CPUID info

print_86:
        cmp     _cpu_type, 0
        jne     print_286
        mov     dx, offset cp_8086
        mov     ah, 9h
        int     21h
        cmp     _fpu_type, 0
        je      end_print
;       mov     edx, offset fp_8087
        mov     dx, offset fp_8087
        mov     ah, 9h
        int     21h
        jmp     end_print

print_286:
        cmp     _cpu_type, 2
```

```
        jne     print_386
;       mov     edx, offset cp_286
        mov     dx, offset cp_286
        mov     ah, 9h
        int     21h
        cmp     _fpu_type, 0
        je      end_print

print_287:
;       mov edx, offset fp_287
        mov     dx, offset fp_287
        mov     ah, 9h
        int     21h
        jmp     end_print

print_386:
        cmp     _cpu_type, 3
        jne     print_486
;       mov     edx, offset cp_386
        mov     dx, offset cp_386
        mov     ah, 9h
        int     21h
        cmp     _fpu_type, 0
        je      end_print
        cmp     _fpu_type, 2
        je      print_287
;       mov     edx, offset fp_387
        mov     dx, offset fp_387
        mov     ah, 9h
        int     21h
        jmp     end_print

print_486:
        cmp     _cpu_type, 4
        jne     print_unknown           ; Intel processors will have
;       mov     edx, offset cp_486sx
        mov     dx, offset cp_486sx     ; CPUID instruction
        cmp     _fpu_type, 0
        je      print_486sx
;       mov     edx, offset cp_486
        mov     dx, offset cp_486

print_486sx:
        mov     ah, 9h
        int     21h
        jmp     end_print

print_unknown:
;       mov     edx, offset cp_error
        mov     dx, offset cp_error
        jmp     print_486sx

print_cpuid_data:
        .486
        cmp     _intel_CPU, 1           ; check for genuine Intel
        jne     not_GenuineIntel        ;  processor
```

```
print_486_type:
        cmp     _cpu_type, 4                    ; if 4, print 80486 processor
        jne     print_pentium_type
;       mov     eax, dword ptr _cpu_signature
        mov     ax, word ptr _cpu_signature
        shr     ax, 4
        and     eax, 0fh                        ; isolate model
;       mov     edx, intel_486_0[eax*2]
        mov     dx, intel_486_0[eax*2]
        jmp     print_common

print_pentium_type:
        cmp     _cpu_type, 5                    ; if 5, print Pentium processor
        jne     print_pentiumpro_type
;       mov     edx,    offset pentium_msg
        mov     dx, offset pentium_msg
        jmp     print_common

print_pentiumpro_type:
        cmp     _cpu_type, 6                    ; if 6 & model 1, print Pentium
                                                        ; Pro processor
        jne     print_unknown_type
;       mov     eax, dword ptr _cpu_signature
    mov ax, word ptr _cpu_signature
        shr     ax, 4
        and  eax, 0fh                           ; isolate model
    cmp  eax, 3
    jge  print_pentiumiimodel3_type
    cmp eax, 1
        jne     print_unknown_type              ; incorrect model number = 2
        mov     _sep_flag, 0            ; does not support Fast System
                                                        ; Call
;       mov     edx, offset pentiumpro_msg
        mov     dx, offset pentiumpro_msg
        jmp     print_common

print_pentiumiimodel3_type:
        cmp     eax, 3                          ; if 6 & model 3, print Pentium
                                                        ; II processor, model 3
        jne     print_pentiumiimodel5_type
;       mov     eax, dword ptr _cpu_signature
        mov     ax, word ptr _cpu_signature
        and     al, 0fh                         ; isolate stepping
    cmp al, 3
        jl      no_sep
    mov _sep_flag, 1
;       mov     edx, offset pentiumiimodel3_msg
        mov     dx, offset pentiumiimodel3_msg
        jmp     print_common

no_sep:
        mov     _sep_flag, 0                    ; stepping does not support
                                                        ; Fast System Call
;       mov     edx, offset pentiumiimodel3_msg
        mov     dx, offset pentiumiimodel3_msg
```

```
        jmp     print_common

print_pentiumiimodel5_type:
        cmp     eax, 5                  ; if 6 & model 5, print Pentium
                                        ; II processor, model 5
        jne     print_unknown_type
        mov     _sep_flag, 1            ; Pentium II processor, model 5
                                        ; supports sep flag
;       mov     edx, offset pentiumiimodel5_msg
        mov     dx, offset pentiumiimodel5_msg
        jmp     print_common

print_unknown_type:
;       mov     edx, offset unknown_msg
        mov     dx, offset unknown_msg  ; if neither, print unknown

print_common:
        mov     ah, 9h
        int     21h

; print family, model, and stepping

print_family:
        mov     al, _cpu_type
        ASC_MSG     family_msg              ; print family msg

print_model:
;       mov     eax, dword ptr _cpu_signature
        mov     ax, word ptr _cpu_signature
        shr     ax, 4
        and     al, 0fh
        ASC_MSG     model_msg               ; print model msg

print_stepping:
;       mov     eax, dword ptr _cpu_signature
        mov     ax, word ptr _cpu_signature
        and     al, 0fh
        ASC_MSG     stepping_msg            ; print stepping msg

print_upgrade:
;       mov     eax, dword ptr _cpu_signature
        mov     ax, word ptr _cpu_signature
        test    ax, 1000h                   ; check for turbo upgrade
        jz      check_dp
;       mov     edx, offset turbo_msg
        mov     dx, offset turbo_msg
        mov     ah, 9h
        int     21h
        jmp     print_features

check_dp:
        test    ax, 2000h                   ; check for dual processor
        jz      print_features
;       mov     edx, offset dp_msg
        mov     dx, offset dp_msg
        mov     ah, 9h
```

```
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, VME_FLAG                    ; check for VME
        jz      check_DE
;       mov     eax, offset vme_msg
        mov     dx, offset vme_msg
        mov     ah, 9h
        int     21h

check_DE:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, DE_FLAG                             ; check for DE
        jz      check_PSE
;       mov     edx, offset de_msg
        mov     dx, offset de_msg
        mov     ah, 9h
        int     21h

check_PSE:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, PSE_FLAG                    ; check for PSE
        jz      check_TSC
;       mov     edx, offset pse_msg
        mov     dx, offset pse_msg
        mov     ah, 9h
        int     21h

check_TSC:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, TSC_FLAG                    ; check for TSC
        jz      check_MSR
;       mov     edx, offset tsc_msg
        mov     dx, offset tsc_msg
        mov     ah, 9h
        int     21h

check_MSR:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, MSR_FLAG                    ; check for MSR
```

```
        jz      check_PAE
;       mov     edx, offset msr_msg
        mov     dx, offset msr_msg
        mov     ah, 9h
        int     21h

check_PAE:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, PAE_FLAG                    ; check for PAE
        jz      check_MCE
;       mov     edx, offset pae_msg
        mov     dx, offset pae_msg
        mov     ah, 9h
        int     21h

check_MCE:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, MCE_FLAG                    ; check for MCE
        jz      check_CX8
;       mov     edx, offset mce_msg
        mov     dx, offset mce_msg
        mov     ah, 9h
        int     21h

check_CX8:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, CX8_FLAG                    ; check for CMPXCHG8B
        jz      check_APIC
;       mov     edx, offset cx8_msg
        mov     dx, offset cx8_msg
        mov     ah, 9h
        int     21h

check_APIC:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, APIC_FLAG                   ; check for APIC
        jz      check_SEP
;       mov     edx, offset apic_msg
        mov     dx, offset apic_msg
        mov     ah, 9h
        int     21h

check_-SEP:
        cmp     _sep_flag, 1
        jne     print_no_sep
;       mov     edx, offset sep_msg
        mov     dx, offset sep_msg
        mov     ah, 9h
        int     21h
        jmp     check_MTRR

print_no_sep:
```

```
;       mov     edx, offset _no_sep_msg
        mov     dx, offset no_sep_msg
        mov     ah, 9h
        int     21h

check_MTRR:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, MTRR_FLAG                   ; check for MTRR
        jz      check_PGE
;       mov     edx, offset mtrr_msg
        mov     dx, offset mtrr_msg
        mov     ah, 9h
        int     21h

check_PGE:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, PGE_FLAG                ; check for PGE
        jz      check_MCA
;       mov     edx, offset pge_msg
        mov     dx, offset pge_msg
        mov     ah, 9h
        int     21h

check_MCA:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, MCA_FLAG                ; check for MCA
        jz      check_CMOV
;       mov     edx, offset mca_msg
        mov     dx, offset mca_msg
        mov     ah, 9h
        int     21h

check_CMOV:
;       mov     eax, dword ptr _features_edx
        mov     ax, word ptr _features_edx
        and     ax, CMOV_FLAG                   ; check for CMOV
        jz      check_PAT
;       mov     edx, offset cmov_msg
        mov     dx, offset cmov_msg
        mov     ah, 9h
        int     21h

check_PAT:
;       mov     eax, dword ptr__features_edx
        mov     eax, word ptr__features_edx
        and     eax, PAT_FLAG
        jz      check_mmx
;       mov     edx, offset pat_msg
        mov     dx, offset pat_msg
        mov     ah, 9h
        int     21h

Check_MMX:
```

```
;       mov     eax, dword ptr _features_edx
        mov     eax, word ptr _features_edx
        and     eax, MMX_FLAG                   ; check for MMX technology
        jz      check_fxsr
;       mov     edx, offset mmx_msg
        mov     dx, offset mmx_msg
        mov     ah, 9h
        int     21h

check_FXSR:
;       mov     eax, dword ptr _features_edx
        mov     eax, word ptr _features_edx
        and     eax, FXSR_FLAG                  ; check for FXSR
        jz      end_print
;       mov     edx, offset fxsr_msg
        mov     dx, offset fxsr_msg
        mov     ah, 9h
        int     21h

        jmp     end_print

not_GenuineIntel:
;       mov     edx, offset not_intel
        mov     dx, offset not_intel
        mov     ah, 9h
        int     21h

end_print:
;       mov     edx, offset cr_lf
        mov     dx, offset cr_lf
        mov     ah, 9h
        int     21h
        ret
print   endp

        end     start
```

```
/* damages, for the use of this program, including liability for     */
/* infringement of any proprietary rights, and including the         */
/* warranties of merchantability and fitness for a particular        */
/* purpose.  Intel does not assume any responsibility for any        */
/* errors which may appear in this program nor any responsibility    */
/* to update it.                                                     */
/*                                                                   */
/*                                                                   */
/* This program contains three parts:                                */
/* Part 1: Identifies CPU type in the variable _cpu_type:            */
/*                                                                   */
/* Part 2: Identifies FPU type in the variable _fpu_type:            */
/*                                                                   */
/* Part 3: Prints out the appropriate message.                       */
/*                                                                   */
/* This program has been tested with the Microsoft Developer Studio. */
/* If this code is compiled with no options specified and linked     */
/* with the cpuid3a module, it correctly identifies the current      */
/* Intel 8086/8088, 80286, 80386, 80486, Pentium(R), Pentium(R) Pro  */
/* processors and Pentium(R) II processors in the real-address mode. */

#define FPU_FLAG            0x0001
#define VME_FLAG            0x0002
#define DE_FLAG             0x0004
#define PSE_FLAG            0x0008
#define TSC_FLAG            0x0010
#define MSR_FLAG            0x0020
#define PAE_FLAG            0x0040
#define MCE_FLAG            0x0080
#define CX8_FLAG            0x0100
#define APIC_FLAG           0x0200
#define SEP_FLAG            0x0800
#define MTRR_FLAG           0x1000
#define PGE_FLAG            0x2000
#define MCA_FLAG            0x4000
#define CMOV_FLAG           0x8000
#define PAT_FLAG            0x10000
#define MMX_FLAG            0x800000
#define FXSR_FLAG           0x1000000

extern char cpu_type;
extern char fpu_type;
extern char cpuid_flag;
```

```
extern char intel_CPU;
extern char vendor_id[12];
extern long cpu_signature;
extern long features_ecx;
extern long features_edx;
extern long features_ebx;

main() {
   get_cpu_type();
   get_fpu_type();
   print();
}

print() {
   printf("This system has a");
   if (cpuid_flag == 0) {
         switch (cpu_type) {
         case 0:
            printf("n 8086/8088 processor");
            if (fpu_type) printf(" and an 8087 math coprocessor");
            break;
         case 2:
            printf("n 80286 processor");
            if (fpu_type) printf(" and an 80287 math coprocessor");
            break;
         case 3:
            printf("n 80386 processor");
            if (fpu_type == 2)
                  printf(" and an 80287 math coprocessor");
            else if (fpu_type)
                  printf(" and an 80387 math coprocessor");
            break;
         case 4:
            if (fpu_type) printf("n 80486DX, 80486DX2 processor or \
80487SX math coprocessor");
            else printf("n 80486SX processor");
            break;
         default:
            printf("n unknown processor");
         }
   } else {
         /* using cpuid instruction */
         if (intel_CPU) {
            if (cpu_type == 4) {
                  switch ((cpu_signature>>4)&0xf) {
                  case  0:
                  case  1:
                     printf(" Genuine Intel486(TM) DX processor");
                     break;
                  case  2:
                     printf(" Genuine Intel486(TM) SX processor");
                     break;
                  case  3:
                     printf(" Genuine IntelDX2(TM) processor");
                     break;
                  case  4:
```

```
                    printf(" Genuine Intel486(TM) processor");
                    break;
                case 5:
                    printf(" Genuine IntelSX2(TM) processor");
                    break;
                case 7:
                    printf(" Genuine Write-Back Enhanced \
IntelDX2(TM) processor");
                    break;
                case 8:
                    printf(" Genuine IntelDX4(TM) processor");
                    break;
                default:
                    printf(" Genuine Intel486(TM) processor");
                }
        } else if (cpu_type == 5)
                printf(" Genuine Intel Pentium(R) processor");
        else if ((cpu_type == 6) && (((cpu_signature >> 4) & 0xf) == 1))
                printf(" Genuine Intel Pentium(R) Pro processor");
        else if ((cpu_type == 6) && (((cpu_signature >> 4) & 0xf) == 3))
                printf(" Genuine Intel Pentium(R) II processor, model 3");
        else if ((cpu_type == 6) && (((cpu_signature >> 4) & 0xf) == 5))
                printf(" Genuine Intel Pentium(R) II processor, model 5");
        else
                printf("n unknown Genuine Intel processor");
        printf("\nProcessor Family: %X", cpu_type);
        printf("\nModel:          %X", (cpu_signature>>4)&0xf);
        printf("\nStepping:       %X\n", cpu_signature&0xf);
        if (cpu_signature & 0x1000)
                printf("\nThe processor is an OverDrive(R)upgrade \
processor");
        else if (cpu_signature & 0x2000)
                printf("\nThe processor is the upgrade processor \
in a dual processor system");
        if (features_edx & FPU_FLAG)
                printf("\nThe processor contains an on-chip FPU");
        if (features_edx & VME_FLAG)
                printf("\nThe processor supports Virtual Mode \
Extensions");
                if (features_edx & DE_FLAG)
                printf("\nThe processor supports the Debugging\
Extensions");
        if (features_edx & PSE_FLAG)
                printf("\nThe processor supports Page Size \
Extensions");
        if (features_edx & TSC_FLAG)
                printf("\nThe processor supports Time Stamp \
Counter");
        if (features_edx & MSR_FLAG)
                printf("\nThe processor supports Model Specific \
Registers");
        if (features_edx & PAE_FLAG)
                printf("\nThe processor supports Physical Address \
Extension");
        if (features_edx & MCE_FLAG)
                printf("\nThe processor supports Machine Check \
```

```
Exceptions");
            if (features_edx & CX8_FLAG)
                printf("\nThe processor supports the CMPXCHG8B \
instruction");
            if (features_edx & APIC_FLAG)
                printf("\nThe processor contains an on-chip APIC");
        if (features_edx & SEP_FLAG) {
            if ((cpu_type == 6) && (((cpu_signature >> 4) &0xf) < 3)
          && ((cpu_signature & 0xf) < 3))
            printf("\nThe processor does not support the Fast \
System Call");
                else
                    printf("\nThe processor supports the Fast System \
Call");
            }
            if (features_edx & MTRR_FLAG)
                printf("\nThe processor supports the Memory Type \
Range Registers");
            if (features_edx & PGE_FLAG)
                printf("\nThe processor supports Page Global Enable");
            if (features_edx & MCA_FLAG)
              printf("\nThe processor supports the Machine Check \
Architecture");
            if (features_edx & CMOV_FLAG)
                printf("\nThe processor supports the Conditional \
Move Instruction");
            if (features_edx & PAT_FLAG)
                printf("\nThe processor supports the Page \
Attribute Table");
            if (features_edx & MMX_FLAG)
                printf("\nThe processor supports Intel Architecture \
MMX technology");
            if (features_edx & FXSR_FLAG)
                printf("\nThe processor supports the Fast floating \
point save and restore");
          } else {
            printf("t least an 80486 processor.\nIt does not \
contain a Genuine Intel part and as a result, the\nCPUID detection \
information cannot be determined at this time.");
          }
    }
    printf("\n");
}
```

Start Body Text Here--Delete This Line.

intel®

MultiProcessor Specification

Version 1.4

May 1997

Revision History

Revision	Revision History	Date
	Pre-release Version 1.0. Formerly called "PC+MP Specification"	10/27/93
-001	Version 1.1. Resolves conflicts with MCA-based systems. The following changes have been made: 1. Two MP feature information bytes were moved from the BIOS System Configuration Table to the RESERVED area of the MP Floating Pointer. Structure. 2. If the MP Floating Pointer Structure is present, it indicates that the system is MP-compliant, in accordance with this specification. (Previously, this was indicated by bit 0 of MP Feature Information Byte 1.) 3. One more hardware default system configuration was added for MCA+PCI with the integrated APIC.	4/11/94
-002	Minor technical corrections.	6/1/94
-003	Added Appendix D: Multiple I/O APIC Multiple PCI Bus Systems.	9/1/94
-004	Version 1.4. Added extended configuration table to improve support for multiple PCI bus configurations and improve future expandability. Made clarifications to Appendix B.	7/1/95
-005	Added Appendix E: Errata. Includes information for hierarchical PCI bus.	08/15/96
-006	Appendix E Update. Included Byte 2, Bit 6 information to MP Floating Point Structure section (4.1).	05/12/97

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Chapter 2: Pentium® Processors

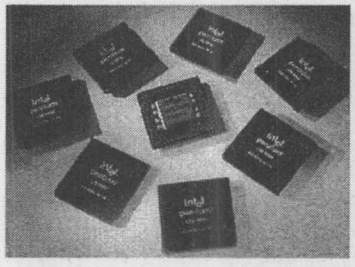
PENTIUM® PROCESSOR

Max. Operating Frequency	75 MHz	90 MHz	100 MHz	120 MHz	133 MHz	150 MHz	166 MHz	200 MHz
iCOMP® Index 2.0 Rating	67	81	90	100	111	114	127	142

Note: Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

- **Compatible with Large Software Base**
  - **— MS-DOS*, Windows*, OS/2*, UNIX***
- **32-Bit CPU with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **— Two Pipelined Integer Units Are Capable of 2 Instructions/Clock**
  - **— Pipe-lined Floating Point Unit**
- **Separate Code and Data Caches**
  - **— 8-Kbyte Code, 8-Kbyte Write Back Data**
  - **— MESI Cache Protocol**
- **Advanced Design Features**
  - **— Branch Prediction**
  - **— Virtual Mode Extensions**
- **3.3V BiCMOS Silicon Technology**
- **4-Mbyte Pages for Increased TLB Hit Rate**
- **IEEE 1149.1 Boundary Scan**
- **Dual Processing Configuration**
- **Functional Redundancy Checking Support**
- **Internal Error Detection Features**
- **Multi-Processor Support**
  - **— Multiprocessor Instructions**
  - **— Support for Second Level Cache**
- **On-Chip Local APIC Controller**
  - **— MP Interrupt Management**
  - **— 8259 Compatible**
- **Upgradable with a Pentium® OverDrive® Processor**
- **Power Management Features**
  - **— System Management Mode**
  - **— Clock Control**
- **Fractional Bus Operation**
  - **— 200-MHz Core/66-MHz Bus**
  - **— 166-MHz Core/66-MHz Bus**
  - **— 150-MHz Core/60-MHz Bus**
  - **— 133-MHz Core/66-MHz Bus**
  - **— 120-MHz Core/60-MHz Bus**
  - **— 100-MHz Core/66-MHz Bus**
  - **— 100-MHz Core/50-MHz Bus**
  - **— 90-MHz Core/60-MHz Bus**
  - **— 75-MHz Core/50-MHz Bus**

The Pentium® processor 75/90/100/120/133/150/166/200 extends the Pentium processor family, providing performance needed for mainstream desktop applications as well as for workstations and servers. The Pentium processor is compatible with the entire installed base of applications for DOS*, Windows*, OS/2*, and UNIX*. The Pentium processor 75/90/100/120/133/150/166/200 superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor 75/90/100/120/133/150/166/200 has 3.3 million transistors and is built on Intel's advanced 3.3V BiCMOS silicon technology. The Pentium processor 75/90/100/120/133/150/166/200 has on-chip dual processing support, a local multiprocessor interrupt controller, and SL power management features. The Pentium processor may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available upon request.



June 1997

Order Number 241997-010



1.0. MICROPROCESSOR ARCHITECTURE OVERVIEW

The Pentium® processor 75/90/100/120/133/150/166/200 extends the Intel Pentium family of microprocessors. It is binary compatible with the 8086/88, 80286, Intel386™ DX CPU, Intel386 SX CPU, Intel486™ DX CPU, Intel486 SX CPU, Intel486 DX2 CPU, and Pentium processor 60/66.

The Pentium processor family consists of the following products.

- Described in this document (product code 80502). The name "Pentium processor 75/90/100/120/133/150/166/200" will be used to refer to these products:
  - Pentium processor at 200 MHz, iCOMP® Index 2.0 rating = 142
  - Pentium processor at 166 MHz, iCOMP Index 2.0 rating = 127
  - Pentium processor at 150 MHz, iCOMP Index 2.0 rating = 114
  - Pentium processor at 133 MHz, iCOMP Index 2.0 rating = 111
  - Pentium processor at 120 MHz, iCOMP Index 2.0 rating = 100
  - Pentium processor at 100 MHz, iCOMP Index 2.0 rating = 90
  - Pentium processor at 90 MHz, iCOMP Index 2.0 rating = 81
  - Pentium processor at 75 MHz, iCOMP Index 2.0 rating = 67
- Original Pentium processor. The name "Pentium processor 60/66" will be used to refer to the original 60 and 66 MHz version products:
  - Pentium processor at 66 MHz, iCOMP Index 2.0 rating = 57
  - Pentium processor at 60 MHz, iCOMP Index 2.0 rating = 51

The Pentium processor family architecture contains all of the features of the Intel486 CPU family, and provides significant enhancements and additions including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 8K Code and 8K Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Functional Redundancy Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions

In addition to the features listed above, the Pentium processor 75/90/100/120/133/150/166/200 offers the following enhancements over Pentium processor 60/66:

- Fractional bus operation allowing higher core frequency operation
- Dual processing support
- SL power management features
- On-chip local APIC device

1.1. Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of CPUs.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used

redesigned over the Intel486 CPU. Faster algorithms provide up to 10X speed-up for common operations including add, multiply, and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache is 8 Kbytes in size, with a 32-byte line size and is 2-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be write back or write through on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst write back cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' Memory Management Unit

the "checker" is used to execute in lock step with the "master" processor. The checker samples the master's outputs and compares those values with the values it computes internally, and asserts an error signal if a mismatch occurs.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified 4 breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 shows a block diagram of the Pentium processor 75/90/100/120/133/150/166/200.

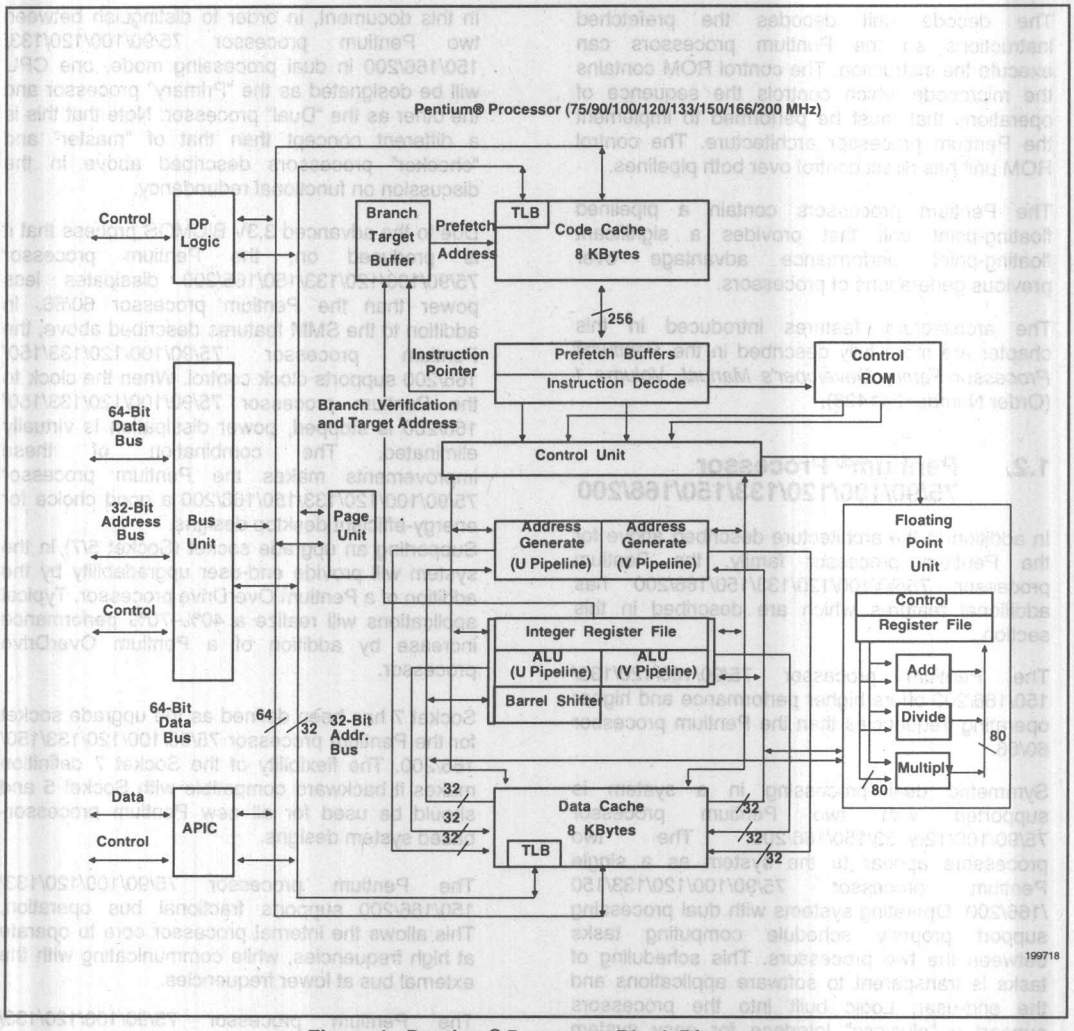


Figure 1. Pentium® Processor Block Diagram

The block diagram shows the two instruction pipelines, the "u" pipe and the "v" pipe. The u-pipe can execute all integer and floating point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processors can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

The architectural features introduced in this chapter are more fully described in the *Pentium® Processor Family Developer's Manual, Volume 1* (Order Number 241428).

1.2. Pentium® Processor 75/90/100/120/133/150/166/200

In addition to the architecture described above for the Pentium processor family, the Pentium processor 75/90/100/120/133/150/166/200 has additional features which are described in this section.

The Pentium processor 75/90/100/120/133/150/166/200 offers higher performance and higher operating frequencies than the Pentium processor 60/66.

Symmetric dual processing in a system is supported with two Pentium processor 75/90/100/120/133/150/166/200. The two processors appear to the system as a single Pentium processor 75/90/100/120/133/150/166/200. Operating systems with dual processing support properly schedule computing tasks between the two processors. This scheduling of tasks is transparent to software applications and the end-user. Logic built into the processors support a "glueless" interface for easy system design. Through a private bus, the two Pentium processor 75/90/100/120/133/150/166/200 arbitrate for the external bus and maintain cache coherency. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies.

In this document, in order to distinguish between two Pentium processor 75/90/100/120/133/150/166/200 in dual processing mode, one CPU will be designated as the "Primary" processor and the other as the "Dual" processor. Note that this is a different concept than that of "master" and "checker" processors described above in the discussion on functional redundancy.

Due to the advanced 3.3V BiCMOS process that it is produced on, the Pentium processor 75/90/100/120/133/150/166/200 dissipates less power than the Pentium processor 60/66. In addition to the SMM features described above, the Pentium processor 75/90/100/120/133/150/166/200 supports clock control. When the clock to the Pentium processor 75/90/100/120/133/150/166/200 is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the Pentium processor 75/90/100/120/133/150/166/200 a good choice for energy-efficient desktop designs.
Supporting an upgrade socket (Socket 5/7) in the system will provide end-user upgradability by the addition of a Pentium OverDrive processor. Typical applications will realize a 40%–70% performance increase by addition of a Pentium OverDrive processor.

Socket 7 has been defined as the upgrade socket for the Pentium processor 75/90/100/120/133/150/166/200. The flexibility of the Socket 7 definition makes it backward compatible with Socket 5 and should be used for all new Pentium processor-based system designs.

The Pentium processor 75/90/100/120/133/150/166/200 supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The Pentium processor 75/90/100/120/133/150/166/200 contains an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

1.3. Pentium® Processors with Voltage Reduction Technology

Currently, Intel's Pentium processor with Voltage Reduction Technology family consists of two sets of products. Please reference the appropriate datasheets for correct pinout, mechanical, thermal, and electrical specifications. Detailed information on Mobile Pentium processors based on 0.6 µm process technology (75, 90, and 100 MHz) is available in the datasheet *Pentium® Processors at iComp® Index 1000\120, 735\90, 610\75 MHz with Voltage Reduction Technology* (Order Number 242973). For detailed information on Mobile Pentium processors based on 0.35 µm process technology (100, 120, and 133 MHz), see Intel datasheet *Pentium® Processors at iComp® Index 1110\133, 1000\120, 815\100 MHz with Voltage Reduction Technology* (Order Number 242557).

2.0. PINOUT

2.1. Pinout and Pin Descriptions

2.1.1. PENTIUM® PROCESSOR 75/90/100/120/133/150/166/200 PINOUT

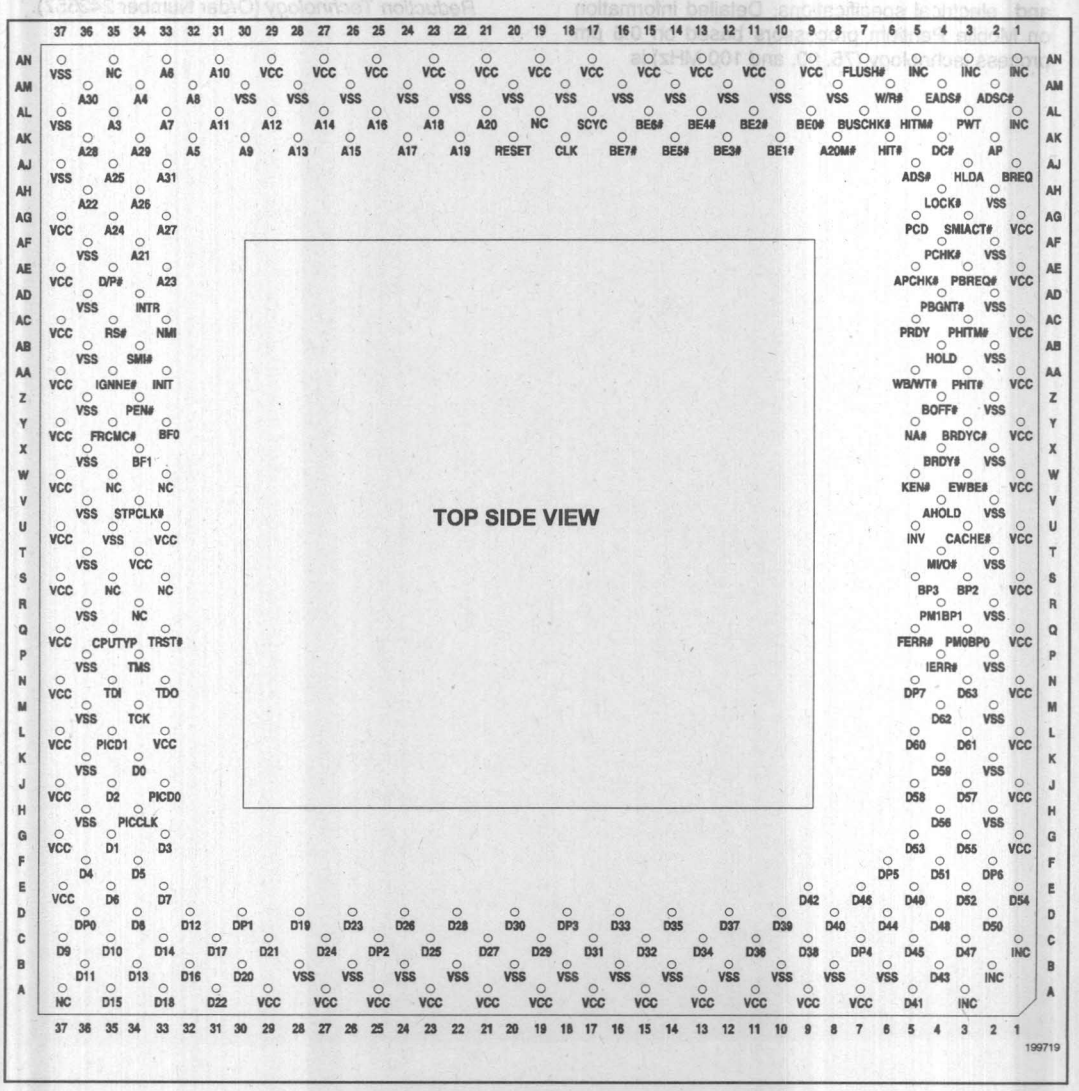


Figure 2. Pentium® Processor 75/90/100/120/133/150/166/200 SPGA and PPGA Package Pinout (Top Side View)

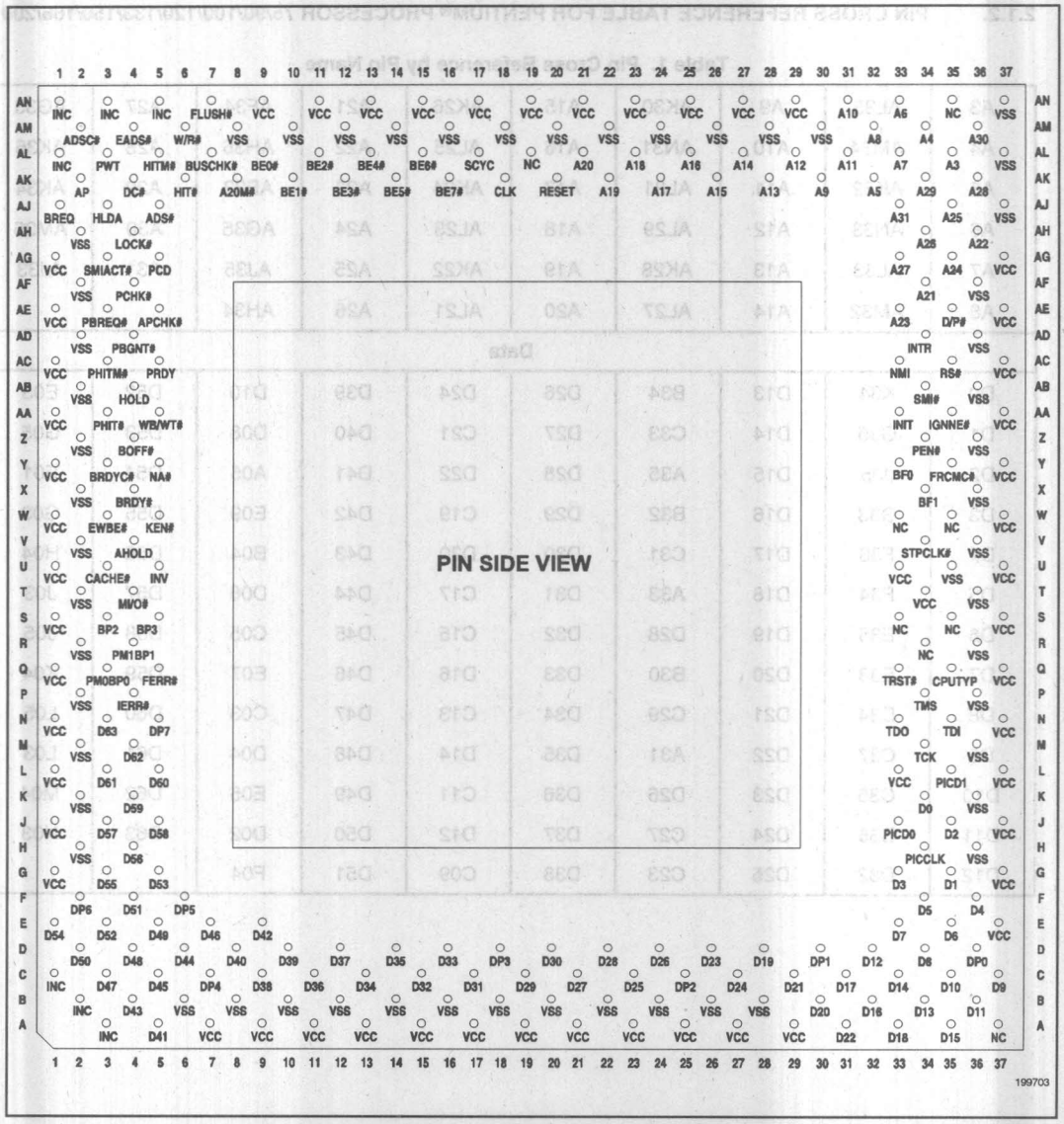


Figure 3. Pentium® Processor 75/90/100/120/133/150/166/200 SPGA and PPGA Package Pinout (Pin Side View)

2.1.2. PIN CROSS REFERENCE TABLE FOR PENTIUM® PROCESSOR 75/90/100/120/133/150/166/200

Table 1. Pin Cross Reference by Pin Name

A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 1. Pin Cross Reference by Pin Name (Continued)

Control							
A20M#	AK08	BRDYC#	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	FRCMC#	Y35	PM0/BP0	Q03
ADSC#	AM02	BUSCHK#	AL07	HIT#	AK06	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HITM#	AL05	PRDY	AC05
AP	AK02	CPUTYP	Q35	HLDA	AJ03	PWT	AL03
APCHK#	AE05	D/C#	AK04	HOLD	AB04	R/S#	AC35
BE0#	AL09	D/P#	AE35	IERR#	P04	RESET	AK20
BE1#	AK10	DP0	D36	IGNNE#	AA35	SCYC	AL17
BE2#	AL11	DP1	D30	INIT	AA33	SMI#	AB34
BE3#	AK12	DP2	C25	INTR/LINT0	AD34	SMIACT#	AG03
BE4#	AL13	DP3	D18	INV	U05	TCK	M34
BE5#	AK14	DP4	C07	KEN#	W05	TDI	N35
BE6#	AL15	DP5	F06	LOCK#	AH04	TDO	N33
BE7#	AK16	DP6	F02	M/IO#	T04	TMS	P34
BOFF#	Z04	DP7	N05	NA#	Y05	TRST#	Q33
BP2	S03	EADS#	AM04	NMI/LINT1	AC33	W/R#	AM06
BP3	S05	EWBE#	W03	PCD	AG05	WB/WT#	AA05
BRDY#	X04	FERR#	Q05	PCHK#	AF04		

APIC		Clock Control		Dual Processor Private Interface	
PICCLK	H34	CLK	AK18	PBGNT#	AD04
PICD0	J33	BF0	Y33	PBREQ#	AE03
[DPEN#]		BF1	X34	PHIT#	AA03
PICD1	L35	STPCLK#	V34	PHITM#	AC03
[APICEN]					

V_{CC}								
A07	A19	E37	L33	S01	W01	AC01	AN09	AN21
A09	A21	G01	L37	S37	W37	AC37	AN11	AN23
A11	A23	G37	N01	T34	Y01	AE01	AN13	AN25
A13	A25	J01	N37	U01	Y37	AE37	AN15	AN27
A15	A27	J37	Q01	U33	AA01	AG01	AN17	AN29
A17	A29	L01	Q37	U37	AA37	AG37	AN19	

B12	B28	P36	X02	AF02	AM14	AM30
B14	H02	R02	X36	AF36	AM16	AN37
B16	H36	R36	Z02	AH02	AM18	
B18	K02	T02	Z36	AJ37	AM20	
B20	K36	T36	AB02	AL37	AM22	
NC/INC[1]						
A03	C01	S35	W35	AL01	AN01	AN05
A37	R34	W33		AL19	AN03	AN35
B02	S33					

NOTE:

1. Please refer to socket 5 and socket 7 specifications if using socket 5 or socket 7.

2.2. Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active HIGH inputs should be connected to GND.

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

2.3. Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the "Hardware Interface" chapter in the *Pentium® Processor Family Developer's Manual*, Volume 1.

Note

All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

The following pins exist on the Pentium processor 60/66 but have been removed from the Pentium processor 75/90/100/120/133/150/166/200:

- IBT, IU, IV, BT0-3

The following pins become I/O pins when two Pentium processors 75/90/100/120/133/150/166/200 are operating in a dual processing environment:

- ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC

Table 2. Quick Pin Reference

Symbol	Type*	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor 75/90/100/120/133/150/166/200 emulates the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the Pentium processor 75/90/100/120/133/150/166/200 when configured as a Dual processor.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the Pentium processor 75/90/100/120/133/150/166/200.
ADSC#	O	ADSC# is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium processor 75/90/100/120/133/150/166/200 will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium processor 75/90/100/120/133/150/166/200 with even parity information on all Pentium processor 75/90/100/120/133/150/166/200 generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium processor 75/90/100/120/133/150/166/200 during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium processor 75/90/100/120/133/150/166/200.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium processor 75/90/100/120/133/150/166/200 has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Additionally, the lower 4-byte enables (BE3#-BE0#) are used on the Pentium processor 75/90/100/120/133/150/166/200 as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
BF[1:0]	I	**Bus Frequency** determines the bus-to-core frequency ratio. BF[1:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[1:0] must not change values while RESET is active. See Table 3 for Bus Frequency Selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium processor 75/90/100/120/133/150/166/200 will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor 75/90/100/120/133/150/166/200 restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium processor 75/90/100/120/133/150/166/200 data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	This signal has the same functionality as BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium processor 75/90/100/120/133/150/166/200 has internally generated a bus request. This signal is always driven whether or not the Pentium processor 75/90/100/120/133/150/166/200 is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor 75/90/100/120/133/150/166/200 will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor 75/90/100/120/133/150/166/200 will vector to the machine check exception. **NOTE:** To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
CACHE#	O	For Pentium processor 75/90/100/120/133/150/166/200 -initiated cycles the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor 75/90/100/120/133/150/166/200 will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the Pentium processor 75/90/100/120/133/150/166/200. Its frequency is the operating frequency of the Pentium processor 75/90/100/120/133/150/166/200 external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK. **NOTE:** It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the Pentium processor 75/90/100/120/133/150/166/200 is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC}. For the Pentium OverDrive processor, CPUTYP will be used to determine whether the bootup handshake protocol will be used (in a dual socket system) or not (in a single socket system).
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor 75/90/100/120/133/150/166/200 with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor 75/90/100/120/133/150/166/200 on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor 75/90/100/120/133/150/166/200. DP7 applies to D63-56, DP0 applies to D7-0.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# shares a pin with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium processor 75/90/100/120/133/150/166/200 address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium processor 75/90/100/120/133/150/166/200 generates a write, and EWBE# is sampled inactive, the Pentium processor 75/90/100/120/133/150/166/200 will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating point error** pin is driven active when an unmasked floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# is never driven active by the Dual processor.
FLUSH#	I	When asserted, the **cache flush** input forces the Pentium processor 75/90/100/120/133/150/166/200 to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium processor 75/90/100/120/133/150/166/200 indicating completion of the write back and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered. If two Pentium processor 75/90/100/120/133/150/166/200 are operating in dual processing mode and FLUSH# is asserted, the Dual processor will perform a flush first (without a flush acknowledge cycle), then the Primary processor will perform a flush followed by a flush acknowledge cycle. **NOTE:** If the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
FRCMC#	I	The **functional redundancy checking master/checker** mode input is used to determine whether the Pentium processor 75/90/100/120/133/150/166/200 is configured in master mode or checker mode. When configured as a master, the Pentium processor 75/90/100/120/133/150/166/200 drives its output pins as required by the bus protocol. When configured as a checker, the Pentium processor 75/90/100/120/133/150/166/200 tristates all outputs (except IERR# and TDO) and samples the output pins. The configuration as a master/checker is set after RESET and may not be changed other than by a subsequent RESET.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor 75/90/100/120/133/150/166/200 data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium processor 75/90/100/120/133/150/166/200 cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor 75/90/100/120/133/150/166/200 has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor 75/90/100/120/133/150/166/200 will resume driving the bus. If the Pentium processor 75/90/100/120/133/150/166/200 has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the **bus hold request**, the Pentium processor 75/90/100/120/133/150/166/200 will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor 75/90/100/120/133/150/166/200 will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium processor 75/90/100/120/133/150/166/200 will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. If a parity error occurs on a read from an internal array, the Pentium processor 75/90/100/120/133/150/166/200 will assert the IERR# pin for one clock and then shutdown. If the Pentium processor 75/90/100/120/133/150/166/200 is configured as a checker and a mismatch occurs between the value sampled on the pins and the corresponding value computed internally, the Pentium processor 75/90/100/120/133/150/166/200 will assert IERR# two clocks after the mismatched value is returned.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor 75/90/100/120/133/150/166/200 will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor 75/90/100/120/133/150/166/200 will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor 75/90/100/120/133/150/166/200 will stop execution and wait for an external interrupt. IGNNE# is internally masked when the Pentium processor 75/90/100/120/133/150/166/200 is configured as a Dual processor.
INIT	I	The Pentium processor 75/90/100/120/133/150/166/200 **initialization** input pin forces the Pentium processor 75/90/100/120/133/150/166/200 to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the Pentium processor 75/90/100/120/133/150/166/200 will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor 75/90/100/120/133/150/166/200 will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized. If the local APIC is enabled, this pin becomes LINT0.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium processor 75/90/100/120/133/150/166/200 generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LINT0/INTR	I	If the APIC is enabled, this pin is **local interrupt 0**. If the APIC is disabled, this pin is INTR.
LINT1/NMI	I	If the APIC is enabled, this pin is **local interrupt 1**. If the APIC is disabled, this pin is NMI.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor 75/90/100/120/133/150/166/200 will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor 75/90/100/120/133/150/166/200 will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium processor 75/90/100/120/133/150/166/200 supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. If the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processor 75/90/100/120/133/150/166/200 are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor 75/90/100/120/133/150/166/200 exists in a system.
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processor 75/90/100/120/133/150/166/200 are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor 75/90/100/120/133/150/166/200 exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processor 75/90/100/120/133/150/166/200 are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor 75/90/100/120/133/150/166/200 will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium processor 75/90/100/120/133/150/166/200 will vector to the machine check exception before the beginning of the next instruction.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processor 75/90/100/120/133/150/166/200 are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected if only one Pentium processor 75/90/100/120/133/150/166/200 exists in a system.
PHITM#	I/O	**Private modified hit** is a hit indication used when two Pentium processor 75/90/100/120/133/150/166/200 are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one Pentium processor 75/90/100/120/133/150/166/200 exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor 75/90/100/120/133/150/166/200.
PICD0-1 [DPEN#] [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium processor 75/90/100/120/133/150/166/200 comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals share pins with DPEN# and APICEN respectively.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
R/S#	I	The **run/stop** input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	**RESET** forces the Pentium processor 75/90/100/120/133/150/166/200 to begin execution at a known state. All the Pentium processor 75/90/100/120/133/150/166/200 internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH#, FRCMC# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.

Table 2. Quick Pin Reference (Continued)

Symbol	Type*	Name and Function
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor 75/90/100/120/133/150/166/200 thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium processor 75/90/100/120/133/150/166/200 will still respond to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the Pentium processor 75/90/100/120/133/150/166/200 boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium processor 75/90/100/120/133/150/166/200 during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium processor 75/90/100/120/133/150/166/200 on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor 75/90/100/120/133/150/166/200 on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC}	I	The Pentium processor 75/90/100/120/133/150/166/200 has 53 3.3V **power** inputs.
V_{SS}	I	The Pentium processor 75/90/100/120/133/150/166/200 has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

NOTE:

- The pins are classified as Input or Output based on their function in Master Mode. See the Functional Redundancy Checking section in the "Error Detection" chapter of the *Pentium® Processor Family Developer's Manual*, Volume 1, for further information.

Table 3. Bus Frequency Selections

Pentium® Processor Core Frequency (max)	External Bus Frequency (max)	Bus/Core Ratio	BF1	BF0
200 MHz	66 MHz	1/3	0	1
166 MHz	66 MHz	2/5	0	0
150 MHz	60 MHz	2/5	0	0
133 MHz	66 MHz	1/2	1	0
120 MHz	60 MHz	1/2	1	0
100 MHz	66 MHz	2/3	1	1
100 MHz	50 MHz	1/2	1	0
90 MHz	60 MHz	2/3	1	1
75 MHz	50 MHz	2/3	1	1

2.4. Pin Reference Tables

Table 4. Output Pins

Name	Active Level	When Floated
ADS#*	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#*	Low	Bus Hold, BOFF#
D/P#**	n/a	
FERR#**	Low	
HIT#*	Low	
HITM#*	Low	
HLD A*	High	
IERR#	Low	
LOCK#*	Low	Bus Hold, BOFF#

Table 4. Output Pins (Continued)

Name	Active Level	When Floated
M/IO#*, D/C#*, W/R#*	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC*	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:
All output and input/output pins are floated during tristate test mode and checker mode (except IERR#).

* These are I/O signals when two Pentium® processor 75/90/100/120/133/150/166/200 are operating in dual processing mode.

** These signals are undefined when the CPU is configured as a Dual Processor.

Table 5. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#*	Low	Asynchronous		
AHOLD	High	Synchronous		
BF[1:0]	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
CPUTYP	High	Synchronous/RESET		
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
FRCMC#	Low	Asynchronous		
HOLD	High	Synchronous		

Table 5. Input Pins (Continued)

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
IGNNE#*	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pullup	
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

NOTE:
* Undefined when the CPU is configured as a Dual processor.

PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTE:
All output and input/output pins are floated during tristate test mode (except TDO) and checker mode (except IERR# and TDO).
* BE3#-BE0# have Pulldowns during RESET only.

Table 7. Inter-Processor Input/Output Pins

Name	Active Level	Internal Resistor
PHIT#	Low	Pullup
PHITM#	Low	Pullup
PBGNT#	Low	Pullup
PBREQ#	Low	Pullup

NOTE:
For proper inter-processor operation, the system cannot load these signals.

2.5. Pin Grouping According to Function

Table 8 organizes the pins with respect to their function.

Table 8. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF1–BF0
Address Bus	A31-A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0-1
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
Functional Redundancy Checking	FRCMC# (IERR#)
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Probe Mode	R/S#, PRDY

3.0. ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium processor 60/66 and the Pentium processor 75/90/100/120/133/150/166/200 and the DC and AC specifications.

3.1. Electrical Differences Between Pentium® Processor 75/90/100/120/133/150/166/200 and Pentium Processor 60/66

Pentium Processor 60/66 Electrical Characteristic	Difference in Pentium® Processor 75/90/100/120/133/150/166/200
5V Power Supply	3.3V Power Supply*
5V TTL Inputs/Outputs	3.3V Inputs/Outputs
Pentium Processor 60/66 Buffer Models	Pentium Processor 75/90/100/120/133/150/166/200 Buffer Models

* The upgrade socket specifies two 5V inputs (section 6.0.).

The sections that follow will briefly point out some ways to design with these electrical differences.

3.1.1. 3.3V POWER SUPPLY

The Pentium processor 75/90/100/120/133/150/166/200 has all V_{CC} 3.3V inputs. By connecting all Pentium processor 60/66 V_{CC} inputs to a common and dedicated power plane, that plane can be converted to 3.3V for the Pentium processor 75/90/100/120/133/150/166/200.

The CLK and PICCLK inputs can tolerate a 5V input signal. This allows the Pentium processor 75/90/100/120/133/150/166/200 to use 5V or 3.3V clock drivers.

3.1.2. 3.3V INPUTS AND OUTPUTS

The inputs and outputs of the Pentium processor 75/90/100/120/133/150/166/200 are 3.3V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the 3.3V V_{IN} max.

For Pentium processor 75/90/100/120/133/150/166/200 outputs, if the Pentium processor 60/66 system support components use TTL-compatible inputs, they will interface to the Pentium processor 75/90/100/120/133/150/166/200 without extra logic. This is because the Pentium processor 75/90/100/120/133/150/166/200 drives according to the 5V TTL specification (but not beyond 3.3V).

For Pentium processor 75/90/100/120/133/150/166/200 inputs, the voltage must not exceed the 3.3V V_{IH3} maximum specification. System support components can consist of 3.3V devices or open-collector devices. 3.3V support components may interface to the Pentium processor 60/66 since they typically meet 5V TTL specifications. In an open-collector configuration, the external resistor may be biased with the CPU V_{CC}; as the CPU's V_{CC} changes from 5V to 3.3V, so does this signal's maximum drive.

The CLK and PICCLK inputs of the Pentium processor 75/90/100/120/133/150/166/200 are 5V tolerant, so they are electrically identical to the Pentium processor 60/66 clock input. This allows a Pentium processor 60/66 clock driver to drive the Pentium processor 75/90/100/120/133/150/166/200.

All pins, other than the CLK and PICCLK inputs, are 3.3V-only. If an 8259A interrupt controller is used, for example, the system must provide level converters between the 8259A and the Pentium processor 75/90/100/120/133/150/166/200.

3.1.3. 3.3V PENTIUM® PROCESSOR 75/90/100/120/133/150/166/200 BUFFER MODELS

The structure of the buffer models of the Pentium processor 75/90/100/120/133/150/166/200 is the same as that of the Pentium processor 60/66 , but the values of the components change since the Pentium processor 75/90/100/120/133/150/166/200 buffers are 3.3V buffers on a different process.

Despite this difference, the simulation results of Pentium processor 75/90/100/120/133/150/166/200 buffers and Pentium processor 60/66 buffers look nearly identical. Since the 0pF AC specifications of the Pentium processor 75/90/100/120/133/150/166/200 are derived from the Pentium processor 60/66 specifications, the system should see little difference between the AC behavior of the Pentium processor 75/90/100/120/133/150/166/200 and the Pentium processor 60/66.

To meet specifications, simulate the AC timings with Pentium processor 75/90/100/120/133/150/166/200 buffer models. Pay special attention to the new signal quality restrictions imposed by 3.3V buffers.

3.2. Absolute Maximum Ratings

The values listed below are stress ratings only. Functional operation at the maximums is not implied or guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor 75/90/100/120/133/150/166/200 contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Case temperature under bias ..... –65°C to 110°C

Storage temperature ..... –65°C to 150°C

3VSupply voltage with respect to V_{ss} ..... –0.5V to +4.6V

3V Only Buffer DC Input Voltage .....–0.5V to V_{cc} + 0.5; not to exceed V_{CC3} max (2)

5V Safe Buffer DC Input Voltage .....–0.5V to 6.5V (1,3)

NOTES:

1. Applies to CLK and PICCLK.
2. Applies to all Pentium processor 75/90/100/120/133/150/166/200 inputs except CLK and PICCLK.
3. See overshoot/undershoot transient spec.

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

3.3. DC Specifications

Table 9, Table 10, and Table 11 list the DC specifications which apply to the Pentium processor 75/90/100/120/133/150/166/200. The Pentium processor 75/90/100/120/133/150/166/200 is a 3.3V part internally. The CLK and PICCLK inputs may be 3.3V or 5V inputs. Since the 3.3V (5V-safe) input levels defined in Table 9 are the same as the 5V TTL levels, the CLK and PICCLK inputs are compatible with existing 5V clock drivers. The power dissipation specification in Table 12 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst case power the device would dissipate in a system. This number is used for design of a thermal solution for the device.

				4250	mA	166 MHz (4)
				3850	mA	150 MHz (4)
				3400	mA	133 MHz (4)
				3730	mA	120 Mhz (4,5)
				3250	mA	100 Mhz (4)
				2950	mA	90 Mhz (4)
				2650	mA	75 Mhz (4)

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK and PICCLK.
4. This value should be used for power supply design. It was determined using a worst case instruction mix and V_{CC} = 3.6V. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to section 3.4.3.
5. Please also check *Pentium®.Processor Specification Update* (Order Number 24280).

Table 10. 3.3V (5V-Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	-0.3	0.8	V	TTL Level(1)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level(1)

NOTE:

1. Applies to CLK and PICCLK only.

Table 11. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	4
C_O	Output Capacitance		20	pF	4
$C_{I/O}$	I/O Capacitance		25	pF	4
C_{CLK}	CLK Input Capacitance		15	pF	4
C_{TIN}	Test Input Capacitance		15	pF	4
C_{TOUT}	Test Output Capacitance		20	pF	4
C_{TCK}	Test Clock Capacitance		15	pF	4
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$(1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$(1)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4V(3)
I_{IL}	Input Leakage Current		-400	µA	V_{IN} = 0.4V(2)

NOTES:
1. This parameter is for input without pullup or pulldown.
2. This parameter is for input with pullup.
3. This parameter is for input with pulldown.
4. Guaranteed by design.

Table 12. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical(1)	Max	Unit	Notes
Active Power Dissipation	6.5	15.5(7)	Watts	200 MHz
	5.4	14.5(7)	Watts	166 MHz
	4.9	11.6(2)	Watts	150 MHz
	4.3	11.2(2)	Watts	133 MHz
	5.06	12.81(6)	Watts	120 MHz
	3.9	10.1(2)	Watts	100 MHz
	3.5	9.0(2)	Watts	90 MHz
	3.0	8.0(2)	Watts	75 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		2.5	Watts	200 Mhz (3)
		2.1	Watts	166 MHz (3)
		1.9	Watts	150 MHz (3)
		1.7	Watts	133 Mhz (3)
		1.76	Watts	120 Mhz (3)
		1.55	Watts	100 Mhz (3)
		1.40	Watts	90 Mhz (3)
		1.20	Watts	75 MHz (3)
Stop Clock Power Dissipation	0.02	<0.3	Watts	(4,5)

NOTES:

1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at nominal V_{CC} (3.3V for 75, 100, 120, 133, and 150 Mhz processors and 3.5V for 166 and 200 Mhz processors) running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with V_{CC} = 3.3V and also takes into account the thermal time constants of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. Complete characterization of this specification was still in process at the time of print. Please contact Intel for the latest information. The final specification will be less than 0.1W.
6. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with V_{CC}=3.52V and also takes into account the thermal time constants of the package.
7. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst-case instruction mix with V_{CC}=3.5V, and also takes into account the thermal time constants of the package.

3.4. AC Specifications

The AC specifications of the Pentium processor 75/90/100/120/133/150/166/200 consist of setup times, hold times, and valid delays at 0 pF.

3.4.1. PRIVATE BUS

When two Pentium processor 75/90/100/120/133/150/166/200 are operating in dual processor mode, a "private bus" exists to arbitrate for the CPU bus and

maintain local cache coherency. The private bus consists of two pinout changes:

1. Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
2. Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC.

The new pins are given AC specifications of valid delays at 0 pF, setup times, and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must only be met when a dual processor is present in the system.

3.4.2. POWER AND GROUND

For clean on-chip power distribution, the Pentium processor 75/90/100/120/133/150/166/200 has 53 V_{CC} (power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium processor 75/90/100/120/133/150/166/200. On the circuit board all V_{CC} pins must be connected to a V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

3.4.3. DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Pentium processor 75/90/100/120/133/150/166/200. The Pentium processor 75/90/100/120/133/150/166/200 driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Pentium processor 75/90/100/120/133/150/166/200 and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

For the Pentium processor 75/90/100/120/133/150/166/200, the power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the Pentium processor 75/90/100/120/133/150/166/200 to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the Pentium processor 75/90/100/120/133/150/166/200. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the Pentium processor 75/90/100/120/133/150/166/200 (on the 3.3V plane) to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

3.4.4. CONNECTION SPECIFICATIONS

All NC and INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground.

3.4.5. AC TIMING TABLES

3.4.5.1. AC Timing Table for a 50-MHz Bus

The AC specifications given in Table 13 and Table 14 consist of output delays, input setup requirements and input hold requirements for a 50-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor 75/90/100/120/133/150/166/200 operation.

Table 13. Pentium® Processor 75 and 100 MHz AC Specifications for 50-MHz Bus Operation

$3.135 < V_{CC} < 3.6V$, $T_{CASE} = 0$ to 70°C, $C_L = 0$ pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	25.0	50.0	MHz		Max Core Freq = 100 MHz
t_{1a}	CLK Period	20.0	40.0	nS	4	
t_{1b}	CLK Period Stability		±250	pS		Adjacent Clocks (1,25)
t_2	CLK High Time	4.0		nS	4	2V,(1)
t_3	CLK Low Time	4.0		nS	4	0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	4	(2.0V–0.8V), (1,5)
t_5	CLK Rise Time	0.15	1.5	nS	4	(0.8V–2.0V), (1,5)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	nS	5	
t_{6b}	AP Valid Delay	1.0	8.5	nS	5	
t_{6c}	BE0-7#, LOCK# Valid Delay	0.9	7.0	nS	5	
t_{6d}	ADS#, ADSC#, D/C#, M/IO#, W/R#, SCYC Valid Delay	0.8	7.0	nS	5	
t_{6e}	A3-A16 Valid Delay	0.5	7.0	nS	5	
t_{6f}	A17-A31 Valid Delay	0.6	7.0	nS	5	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	6	1

Table 13. Pentium® Processor 75 and 100 MHz AC Specifications for 50-MHz Bus Operation (Continued)

$3.135 < V_{CC} < 3.6V$, $T_{CASE} = 0$ to 70°C, $C_L = 0$ pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_8	APCHK#, IERR#, FERR#, PCHK# Valid Delay	1.0	8.3	nS	5	4
t_{9a}	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	5	4
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	5	
t_{10b}	HITM# Valid Delay	0.7	6.0	nS	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	5	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	6	1
t_{14}	A5-A31 Setup Time	6.5		nS	7	26
t_{15}	A5-A31 Hold Time	1.0		nS	7	
t_{16a}	INV, AP Setup Time	5.0		nS	7	
t_{16b}	EADS# Setup Time	6.0		nS	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	7	
t_{18a}	KEN# Setup Time	5.0		nS	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	7	
t_{22}	BOFF# Setup Time	5.5		nS	7	
t_{22a}	AHOLD Setup Time	6.0		nS	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	7	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	7	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	7	
t_{25a}	HOLD Hold Time	1.5		nS	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	7	12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1 .0		nS	7	13

	Width, Async					
t_{31}	R/S# Setup Time	5.0		nS	7	12, 16, 17
t_{32}	R/S# Hold Time	1.0		nS	7	13
t_{33}	R/S# Pulse Width, Async.	2. 0		CLKs	7	15, 17
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	7	
t_{36}	RESET Setup Time	5.0		nS	8	11, 12, 16
t_{37}	RESET Hold Time	1.0		nS	8	11, 13
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	8	11, 17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	8	12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	8	13
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async	2.0		CLKs	8	To RESET falling edge(16)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async	2.0		CLKs	8	To RESET falling edge(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge(27)
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge(1,27)
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	8	To RESET falling edge(22)
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	8	To RESET falling edge(22)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	8	To RESET falling edge

Table 13. Pentium® Processor 75 and 100 MHz AC Specifications for 50-MHz Bus Operation (Continued)

$3.135 < V_{CC} < 3.6V$, $T_{CASE} = 0$ to 70°C, $C_L = 0$ pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	8	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		nS	4	
t_{46}	TCK High Time	25.0		nS	4	2V(1)
t_{47}	TCK Low Time	25.0		nS	4	0.8V(1)
t_{48}	TCK Fall Time		5.0	nS	4	(2.0V–0.8V)(1,8,9)
t_{49}	TCK Rise Time		5.0	nS	4	(0.8V–2.0V)(1,8,9)
t_{50}	TRST# Pulse Width	40.0		nS	10	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	9	7
t_{52}	TDI, TMS Hold Time	13.0		nS	9	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	9	8
t_{54}	TDO Float Delay		25.0	nS	9	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	9	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	9	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	9	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	9	3, 7, 10
	APIC AC Specifications					
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60.0	500.0	nS	4	
t_{60c}	PICCLK High Time	15.0		nS	4	
t_{60d}	PICCLK Low Time	15.0		nS	4	
t_{60e}	PICCLK Rise Time	0.15	25	nS	4	
t_{60f}	PICCLK Fall Time	0.15	25	nS	4	
t_{60g}	PICD0-1 Setup Time	3.0		nS	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	7	To PICCLK

Table 13. Pentium® Processor 75 and 100 MHz AC Specifications for 50-MHz Bus Operation (Continued)

$3.135 < V_{CC} < 3.6V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	nS	5	From PICCLK(28,29)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	nS	5	From PICCLK(28,29)
t_{61}	PICCLK Setup Time	5.0		nS		To CLK (30)
t_{62}	PICCLK Hold Time	2.0		nS		To CLK (30)
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				31

Note: See notes following Table 18.

t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	6.0		nS	7	18, 21
t_{83c}	ADS#, M/IO# Setup Time	8.0		nS	7	18, 21
t_{83d}	HIT#, HITM# Setup Time	8.0		nS	7	18, 21
t_{83e}	HLDA Setup Time	6.0		nS	7	18, 21
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A5-A31, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		nS	7	18, 21
t_{85}	DPEN# Valid Time		10.0	CLKs		18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLKs		18, 20, 23
t_{87}	APIC ID (BE0#-BE3#) Setup Time	2.0		CLKs	8	To RESET falling edge(23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLKs	8	From RESET falling edge(23)
t_{89}	D/P# Valid Delay	1.0	8.0	nS	5	Primary Processor Only

Note: See notes following Table 18.

3.4.5.2. AC Timing Tables for a 60-MHz Bus

The AC specifications given in Table 15 and Table 16 consist of output delays, input setup requirements and input hold requirements for a 60-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor 75/90/100/120/133/150/166/200 operation.

Table 15. Pentium® Processor 90, 120 and 150 MHz AC Specifications for 60-MHz Bus Operation

$3.135 < V_{CC} < 3.6V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz	4	
t_{1a}	CLK Period	16.67	33.33	nS	4	
t_{1b}	CLK Period Stability		±250	pS	4	Adjacent Clocks (1,25)
t_2	CLK High Time	4.0		nS	4	2V(1)
t_3	CLK Low Time	4.0		nS	4	0.8V(1)
t_4	CLK Fall Time	0.15	1.5	nS	4	(2.0V–0.8V)(1,5)
t_5	CLK Rise Time	0.15	1.5	nS	4	(0.8V–2.0V)(1,5)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	nS	5	
t_{6b}	AP Valid Delay	1.0	8.5	nS	5	
t_{6c}	BE0-7#, LOCK# Valid Delay	0.9	7.0	nS	5	
t_{6d}	ADS#, ADSC#, D/C#, M/IO#, W/R#, SCYC, Valid Delay	0.8	7.0	nS	5	
t_{6e}	A3–A16 Valid Delay	0.5	6.3	nS	5	
t_{6f}	A17–A31 Valid Delay	0.6	6.3	nS	5	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	5	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	5	4
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	5	4
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	5	
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	5	
t_{10b}	HITM# Valid Delay	0.7	6.0	nS	5	

Table 15. Pentium® Processor 90, 120 and 150 MHz AC Specifications for 60-MHz Bus Operation
(Continued)

$3.135 < V_{CC} < 3.6V$, $T_{CASE} = 0$ to 70°C, $C_L = 0$ pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	5	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	6	1
t_{14}	A5-A31 Setup Time	6.0		nS	7	26
t_{15}	A5-A31 Hold Time	1.0		nS	7	
t_{16a}	INV, AP Setup Time	5.0		nS	7	
t_{16b}	EADS# Setup Time	5.5		nS	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	7	
t_{18a}	KEN# Setup Time	5.0		nS	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	7	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	7	
t_{25b}	HOLD Hold Time	1.5		nS	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	7	12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	7	13
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	7	12, 16, 17
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	7	13
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		15, 17
t_{31}	R/S# Setup Time	5.0		nS	7	12, 16, 17

t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	8	
t_{36}	RESET Setup Time	5.0		nS	8	11, 12, 16
t_{37}	RESET Hold Time	1.0		nS	8	11, 13
t_{38}	RESET Pulse Width, VCC & CLK Stable	15		CLKs	8	11, 17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	8	12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	8	13
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge(16)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge(27)
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge(1,27)
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	8	To RESET falling edge(22)
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	8	To RESET falling edge(22)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	8	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	8	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz	8	
t_{45}	TCK Period	62.5		nS	4	
t_{46}	TCK High Time	25.0		nS	4	2V(1)

t_{50}	TRST# Pulse Width	40.0		nS	10	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	9	7
t_{52}	TDI, TMS Hold Time	13.0		nS	9	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	9	8
t_{54}	TDO Float Delay		25.0	nS	9	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	9	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	9	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	9	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	9	3, 7, 10
	APIC AC Specifications					
t_{60a}	PICCLK Frequency	2.0	16.66	MHz	4	
t_{60b}	PICCLK Period	60.0	500.0	nS	4	
t_{60c}	PICCLK High Time	15.0		nS	4	
t_{60d}	PICCLK Low Time	15.0		nS	4	
t_{60e}	PICCLK Rise Time	0.15	2.5	nS	4	
t_{60f}	PICCLK Fall Time	0.15	2.5	nS	4	
t_{60g}	PICD0-1 Setup Time	3.0		nS	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	nS	5	From PICCLK(28,29)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	nS	5	From PICCLK(28,29)
t_{61}	PICCLK Setup Time	5.0		nS		To CLK (30)
t_{62}	PICCLK Hold Time	2.0		nS		To CLK (30)
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				31

Note: See notes following Table 18.

Table 16. Pentium® Processor 90, 120 and 150 MHz Dual Processor Mode AC Specifications for 60-MHz Bus Operation

$3.135 < V_{CC} < 3.6V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT#, PHIT# Flight Time	0	2.0	nS		29
t_{80b}	PHITM# Flight Time	0	1.8	nS		29
t_{83a}	A5-A31 Setup Time	3.9		nS	7	18, 21, 26
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	4.0		nS	7	18, 21
t_{83c}	ADS#, M/IO# Setup Time	6.0		nS	7	18, 21
t_{83d}	HIT#, HITM# Setup Time	6.0		nS	7	18, 21
t_{83e}	HLDA Setup Time	6.0		nS	7	18, 21
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A5-A31, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		nS	7	18, 21
t_{85}	DPEN# Valid Time		10.0	CLKs		18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLKs		18, 20, 23
t_{87}	APIC ID (BE0#–BE3#) Setup Time	2.0		CLKs	8	To RESET falling edge(23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLKs	8	From RESET falling edge(23)
t_{89}	D/P# Valid Delay	1.0	8.0	nS	5	Primary Processor Only

Note: See notes following Table 18.

3.4.5.3. AC Timing Tables for a 66-MHz Bus

The AC specifications given in Table 17 and Table 18 consist of output delays, input setup requirements and input hold requirements for a 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and AP IC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor 75/90/100/120/133/150/166/200 operation.

Table 17. Pentium® Processor 100, 133, 166 and 200 MHz AC Specifications for 66-MHz Bus Operation

$3.135 < V_{CC} < 3.6V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	nS	4	
t_{1b}	CLK Period Stability		±250	pS		Adjacent Clocks (1,25)
t_2	CLK High Time	4.0		nS	4	2V(1)
t_3	CLK Low Time	4.0		nS	4	0.8V(1)
t_4	CLK Fall Time	0.15	1.5	nS	5	(2.0V–0.8V)(1)
t_5	CLK Rise Time	0.15	1.5	nS	4	(0.8V–2.0V)(1)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	nS	5	
t_{6b}	AP Valid Delay	1.0	8.5	nS	5	
t_{6c}	BE0-7#, LOCK# Valid Delay	0.9	7.0	nS	5	
t_{6d}	ADS# Valid Delay	0.8	6.0	nS	5	
t_{6e}	ADSC#, D/C#, W/R#, SCYC, Valid Delay	0.8	7.0	nS	5	
t_{6f}	M/IO# Valid Delay	0.8	5.9	nS	5	
t_{6g}	A3–A16 Valid Delay	0.5	6.3	nS	5	
t_{6h}	A17–A31 Valid Delay	0.6	6.3	nS	5	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	6	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	5	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	5	4
t_{9a}	BREQ Valid Delay	1.0	8.0	nS	5	4
t_{9b}	SMIACT# Valid Delay	1.0	7.3	nS	5	4
t_{9c}	HLDA Valid Delay	1.0	6.8	nS	5	
t_{10a}	HIT# Valid Delay	1.0	6.8	nS	5	
t_{10b}	HITM# Valid Delay	0.7	6.0	nS	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	5	

t_{16b}	EADS# Setup Time	5.0		nS	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	7	
t_{18a}	KEN# Setup Time	5.0		nS	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	7	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		nS	7	
t_{24b}	PEN# Setup Time	4.8		nS	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	7	
t_{25b}	HOLD Hold Time	1.5		nS	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	7	12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	7	13
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	7	12, 16, 17
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	7	13

t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		15, 17
t_{34}	D0-D63, DP0-7 Read Data Setup Time	2.8		nS	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	7	
t_{36}	RESET Setup Time	5.0		nS	8	11, 12, 16
t_{37}	RESET Hold Time	1.0		nS	8	11, 13
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	8	11, 17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	8	12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	8	13
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge(16)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge(27)
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge(1,27)
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	8	To RESET falling edge(22)

Table 17. Pentium® Processor 100, 133, 166 and 200 MHz AC Specifications for 66-MHz Bus Operation (Continued)

$3.135 < V_{CC} < 3.6V$, $T_{CASE} = 0$ to 70°C, $C_L = 0$ pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	8	To RESET falling edge(22)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	8	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	8	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		nS	4	
t_{46}	TCK High Time	25.0		nS	4	2V(1)
t_{47}	TCK Low Time	25.0		nS	4	0.8V(1)
t_{48}	TCK Fall Time		5.0	nS	4	(2.0V–0.8V)(1,8,9)
t_{49}	TCK Rise Time		5.0	nS	4	(0.8V–2.0V)(1,8,9)
t_{50}	TRST# Pulse Width	40.0		nS	10	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	9	7
t_{52}	TDI, TMS Hold Time	13.0		nS	9	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	9	8
t_{54}	TDO Float Delay		25.0	nS	9	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	9	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	9	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	9	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	9	3, 7, 10
	APIC AC Specifications					
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60.0	500.0	nS	4	
t_{60c}	PICCLK High Time	15.0		nS	4	
t_{60d}	PICCLK Low Time	15.0		nS	4	
t_{60e}	PICCLK Rise Time	0.15	2.5	nS	4	
t_{60f}	PICCLK Fall Time	0.15	2.5	nS	4	

Table 17. Pentium® Processor 100, 133, 166 and 200 MHz AC Specifications for 66-MHz Bus Operation (Continued)

$3.135 < V_{CC} < 3.6V$, $T_{CASE} = 0$ to 70°C, $C_L = 0$ pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60g}	PICD0-1 Setup Time	3.0		nS	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	nS	5	From PICCLK(28,29)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	nS	5	From PICCLK(28,29)
t_{61}	PICCLK Setup Time	5.0		nS		To CLK (30)
t_{62}	PICCLK Hold Time	2.0		nS		To CLK (30)
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				31

Note: See notes following Table 18.

t_{83c}	ADS#, M/IO# Setup Time	5.8		nS	7	18, 21
t_{83d}	HIT#, HITM# Setup Time	6.0		nS	7	18, 21
t_{83e}	HLDA Setup Time	6.0		nS	7	18, 21
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A5-A31, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		nS	7	18, 21
t_{85}	DPEN# Valid Time		10.0	CLKs		18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLKs		18, 20, 23
t_{87}	APIC ID (BE0#-BE3#) Setup Time	2.0		CLKs	8	To RESET falling edge(23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLKs	8	From RESET falling edge(23)
t_{89}	D/P# Valid Delay	1.0	8.0	nS	5	Primary Processor Only

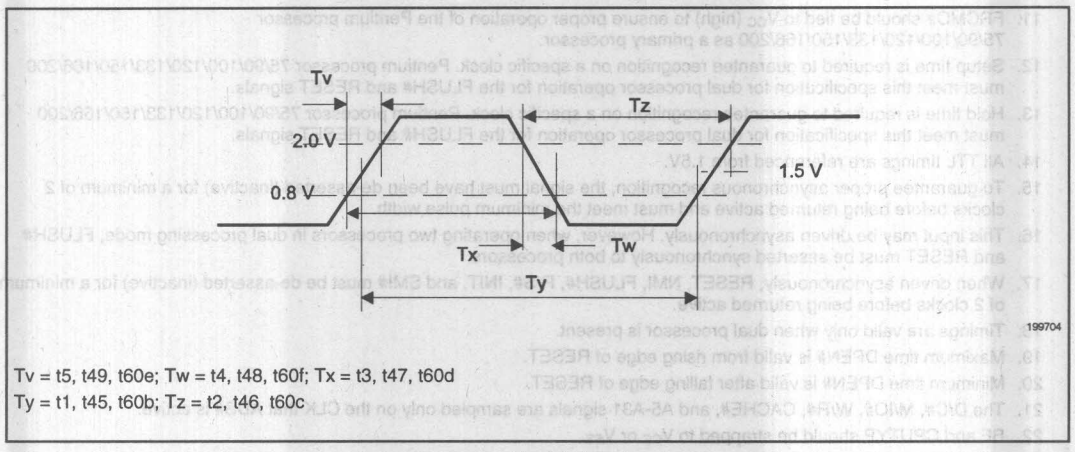
NOTES:

Notes 2, 6, and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1V/nS rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns ≤ CLK input rise/fall time ≤ 8V/ns.
6. 0.3V/ns ≤ input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).

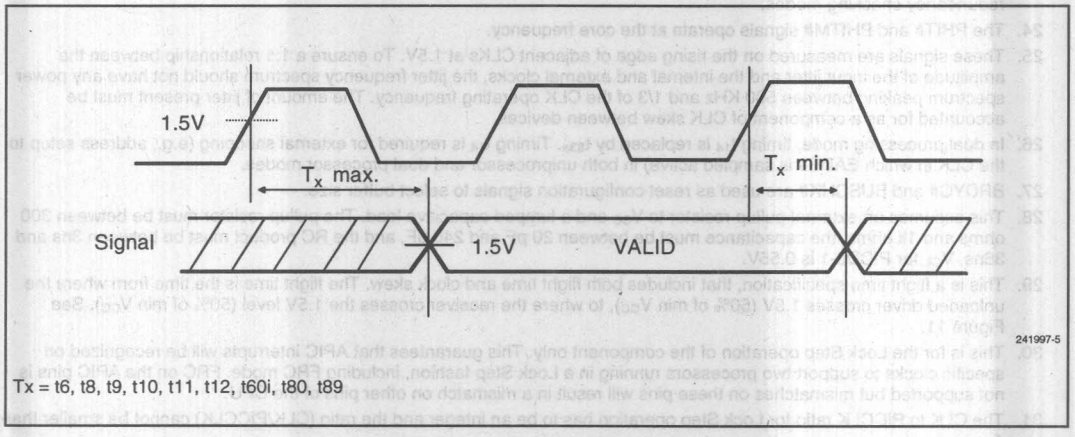
11. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the Pentium processor 75/90/100/120/133/150/166/200 as a primary processor.
12. Setup time is required to guarantee recognition on a specific clock. Pentium processor 75/90/100/120/133/150/166/200 must meet this specification for dual processor operation for the FLUSH# and RESET signals.
13. Hold time is required to guarantee recognition on a specific clock. Pentium processor 75/90/100/120/133/150/166/200 must meet this specification for dual processor operation for the FLUSH# and RESET signals.
14. All TTL timings are referenced from 1.5V.
15. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
16. This input may be driven asynchronously. However, when operating two processors in dual processing mode, FLUSH# and RESET must be asserted synchronously to both processors.
17. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of 2 clocks before being returned active.
18. Timings are valid only when dual processor is present.
19. Maximum time DPEN# is valid from rising edge of RESET.
20. Minimum time DPEN# is valid after falling edge of RESET.
21. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
22. BF and CPUTYP should be strapped to V_{CC} or V_{SS}.
23. RESET is synchronous in dual processing mode and functional redundancy checking mode. All signals which have a setup or hold time with respect to a falling or rising edge of RESET in UP mode, should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing and functional redundancy checking modes.
24. The PHIT# and PHITM# signals operate at the core frequency.
25. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
26. In dual processing mode, timing t_{14} is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
27. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
28. This assumes an external pullup resistor to V_{CC} and a lumped capacitive load. The pullup resistor must be between 300 ohms and 1k ohms, the capacitance must be between 20 pF and 240 pF, and the RC product must be between 3ns and 36ns. V_{OL} for PICD0-1 is 0.55V.
29. This is a flight time specification, that includes both flight time and clock skew. The flight time is the time from where the unloaded driver crosses 1.5V (50% of min V_{CC}), to where the receiver crosses the 1.5V level (50% of min V_{CC}). See Figure 11.
30. This is for the Lock Step operation of the component only. This guarantees that APIC interrupts will be recognized on specific clocks to support two processors running in a Lock Step fashion, including FRC mode. FRC on the APIC pins is not supported but mismatches on these pins will result in a mismatch on other pins of the CPU.
31. The CLK to PICCLK ratio for Lock Step operation has to be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4.

* Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer models to account for signal flight time delays.



Tv = t5, t49, t60e; Tw = t4, t48, t60f; Tx = t3, t47, t60d
Ty = t1, t45, t60b; Tz = t2, t46, t60c

Figure 4. Clock Waveform



Tx = t6, t8, t9, t10, t11, t12, t60i, t80, t89

Figure 5. Valid Delay Timings

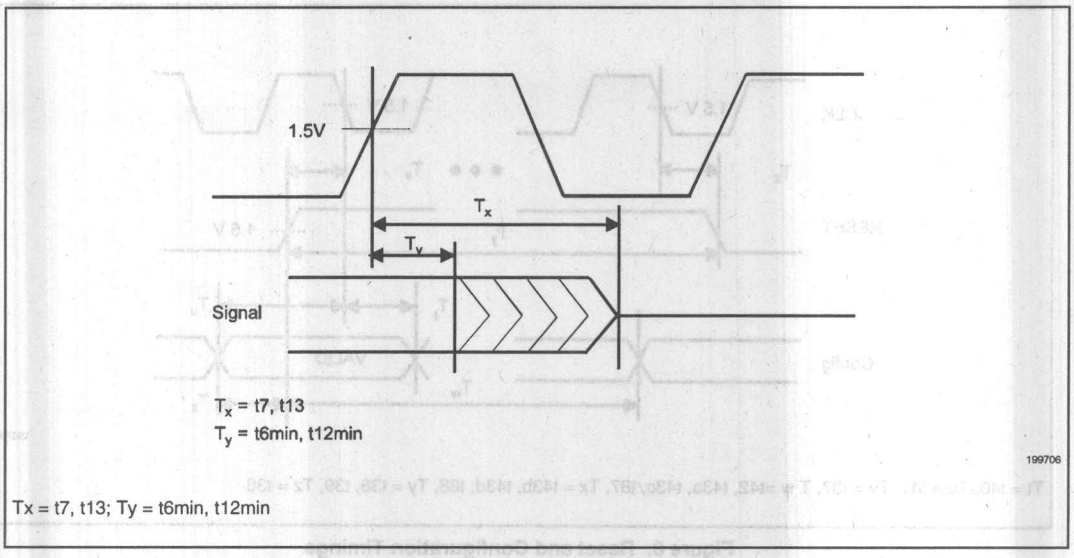


Figure 6. Float Delay Timings

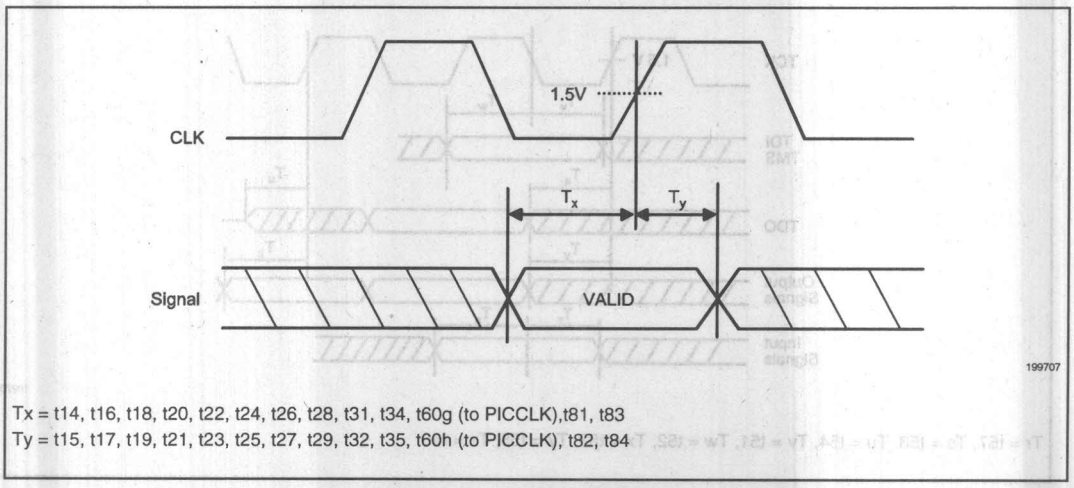
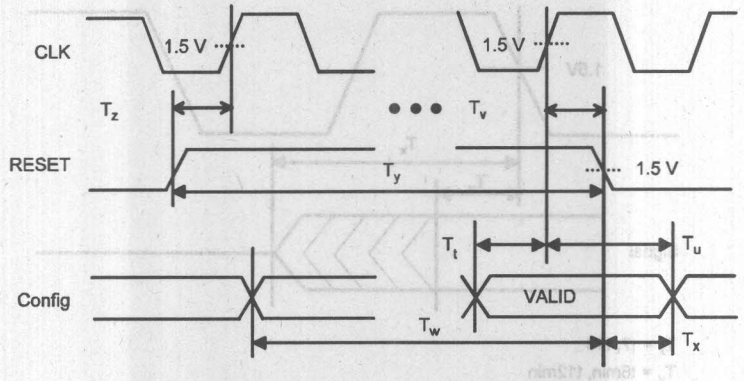
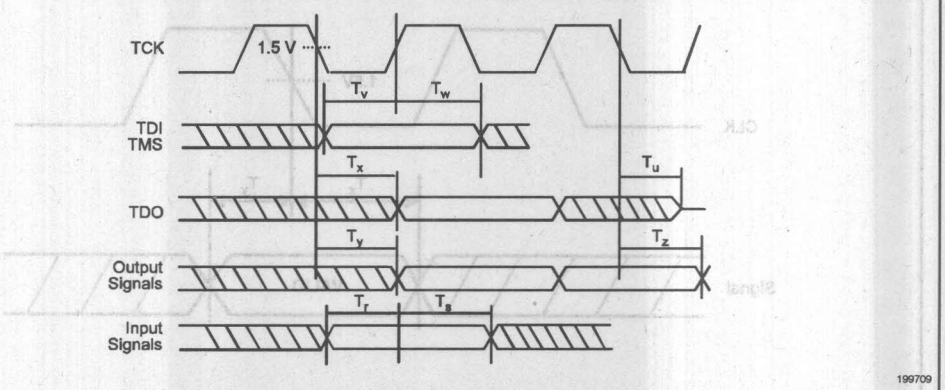


Figure 7. Setup and Hold Timings



Tt = t40, Tu = t41, Tv = t37, T w =t42, t43a, t43c, t87, Tx = t43b, t43d, t88, Ty = t38, t39, Tz = t36

Figure 8. Reset and Configuration Timings



Tr = t57, Ts = t58, Tu = t54, Tv = t51, Tw = t52, Tx = t53, Ty = t55, Tz = t56

Figure 9. Test Timings

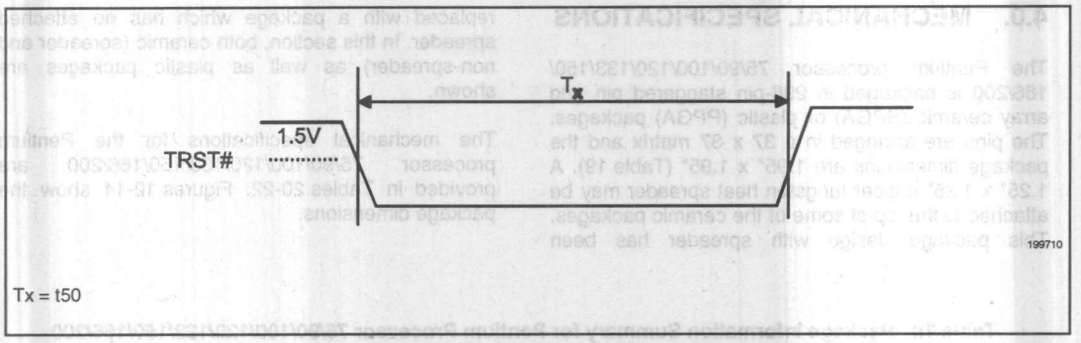


Figure 10. Test Reset Timings

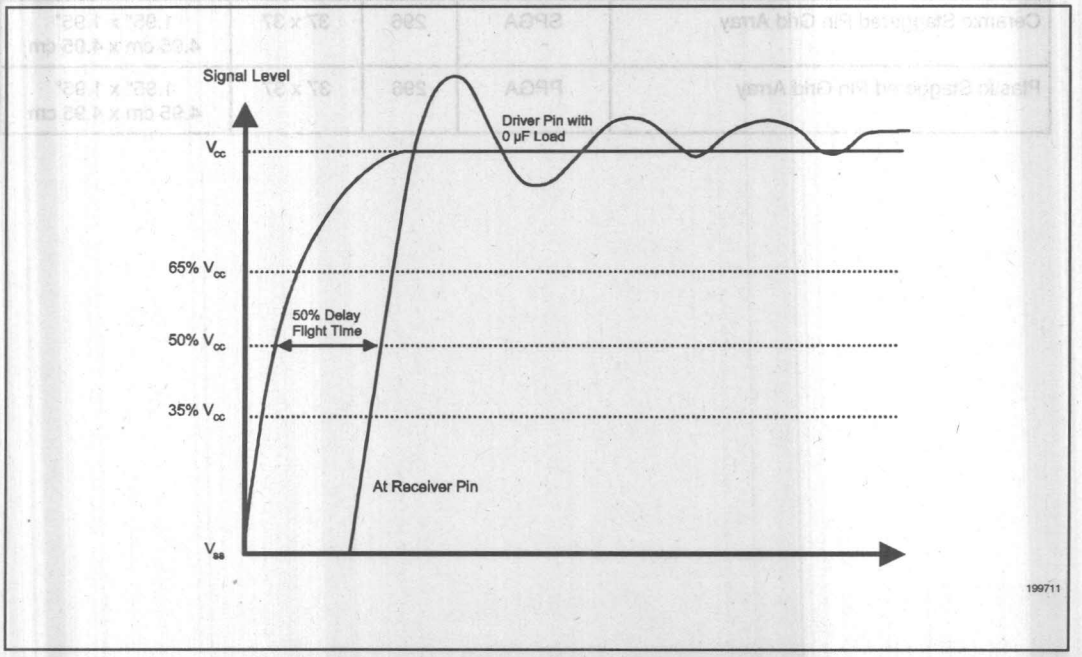


Figure 11. 50% V_{CC} Measurement of Flight Time

4.0. MECHANICAL SPECIFICATIONS

The Pentium processor 75/90/100/120/133/150/166/200 is packaged in 296-pin staggered pin grid array ceramic (SPGA) or plastic (PPGA) packages. The pins are arranged in a 37 x 37 matrix and the package dimensions are 1.95" x 1.95" (Table 19). A 1.25" x 1.25" copper tungsten heat spreader may be attached to the top of some of the ceramic packages. This package design with spreader has been replaced with a package which has no attached spreader. In this section, both ceramic (spreader and non-spreader) as well as plastic packages are shown.

The mechanical specifications for the Pentium processor 75/90/100/120/133/150/166/200 are provided in Tables 20-22. Figures 12-14 show the package dimensions.

Table 19. Package Information Summary for Pentium Processor 75/90/100/120/133/150/166/200

Package Type		Total Pins	Pin Array	Package Size
Ceramic Staggered Pin Grid Array	SPGA	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm
Plastic Staggered Pin Grid Array	PPGA	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

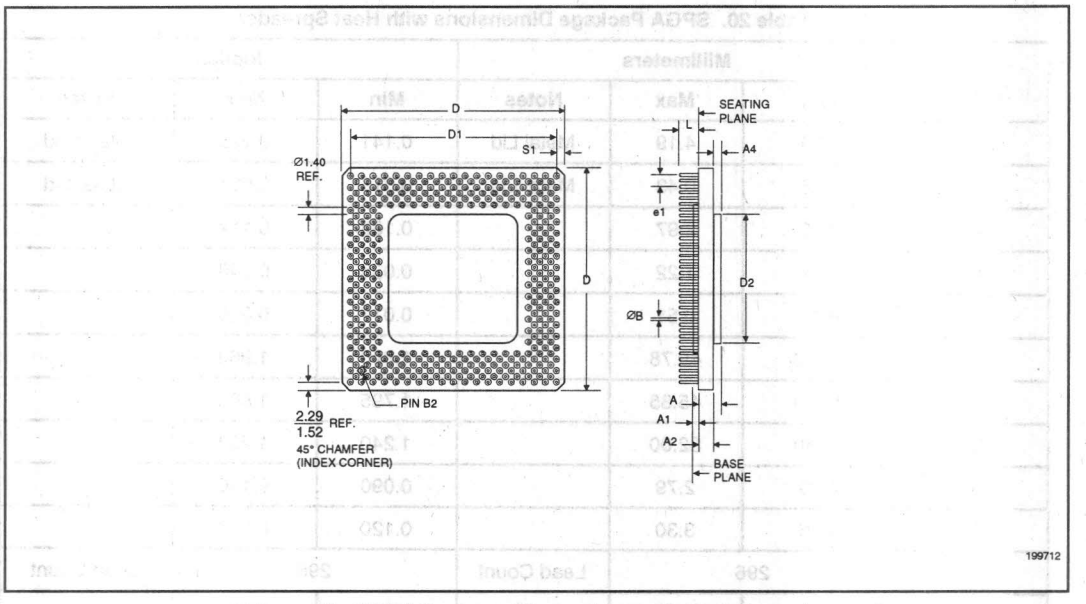


Figure 12. SPGA Package Dimensions with Heat Spreader

B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
D_2	31.50	32.00		1.240	1.260	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

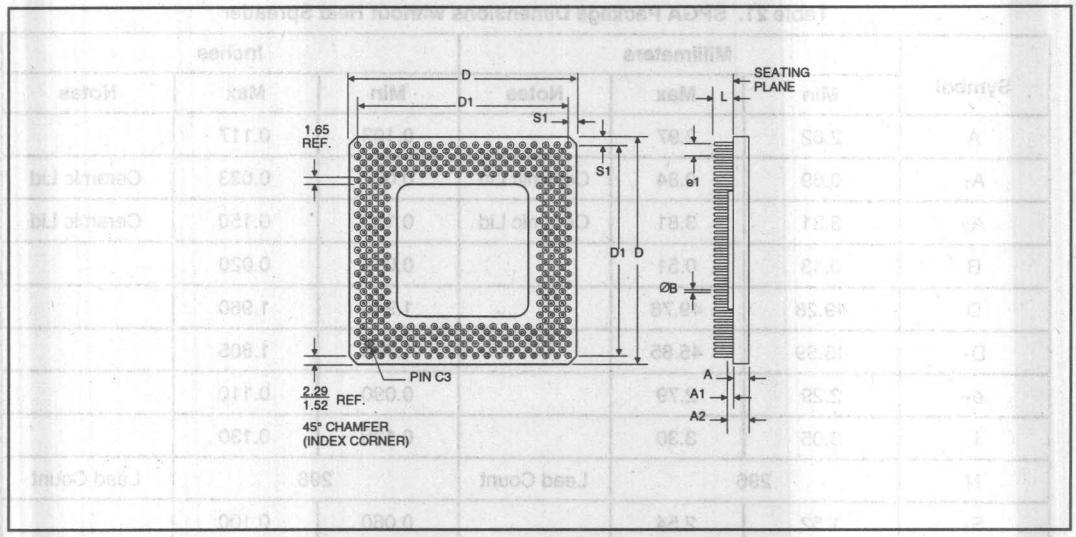


Figure 13. SPGA Package Dimensions without Heat Spreader

Table 21. SPGA Package Dimensions without Heat Spreader

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.62	2.97		0.103	0.117	
A_1	0.69	0.84	Ceramic Lid	0.027	0.033	Ceramic Lid
A_2	3.31	3.81	Ceramic Lid	0.130	0.150	Ceramic Lid
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

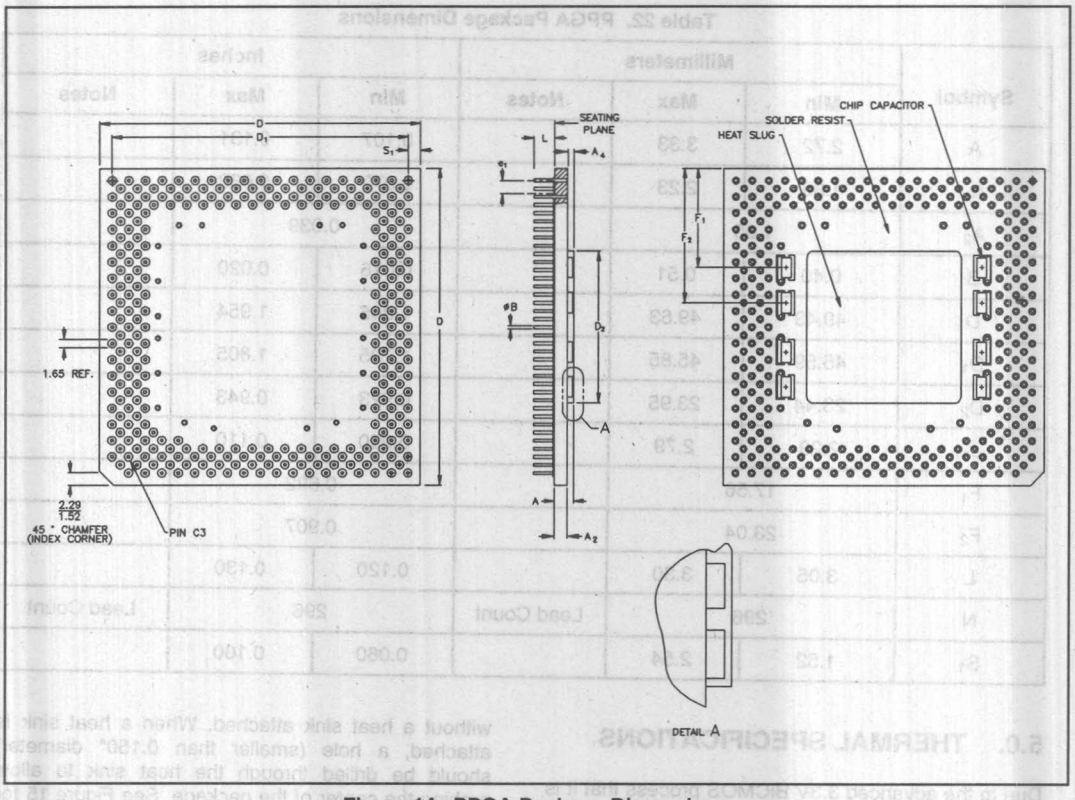


Figure 14. PPGA Package Dimensions

Table 22. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.72	3.33		0.107	0.131	
A_1	1.83	2.23		0.072	0.088	
A_2	1.00			0.039		
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D_1	45.59	45.85		1.795	1.805	
D_2	23.44	23.95		0.923	0.943	
e_1	2.29	2.79		0.090	0.110	
F_1	17.56			0.692		
F_2	23.04			0.907		
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

5.0. THERMAL SPECIFICATIONS

Due to the advanced 3.3V BiCMOS process that it is produced on, the Pentium processor 75/90/100/120/133/150/166/200 dissipates less power than the Pentium processor 60/66 .

The Pentium processor 75/90/100/120/133/150/166/200 is specified for proper operation when case temperature, T_{CASE}, (T_C) is within the specified range of 0°C to 70°C.

5.1. Measuring Thermal Values

To verify that the proper T_C (case temperature) is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heat sink attached. When a heat sink is attached, a hole (smaller than 0.150" diameter) should be drilled through the heat sink to allow probing the center of the package. See Figure 15 for an illustration of how to measure T_C.

To minimize the measurement errors, it is recommended to use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number: OB-100).

θ_{JC} =	junction-to-case thermal resistance. (ºC/Watt)
P =	maximum power consumption (Watt)

Tables 23-26 list the θ_{CA} values for the Pentium processor 75/90/100/120/133/150/166/200 with passive heat sinks. Figures 16-17 show Tables 23-24 in graphic format.

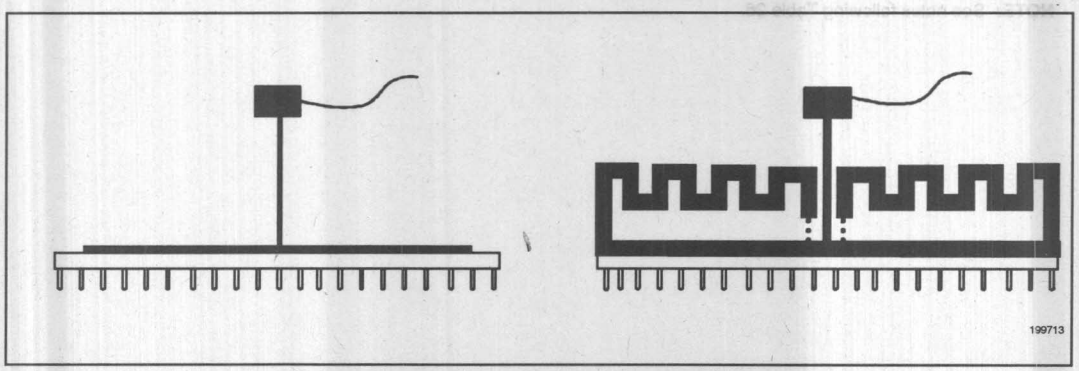


Figure 15. Technique for Measuring T_C*

*Though the figure shows the package with a heat spreader, the same technique applies to measuring T_C of the package without a heat spreader.

Table 23. Thermal Resistances for SPGA Packages with Heat Spreader

Heat Sink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.8	8.7	7.6	6.2	4.0	3.2	2.6
0.35	0.8	8.4	7.1	5.6	3.6	2.9	2.4
0.45	0.8	8.0	6.6	4.9	3.2	2.5	2.1
0.55	0.8	7.7	6.1	4.3	2.8	2.2	1.9
0.65	0.8	7.3	5.6	3.9	2.6	2.0	1.7
0.80	0.8	6.6	4.9	3.5	2.2	1.8	1.6
1.00	0.8	5.9	4.2	3.2	2.2	1.7	1.4
1.20	0.8	5.5	3.9	2.9	2.0	1.6	1.4
1.40	0.8	5.0	3.5	2.6	1.8	1.5	1.3
Without Heat Sink	1.3	11.4	10.5	8.7	5.7	4.5	3.8

NOTE: See notes following Table 26.

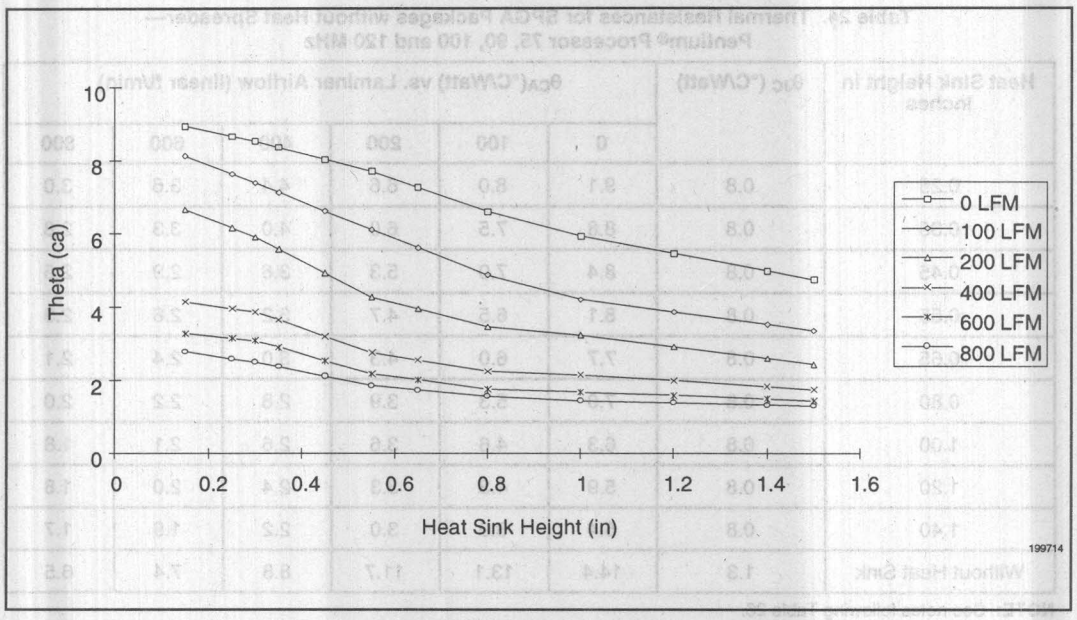


Figure 16. Thermal Resistance vs. Heatsink Height, SPGA Packages with Heat Spreader

0.55	0.8	8.1	6.5	4.7	3.2	2.6	2.3
0.65	0.8	7.7	6.0	4.3	3.0	2.4	2.1
0.80	0.8	7.0	5.3	3.9	2.8	2.2	2.0
1.00	0.8	6.3	4.6	3.6	2.6	2.1	1.8
1.20	0.8	5.9	4.3	3.3	2.4	2.0	1.8
1.40	0.8	5.4	3.9	3.0	2.2	1.9	1.7
Without Heat Sink	1.3	14.4	13.1	11.7	8.8	7.4	6.5

NOTE: See notes following Table 26.

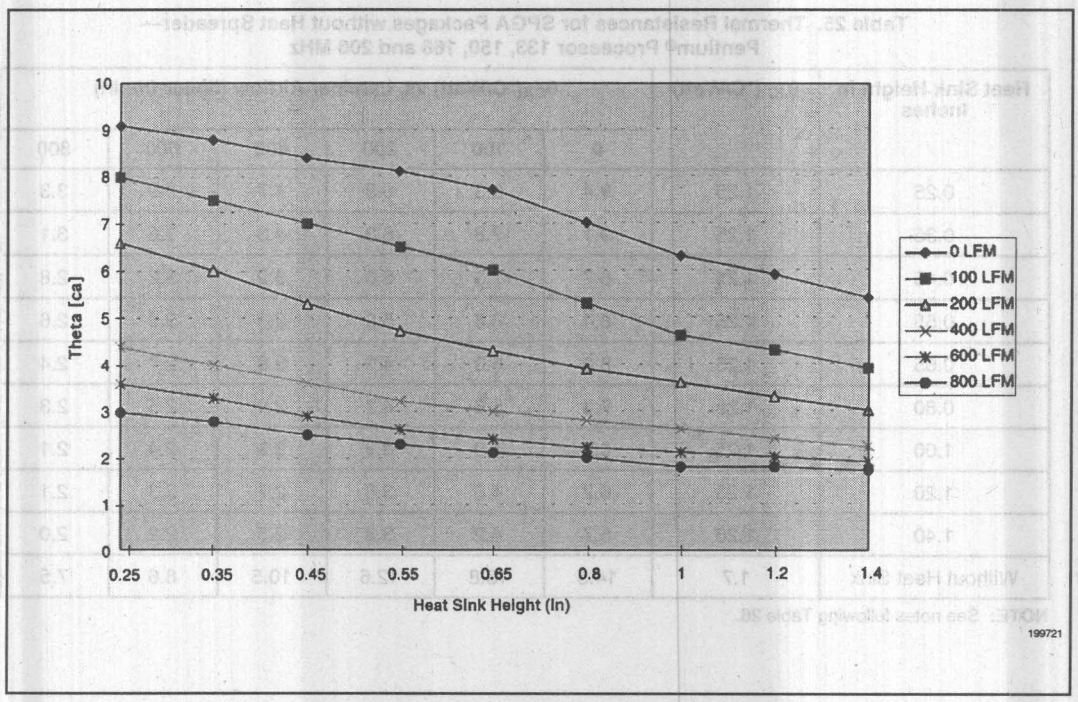


Figure 17. Thermal Resistance vs. Heatsink Height, SPGA Packages without Heat Spreader—Pentium® Processor 75, 90, 100 and 120 MHz

Table 25. Thermal Resistances for SPGA Packages without Heat Spreader—Pentium® Processor 133, 150, 166 and 200 MHz

Heat Sink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	1.25	9.4	8.3	6.9	4.7	3.9	3.3
0.35	1.25	9.1	7.8	6.3	4.3	3.6	3.1
0.45	1.25	8.7	7.3	5.6	3.9	3.2	2.8
0.55	1.25	8.4	6.8	5.0	3.5	2.9	2.6
0.65	1.25	8.0	6.3	4.6	3.3	2.7	2.4
0.80	1.25	7.3	5.6	4.2	2.9	2.5	2.3
1.00	1.25	6.6	4.9	3.9	2.9	2.4	2.1
1.20	1.25	6.2	4.6	3.6	2.7	2.3	2.1
1.40	1.25	5.7	4.2	3.3	2.5	2.2	2.0
Without Heat Sink	1.7	14.5	13.8	12.6	10.5	8.6	7.5

NOTE: See notes following Table 26.

Table 26. Thermal Resistances for PPGA Packages

Heat Sink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.5	9.0	7.9	6.5	4.3	3.5	2.9
0.35	0.5	8.7	7.4	5.9	3.9	3.2	2.7
0.45	0.5	8.3	6.9	5.2	3.5	2.8	2.4
0.55	0.5	8.0	6.4	4.6	3.1	2.5	2.2
0.65	0.5	7.6	5.9	4.2	2.9	2.3	2.0
0.80	0.5	6.9	5.2	3.8	2.5	2.1	1.9
1.00	0.5	6.2	4.5	3.5	2.5	2.0	1.7
1.20	0.5	5.8	4.2	3.2	2.3	1.9	1.7
1.40	0.5	5.3	3.8	2.9	2.1	1.8	1.6
None	1.3	13.0	12.3	11.4	8.0	6.6	5.7

NOTES:

Heat sinks are omni directional pin aluminum alloy.

Features were based on standard extrusion practices for a given height

Pin size ranged from 50 to 129 mils

Pin spacing ranged from 93 to 175 mils

Based thickness ranged from 79 to 200 mils

Heat sink attach was 0.005" of thermal grease.

Attach thickness of 0.002" will improve performance approximately 0.3°C/Watt

6.0. OverDrive® PROCESSOR SOCKET SPECIFICATION

6.1. Introduction

The OverDrive processors are end-user single chip CPU upgrade products for Pentium processor-based systems. The OverDrive processors will speed up most software applications and are binary compatible with the Pentium processor.

6.2. Socket 5

Two upgrade sockets have been defined for the Pentium processor-based systems as part of the processor architecture. Socket 5 has been defined for Pentium processor 75, 90, 100, and 120 MHz-based systems and is defined in the *Pentium® Processor Family Developer's Manual*, Volume 1. Socket 5 does not support upgradability for 133 MHz or higher processors.

Socket 5 supports the following upgrades:

Original Processor	OverDrive® Processor
Pentium® processor 75 MHz at iCOMP® index 2.0 rating 67	125 MHz
Pentium processor 90 MHz at iCOMP index 2.0 rating 81	150 MHz
Pentium Processor 100 MHz at iCOMP index 2.0 rating 90	166 MHz
Pentium Processor 120 MHz at iCOMP index 2.0 rating 100	180 MHz[1]

NOTE:
1. This is a future OverDrive® upgrade processor.

6.3. Socket 7

Socket 7 has been defined as the upgrade socket for the Pentium processor 133, 150, 166 and 200 MHz in addition to the Pentium processor 75, 90, 100, and 120 MHz. The flexibility of the Socket 7 definition makes it backward compatible with Socket 5 and should be used for all new Pentium processor-based system designs. The Socket 7 support requires minor changes from Socket 5 designs – an additional key pin, 3.3V clocks, additional supply current, etc. Contact Intel for further information regarding the Socket 7 specifications.

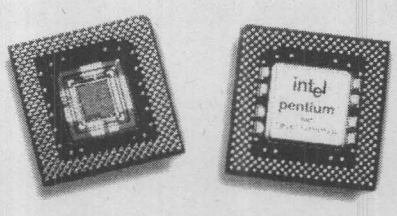
In addition to supporting all of the OverDrive processors for Socket 5, Socket 7 supports the following CPU upgrades:

Original Processor	Future OverDrive® Processor
Pentium® processor 75 MHz at iCOMP® index 2.0 rating 67	150 MHz
Pentium processor 90 MHz at iCOMP index 2.0 rating 81	180 MHz
Pentium processor 120 MHz at iCOMP Index 2.0 rating 100	
Pentium processor 150 MHz at iCOMP index 2.0 rating 114	
Pentium processor 100 MHz at iCOMP index 2.0 rating 90	200 MHz
Pentium processor 133 MHz at iCOMP index 2.0 rating 111	
Pentium processor 166 MHz at iCOMP index 2.0 rating 127	

- Compatible with Large Software Base
  - MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit Processor with 64-Bit Data Bus
- Superscalar Architecture
  - Enhanced Pipelines
  - Two Pipelined Integer Units Capable of Two Instructions per Clock
  - Pipelined MMX Unit
  - Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - 16-Kbyte Code, 16-Kbyte Write Back Data
  - MESI Cache Protocol
- Advanced Design Features
  - Deeper Write Buffers
  - Enhanced Branch Prediction Feature
  - Virtual Mode Extensions
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Dual Processing Configuration
- Internal Error Detection Features
- Multi-Processor Support
  - Multiprocessor Instructions
  - Support for Second Level Cache
- On-Chip Local APIC Controller
  - MP Interrupt Management
  - 8259 Compatible
- Power Management Features
  - System Management Mode
  - Clock Control
- Fractional Bus Operation
  - 233 MHz Core/66 MHz Bus
  - 200 MHz Core/66 MHz Bus
  - 166 MHz Core/66 MHz Bus

The Pentium® processor with MMX™ technology extends the Pentium processor family, providing performance needed for mainstream desktop applications as well as for workstations. The Pentium processor with MMX technology is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2* and UNIX*. The Pentium processor with MMX technology is the first microprocessor to support Intel MMX technology. Furthermore, the Pentium processor with MMX technology superscalar architecture can execute two instructions per clock cycle. Enhanced branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor with MMX technology has 4.5 million transistors and is built on Intel's enhanced CMOS silicon technology.

The Pentium processor with MMX technology may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available on request.



June 1997

Order Number: 243185.004

PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY

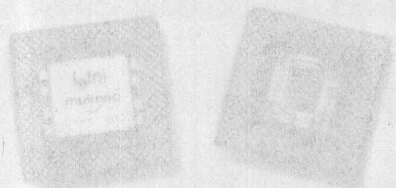
Maximum Operating Frequency	166 MHz	200 MHz	233 MHz
iCOMP® Index 2.0 Rating	180	182	203

NOTE: Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

- Support for MMX™ Technology
- Compatible with Large Software Base
  - MS-DOS®, Windows®, OS/2®, UNIX®
- 32-Bit Processor with 64-Bit Data Bus
- Superscalar Architecture
  - Enhanced Pipelines
  - Two Pipelined Integer Units
    Capable of Two Instructions per Clock
  - Pipelined MMX Unit
  - Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - 16-Kbyte Code, 16-Kbyte Write Back Data
  - MESI Cache Protocol
- Advanced Design Features
  - Deeper Write Buffers
  - Enhanced Branch Prediction Feature
  - Virtual Mode Extensions
- Enhanced CMOS Silicon Technology
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Dual Processing Configuration
- Internal Error Detection Features
- Multi-Processor Support
  - Multiprocessor Instructions
  - Support for Second Level Cache
- On-Chip Local APIC Controller
  - MP Interrupt Management
  - 8259 Compatible
- Power Management Features
  - System Management Mode
  - Clock Control
- Fractional Bus Operation
  - 233 MHz Core/66 MHz Bus
  - 200 MHz Core/66 MHz Bus
  - 166 MHz Core/66 MHz Bus

The Pentium® processor with MMX™ technology extends the Pentium processor family, providing performance needed for mainstream desktop applications as well as for workstations. The Pentium processor with MMX technology is compatible with the entire installed base of applications for MS-DOS®, Windows®, OS/2® and UNIX®. The Pentium processor with MMX technology is the first microprocessor to support Intel MMX technology. Furthermore, the Pentium processor with MMX technology superscalar architecture can execute two instructions per clock cycle. Enhanced branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while maintaining software transparent. The Pentium processor with MMX technology has 4.5 million transistors and is built on Intel's enhanced CMOS silicon technology.

The Pentium processor with MMX technology may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available on request.



June 1997 Order Number 243078-002

1.0. MICROPROCESSOR ARCHITECTURE OVERVIEW

The Pentium® processor with MMX™ technology extends the Intel Pentium family of microprocessors. It is binary compatible with the 8086/88, 80286, Intel386™ DX, Intel386 SX, Intel486™ DX, Intel486 SX, Intel486 DX2 and Pentium processors 60/66/75/90/100/120/133/150/166/200.

The Pentium processor family currently includes the following products.

- Pentium processor with MMX technology:
  - Pentium processor with MMX technology at 233 MHz, iCOMP® Index 2.0 rating = 203
  - Pentium processor with MMX technology at 200 MHz, iCOMP Index 2.0 rating = 182
  - Pentium processor with MMX technology at 166 MHz, iCOMP Index 2.0 rating = 160
- Pentium processor 133/150/166/200. The name "Pentium processor 133/150/166/200" will be used in this document to refer to the Pentium processor with 133, 150, 166 and 200 MHz versions of the Pentium processor:
  - Pentium processor at 200 MHz, iCOMP Index 2.0 rating = 142
  - Pentium processor at 166 MHz, iCOMP Index 2.0 rating = 127
  - Pentium processor at 150 MHz, iCOMP Index 2.0 rating = 114
  - Pentium processor at 133 MHz, iCOMP Index 2.0 rating = 111
  - Pentium processor at 120 MHz, iCOMP Index 2.0 rating = 100
  - Pentium processor at 100 MHz, iCOMP Index 2.0 rating = 90
  - Pentium processor at 90 MHz, iCOMP Index 2.0 rating = 81
  - Pentium processor at 75 MHz, iCOMP Index 2.0 rating = 67

The Pentium processor family supports the features of previous Intel Architecture processors, and provides significant enhancements and additions including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate Code and Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- Dual processing support
- On-chip local APIC device

In addition to the features listed above, the Pentium processor with MMX technology offers the following enhancements over Pentium processor 133/150/166/200:

- Support for Intel MMX technology
- Doubled code and data cache sizes to 16 KB each
- Improved branch prediction
- Enhanced pipeline
- Deeper write buffers

The following features are supported by the Pentium processor 133/150/166/200, but these features are not supported by the Pentium processor with MMX technology:

- Functional redundancy check and Lock Step operation.
- Support for Intel 82498/82493 and 82497/82492 cache chipset products
- Split line accesses to the code cache

For a more detailed description of the Pentium processor family products, please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

1.1. Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 processor family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of processors.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the BTB so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 processor. Faster algorithms provide up to 10X speed-up for common operations including add, multiply and load.

Pentium processors include separate code and data caches are integrated on-chip to meet performance goals. Each cache has a 32-byte line size. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be write back or write through on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are multi-ported to support snooping. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst write back cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' Memory Management Unit contains optional extensions to the architecture which allow 4-Kbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified 4 breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 shows a block diagram of the Pentium processor with MMX technology as a representative of the Pentium processor family.

The block diagram shows the two instruction pipelines, the "u" pipe and the "v" pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

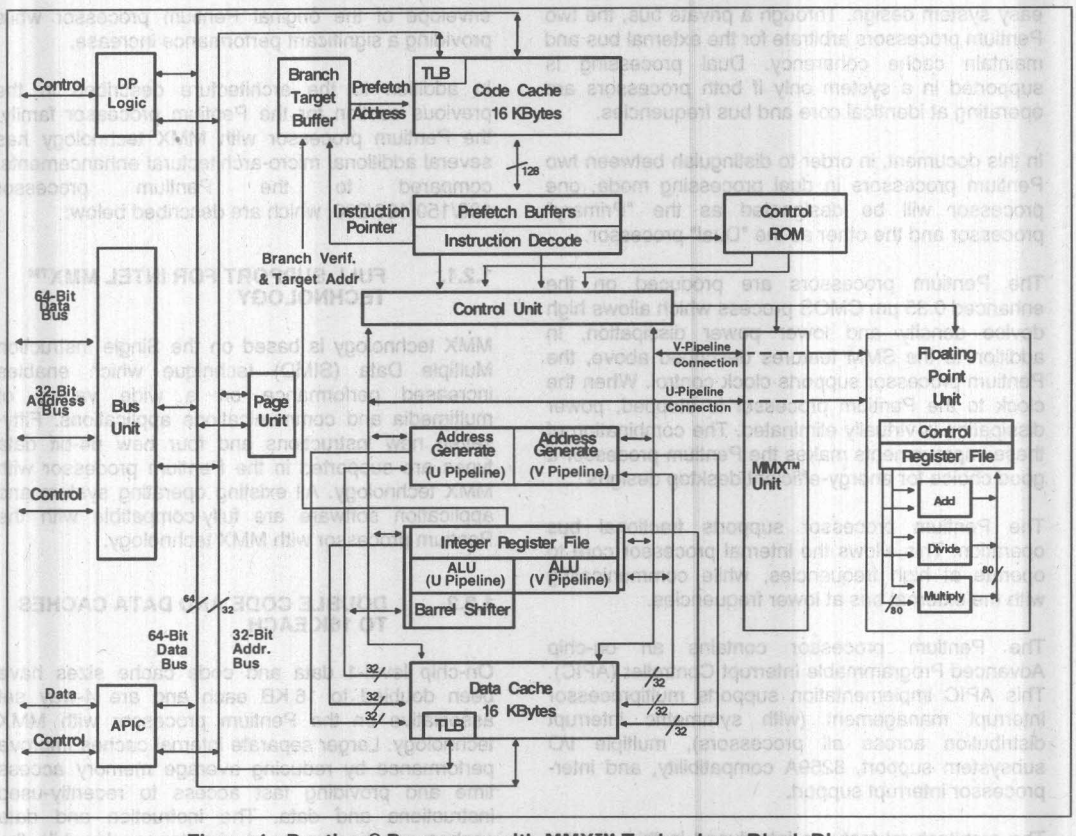


Figure 1. Pentium® Processor with MMX™ Technology Block Diagram

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processors can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

Symmetric dual processing in a system is supported with two Pentium processors. The two processors appear to the system as a single Pentium processor. Operating systems with dual processing support properly schedule computing tasks between the two processors. This scheduling of tasks is transparent to software applications and the end-user. Logic built into the processors support a "glueless" interface for

easy system design. Through a private bus, the two Pentium processors arbitrate for the external bus and maintain cache coherency. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies.

In this document, in order to distinguish between two Pentium processors in dual processing mode, one processor will be designated as the "Primary" processor and the other as the "Dual" processor.

The Pentium processors are produced on the enhanced 0.35 µm CMOS process which allows high device density and lower power dissipation. In addition to the SMM features described above, the Pentium processor supports clock control. When the clock to the Pentium processor is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the Pentium processor a good choice for energy-efficient desktop designs.

The Pentium processor supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The Pentium processor contains an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

The architectural features introduced in this chapter are more fully described in the *Pentium® Processor Family Developer's Manual*(Order Number 241428).

1.2. Pentium® Processor with MMX™ Technology

The Pentium processor with MMX technology is a significant addition to the Pentium processor family. Available at 166, 200 and 233 MHz, it is the first microprocessor to support Intel's MMX technology.

The Pentium processor with MMX technology is both software and pin compatible with previous members of the Pentium processor family. It contains 4.5 million transistors and is manufactured on Intel's enhanced 0.35 micron CMOS process which allows voltage reduction technology for low power and high density. This enables the Pentium processor with MMX technology to remain within the thermal envelope of the original Pentium processor while providing a significant performance increase.

In addition to the architecture described in the previous section for the Pentium processor family, the Pentium processor with MMX technology has several additional micro-architectural enhancements, compared to the Pentium processor 133/150/166/200, which are described below:

1.2.1. FULL SUPPORT FOR INTEL MMX™ TECHNOLOGY

MMX technology is based on the Single Instruction Multiple Data (SIMD) technique which enables increased performance on a wide variety of multimedia and communications applications. Fifty-seven new instructions and four new 64-bit data types are supported in the Pentium processor with MMX technology. All existing operating system and application software are fully-compatible with the Pentium processor with MMX technology.

1.2.2. DOUBLE CODE AND DATA CACHES TO 16K EACH

On-chip level-1 data and code cache sizes have been doubled to 16 KB each and are 4-way set associative on the Pentium processor with MMX technology. Larger separate internal caches improve performance by reducing average memory access time and providing fast access to recently-used instructions and data. The instruction and data caches can be accessed simultaneously while the data cache supports two data references simultaneously. The data cache supports a write-back (or alternatively, write-through, on a line by line basis) policy for memory updates.

1.2.3. IMPROVED BRANCH PREDICTION

Dynamic branch prediction uses the Branch Target Buffer (BTB) to boost performance by predicting the most likely set of instructions to be executed. The BTB has been improved on the Pentium processor with MMX technology to increase its accuracy. Further, the Pentium processor with MMX technology has four prefetch buffers that can hold up to four successive code streams.

1.2.4. ENHANCED PIPELINE

An additional pipeline stage has been added and the pipeline has been enhanced to improve performance.

The integration of the MMX pipeline with the integer pipeline is very similar to that of the floating-point pipeline. Under some circumstances, two MMX instructions or one integer and one MMX instruction can be paired and issued in one clock cycle to increase throughput.

The enhanced pipeline is described in more detail in the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

1.2.5. DEEPER WRITE BUFFERS

A pool of four write buffers is now shared between the dual pipelines to improve memory write performance.

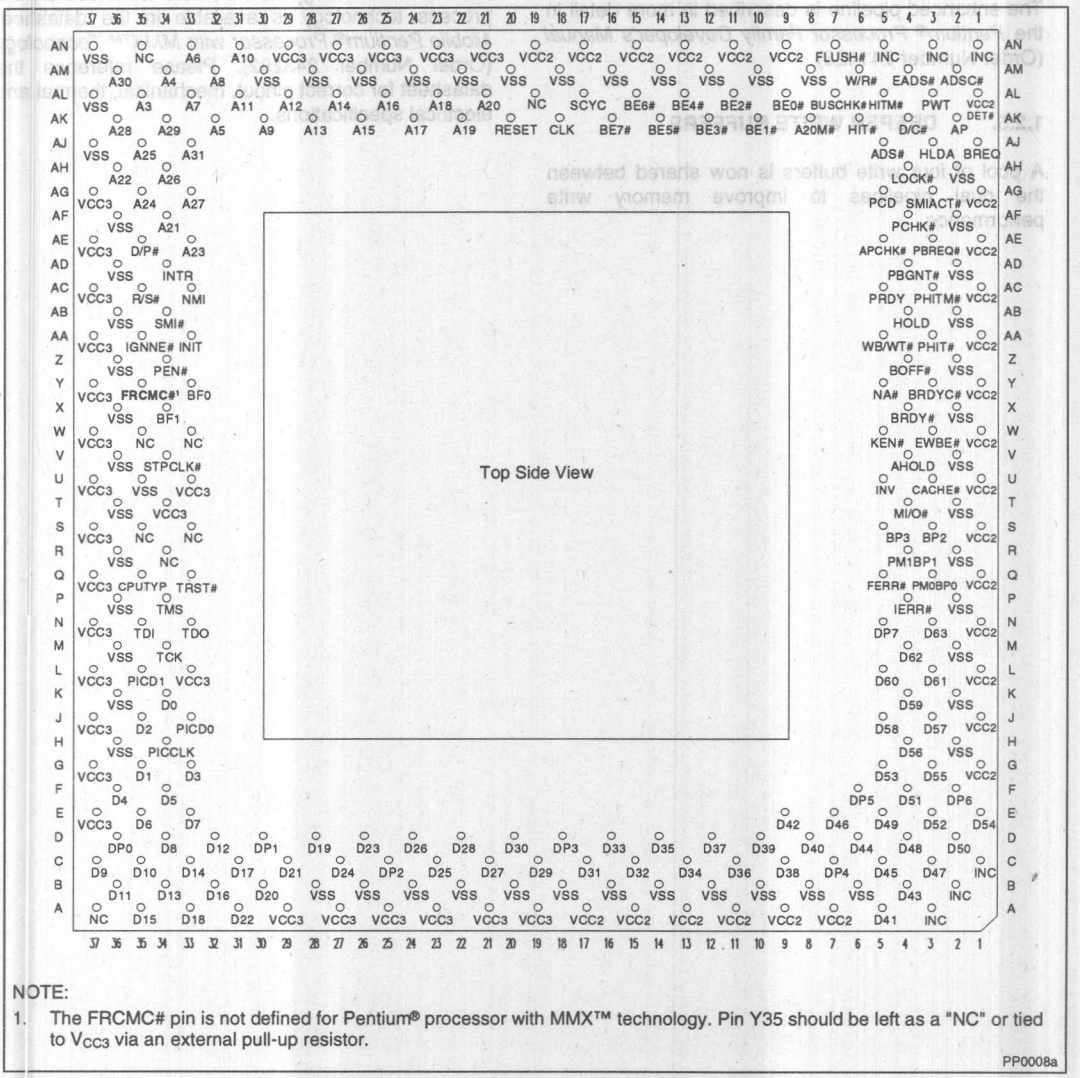
1.3. Mobile Pentium® Processor with MMX™ Technology

Currently, Intel's Mobile Pentium processor with MMX technology family consists of three products. Detailed information on Mobile Pentium processors with MMX technology based on the enhanced CMOS process technology is available in the datasheet *Mobile Pentium® Processor with MMX™ Technology* (Order Number 243292). Please reference the datasheet for correct pinout, mechanical, thermal and electrical specifications.

2.0. PINOUT

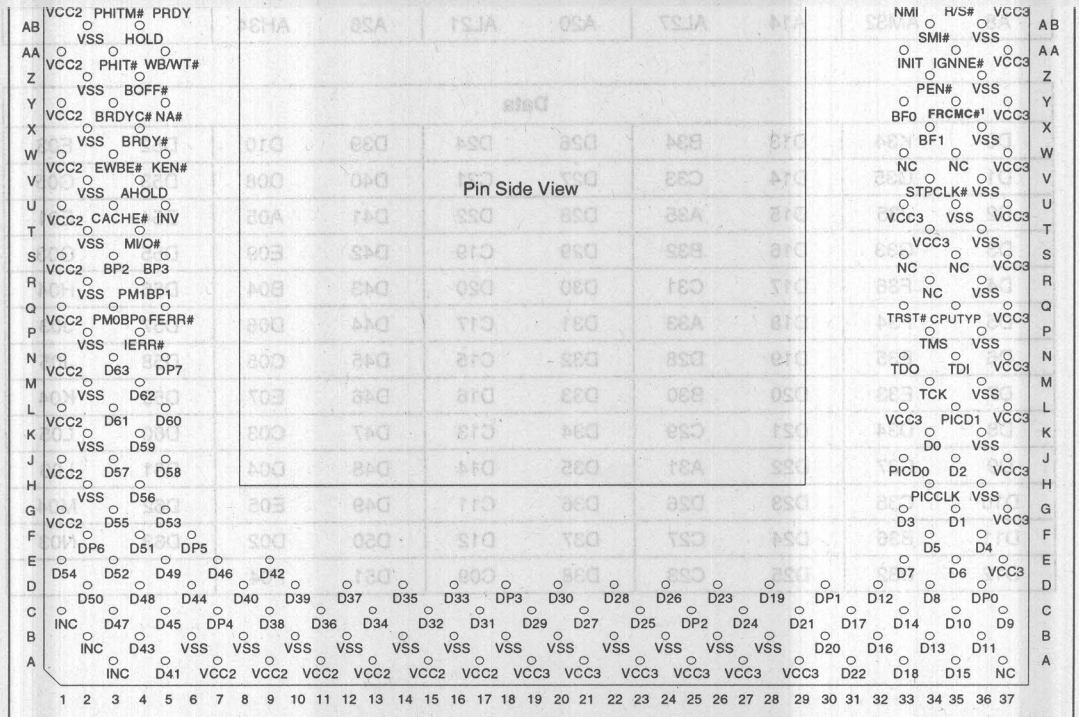
2.1. Pinout and Pin Descriptions

2.1.1. PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY PINOUT



NOTE:
1. The FRCMC# pin is not defined for Pentium® processor with MMX™ technology. Pin Y35 should be left as a "NC" or tied to V_{CC3} via an external pull-up resistor.

Figure 2. Pentium® Processor with MMX™ Technology SPGA and PPGA Package Pinout (Top Side View)



NOTE:

1. The FRCMC# pin is not defined for Pentium® processor with MMX™ technology. Pin Y35 should be left as a "NC" or tied to V_{CC3} via an external pull-up resistor.

PP0009a

Figure 3. Pentium® Processor with MMX™ Technology SPGA and PPGA Package Pinout (Pin Side View)

2.1.2. PIN CROSS-REFERENCE TABLE FOR PENTIUM® PROCESSOR WITH MMX™

Table 1. Pin Cross-Reference by Pin Name (xPGA Package)

Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		

Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 1. Pin Cross-Reference by Pin Name (xPGA Package)(Cont'd)

Control							
A20M#	AK08	BREQ	AJ01	HIT#	AK06	PRDY	AC05
ADS#	AJ05	BUSCHK#	AL07	HITM#	AL05	PWT	AL03
ADSC#	AM02	CACHE#	U03	HLDA	AJ03	R/S#	AC35
AHOLD	V04	CPUTYP	Q35	HOLD	AB04	RESET	AK20
AP	AK02	D/C#	AK04	IERR#	P04	SCYC	AL17
APCHK#	AE05	D/P#	AE35	IGNNE#	AA35	SMI#	AB34
BE0#	AL09	DP0	D36	INIT	AA33	SMIACT#	AG03
BE1#	AK10	DP1	D30	INTR/LINT0	AD34	TCK	M34
BE2#	AL11	DP2	C25	INV	U05	TDI	N35
BE3#	AK12	DP3	D18	KEN#	W05	TDO	N33
BE4#	AL13	DP4	C07	LOCK#	AH04	TMS	P34
BE5#	AK14	DP5	F06	M/IO#	T04	TRST#	Q33
BE6#	AL15	DP6	F02	NA#	Y05	VCC2DET#	AL01
BE7#	AK16	DP7	N05	NMI/LINT1	AC33	W/R#	AM06
BOFF#	Z04	EADS#	AM04	PCD	AG05	WB/WT#	AA05
BP2	S03	EWBE#	W03	PCHK#	AF04		
BP3	S05	FERR#	Q05	PEN#	Z34		
BRDY#	X04	FLUSH#	AN07	PM0/BP0	Q03		
BRDYC#	Y03	FRCMC#[1]	Y35	PM1/BP1	R04		

APIC		Clock Control		Dual Processor Private Interface			
PICCLK	H34 (2)	CLK	AK18 (2)	PBGNT#	AD04		
PICD0	J33	[BF0]	Y33	PBREQ#	AE03		
[DPEN#]		[BF1]	X34	PHIT#	AA03		
PICD1	L35	STPCLK#	V34	PHITM#	AC03		
[APICEN]							

V_{CC2}				
A17	A07	Q01	AA01	AN11
A15	G01	S01	AC01	AN13
A13	J01	U01	AE01	AN15
A11	L01	W01	AG01	AN17
A09	N01	Y01	AN09	AN19

Table 1. Pin Cross-Reference by Pin Name (xPGA Package)(Cont'd)

V_{CC3}						
A19	A27	J37	Q37	U37	AC37	AN27
A21	A29	L37	S37	W37	AE37	AN25
A23	E37	L33	T34	Y37	AG37	AN23
A25	G37	N37	U33	AA37	AN29	AN21

V_{SS}								
B06	B18	H02	P02	U35	Z36	AF36	AM12	AM24
B08	B20	H36	P36	V02	AB02	AH02	AM14	AM26
B10	B22	K02	R02	V36	AB36	AJ37	AM16	AM28
B12	B24	K36	R36	X02	AD02	AL37	AM18	AM30
B14	B26	M02	T02	X36	AD36	AM08	AM20	AN37
B16	B28	M36	T36	Z02	AF02	AM10	AM22	

NC		
A37	S35	AL19
R34	W33	AN35
S33	W35	—

INC					
A03	B02	C01	AN01	AN03	AN05

NOTES:

1. The FRCMC# pin is not defined for the Pentium® processor with MMX™ technology. This pin should be left as a "NC" or tied to V_{CC3} via an external pull-up resistor on the Pentium processor with MMX technology.
2. PICCLK and CLK are 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for the CLK and PICCLK signal quality specification.

2.2. Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to GND.

No Connect (NC) pins must remain unconnected. Connection of NC or INC pins may result in component failure or incompatibility with processor steppings.

2.3. Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the Hardware Interface chapter in the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

NOTE

All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The following pins become I/O pins when two Pentium processors with MMX technology are operating in a dual processing environment:

ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC, BE#4

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor with MMX™ technology emulates the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the Pentium processor with MMX technology when configured as a Dual processor.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the Pentium processor with MMX technology.
ADSC#	O	The **address strobe (copy)** is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium processor with MMX technology will stop driving the address lines (A31-A3) and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium processor with MMX technology with even parity information on all Pentium processor with MMX technology generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium processor with MMX technology during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium processor with MMX technology.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium processor with MMX technology has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
BE7#–BE4# BE3#–BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Additionally, the lower 4-byte enables (BE3#-BE0#) are used on the Pentium processor with MMX technology as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF[1:0]	I	The **bus frequency** pins determine the bus-to-core frequency ratio. BF[1:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[1:0] must not change values while RESET is active. See Table 3 for Bus Frequency Selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium processor with MMX technology will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor with MMX technology restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the**performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium processor with MMX technology data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **burst ready (copy)** is functionally identical to BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium processor with MMX technology has internally generated a bus request. This signal is always driven whether or not the Pentium processor with MMX technology is driving its bus.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor with MMX technology will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor with MMX technology will vector to the machine check exception. **NOTE:** To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For Pentium processor with MMX technology-initiated cycles the**cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor with MMX technology will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the Pentium processor with MMX technology. Its frequency is the operating frequency of the Pentium processor with MMX technology external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for the CLK and PICCLK signal quality specification. **NOTE:** It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the Pentium processor with MMX technology is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC3}.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with MMX technology with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with MMX technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor with MMX technology. DP7 applies to D63-56, DP0 applies to D7-0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# is multiplexed with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium processor with MMX technology address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium processor with MMX technology generates a write, and EWBE# is sampled inactive, the Pentium processor with MMX technology will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked **floating-point** error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type **floating-point** error reporting. FERR# is never driven active by the Dual processor.

		mode is entered. If two Pentium processors with MMX technology are operating in dual processing mode and FLUSH# is asserted, the Dual processor will perform a flush first (without a flush acknowledge cycle), then the Primary processor will perform a flush followed by a flush acknowledge cycle. **NOTE:** If the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
FRCMC#	I	Functional Redundancy Checking is not supported on thePentium processor with MMX technology. The FRCMC# pin is not defined for the Pentium processor with MMX technology. This pin should be left as a"NC" or tied to V_{CC3} via an external pull-up resistor.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor with MMX technology data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium processor with MMX technology cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor with MMX technology has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor with MMX technology will resume driving the bus. If the Pentium processor with MMX technology has a bus cycle pending, it will be driven one clock cycle after HLDA is de-asserted.
HOLD	I	In response to the **bus hold request**, the Pentium processor with MMX technology will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor with MMX technology will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium processor with MMX technology will recognize HOLD during reset.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium processor with MMX technology will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor with MMX technology will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor with MMX technology will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor with MMX technology will stop execution and wait for an external interrupt. IGNNE# is internally masked when the Pentium processor with MMX technology is configured as a Dual processor.
INIT	I	The Pentium processor with MMX technology **initialization** input pin forces the Pentium processor with MMX technology to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the Pentium processor with MMX technology will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor with MMX technology will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized. If the local APIC is enabled, this pin becomes LINT0.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium processor with MMX technology generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
LINT0/INTR	I	If the APIC is enabled, this pin is **local interrupt 0**. If the APIC is disabled, this pin is INTR.
LINT1/NMI	I	If the APIC is enabled, this pin is **local interrupt 1**. If the APIC is disabled, this pin is NMI.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor with MMX technology will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor with MMX technology will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium processor with MMX technology supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. If the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processors with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processor with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors with MMX technology are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor with MMX technology will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium processor with MMX technology will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PHITM#	I/O	**Private modified hit** is a hit on a modified cache line indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor with MMX technology. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for the CLK and PICCLK signal quality specification.
PICD0-1 [DPEN#] [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals are multiplexed with DPEN# and APICEN respectively.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin is provided for use with the Intel debug port. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for more details.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for more details.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
RESET	I	**RESET** forces the Pentium processor with MMX technology to begin execution at a known state. All the Pentium processor with MMX technology internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if Built-In Self-Test (BIST) will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with MMX technology, thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium processor with MMX technology will still respond to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the Pentium processor with MMX technology boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium processor with MMX technology during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium processor with MMX technology on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor with MMX technology on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC2}	I	The Pentium processor with MMX technology has 25 2.8V **power** inputs.
V_{CC3}	I	The Pentium processor with MMX technology has 28 3.3V **power** inputs.
V_{CC2}DET#	O	**V_{CC2} detect** is used in flexible motherboard implementations to configure the voltage output set-point appropriately for the V_{CC2} inputs of the processor.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
V_{SS}	I	The Pentium processor with MMX technology has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

Core and bus frequencies can be set according to Table 3 below. Each Pentium processor with MMX technology specified to operate within a single bus-to-core ratio and a specific minimum to maximum bus frequency range (corresponding to a minimum to maximum core frequency range). Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported. For example, the 166 MHz Pentium processor with MMX technology does not operate beyond the 66 MHz bus frequency and only supports the 2/5 bus-to-core ratio; it does not support the 1/3, 1/2, or 2/3 bus-to-core ratios. Table 3 clarifies and summarizes these specifications.

Table 3. Bus Frequency Selections

BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)	Min Bus/Core Frequency (MHz)
0	1	1/3	66/200	33/100
0	0	2/5	66/166	33/83
1	0	1/2 (1, 2)	N/A (2)	N/A (2)
1	1	2/7	66/233	33/117

NOTES:

1. This is the default bus to core ratio for the Pentium® processor with MMX™ technology. If the BF pins are left floating, the processor will be configured for the 1/2 bus to core frequency ratio.
2. Currently, there are no products that support these bus fractions.

2.4. Pin Reference Tables

Table 4. Output Pins

Name	Active Level	When Floated
ADS# (1)	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE4#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE# (1)	Low	Bus Hold, BOFF#
D/P# (2)	N/A	
FERR# (2)	Low	
HIT# (1)	Low	
HITM# (1, 3)	Low	
HLDA (1)	High	
IERR#	Low	
LOCK# (1)	Low	Bus Hold, BOFF#
M/IO# (1), D/C# (1), W/R# (1)	N/A	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC (1)	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	N/A	All states except Shift-DR and Shift-IR
V_{CC}2DET#	Low	

NOTES:
All output and input/output pins are floated during tristate test mode (except IERR#).
1. These are I/O signals when two Pentium® processor with MMX™ technology are operating in dual processing mode.
2. These signals are undefined when the processor is configured as a Dual processor.
3. M# pin has an internal pull-up resistor.

Table 5. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M# (1)	Low	Asynchronous		
AHOLD	High	Synchronous		
APICEN	High	Synchronous/RESET	Pull-up	
BF0	N/A	Synchronous/RESET	Pull-down	
BF1	N/A	Synchronous/RESET	Pull-up	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pull-up	Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pull-up	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pull-up	BRDY#
CLK	N/A			
CPUTYP	High	Synchronous/RESET	Pull-down	
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE# (1)	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
LINT[1:0]	High	Asynchronous		APICEN at RESET
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2, TD, T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pull-up	
R/S#	N/A	Asynchronous	Pull-up	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pull-up	
STPCLK#	Low	Asynchronous	Pull-up	
TCK	N/A		Pull-up	
TDI	N/A	Synchronous/TCK	Pull-up	TCK
TMS	N/A	Synchronous/TCK	Pull-up	TCK
TRST#	Low	Asynchronous	Pull-up	
WB/WT#	N/A	Synchronous		First BRDY#/NA#

NOTES:

1. Undefined when the processor is configured as a Dual processor.

DP7-DP0	N/A	Bus Hold, BOFF#	BRDY#	
DPEN#	low		RESET	Pull-up
PICD0	N/A			Pull-up
PICD1	N/A			Pull-down

NOTES:

1. All output and input/output pins are floated during tristate test mode (except TDO, IERR# and TDO).
2. BE3#-BE0# have Pull-downs during RESET only.

Table 7. Inter-Processor Input/Output Pins

Name	Active Level	Internal Resistor
PHIT#	Low	Pull-up
PHITM#	Low	Pull-up
PBGNT#	Low	Pull-up
PBREQ#	Low	Pull-up

NOTES:

For proper inter-processor operation, the system cannot load these signals.

2.5. Pin Grouping According to Function

Table 8 organizes the pins with respect to their function.

Table 8. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF1–BF0
Address Bus	A31-A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0-1
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Debugging	R/S#, PRDY
Voltage Detection	VCC2DET#

3.0. ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium processor with MMX technology and the Pentium processor 133/150/166/200, as well as the AC and DC specifications of the Pentium processor with MMX technology.

3.1. Electrical Characteristics and Differences between the Pentium® Processor with MMX™ Technology and the Pentium Processor 133/150/166/200

When designing a Pentium processor with MMX technology system from a Pentium processor 133/150/166/200 system, there are a number of electrical differences that require attention. Designing a single motherboard that supports various members of the Pentium processor family including the Pentium processor with MMX technology, Pentium processor 133/150/166/200, Pentium OverDrive® processor, or future Pentium OverDrive processor can be easily accomplished. Refer to the *Pentium® Processor Flexible Motherboard Design Guidelines* application note (Order Number 243187) for more information and specific implementation examples.

The following sections highlight key electrical issues pertaining to the Pentium processor with MMX technology power supplies, connection specifications and buffer models.

3.1.1. POWER SUPPLIES

The main electrical difference between the Pentium processor with MMX technology and the Pentium processor 133/150/166/200 is the operating voltage. The Pentium processor with MMX technology requires two separate voltage inputs, V_{CC2} and V_{CC3}. The V_{CC2} pins supply power to the Pentium processor with MMX technology core, while the V_{CC3} pins supply power to the processor I/O pins.

The Pentium processor 133/150/166/200, on the other hand, requires a single voltage supply for all V_{CC} pins. This single supply powers both the core and I/O pins of the Pentium processor 133/150/166/200.

By connecting all of the V_{CC2} pins together and all the V_{CC3} pins together on separate power islands, Pentium processor 133/150/166/200 designs can easily be converted to support the Pentium processor with MMX technology. In order to maintain compatibility with Pentium processor 133/150/166/200-based platforms, the Pentium processor with MMX technology supports the standard 3.3V specification on its V_{CC3} pins.

3.1.1.1. Power Supply Sequencing

There is no specific power sequence required for powering up or powering down the separate V_{CC2} and V_{CC3} supplies of the Pentium processor with MMX technology. It is recommended that the V_{CC2} and V_{CC3} supplies be either both ON or both OFF within one second of each other.

3.1.2. CONNECTION SPECIFICATIONS

Connection specifications for the power and ground inputs, 3.3V inputs and outputs, and the NC/INC and unused inputs are discussed in the following sections.

3.1.2.1. Power and Ground

For clean on-chip power distribution, the Pentium processor with MMX technology in PPGA and SPGA packages has 28 V_{CC3} (I/O power), 25 V_{CC2} (core power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium processor with MMX technology. On the circuit board all V_{CC3} pins must be connected to a 3.3V V_{CC} plane. All V_{CC2} pins must be connected to a 2.8V V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

3.1.2.1.1. V_{CC2} and V_{CC3} Measurement Specification

The values of V_{CC2} and V_{CC3} should be measured at the bottom side of the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 MS/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board.

The measurement should be taken at the following V_{CC}/V_{SS} pairs: AN13/AM10, AN21/AM18, AN29/AM26, AC37/Z36, U37/R36, L37/H36, A25/B28, A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2. One-half of these pins are V_{CC2} while the others are V_{CC3}; the operating ranges for the V_{CC2} and V_{CC3} pins are

specified at different voltages. See Table 10 for the specification.

The display should show continuous sampling of the voltage line, at 20 mV/div, and 500 ns/div with the trigger point set to the center point of the range. Slowly move the trigger to the high and low ends of the specification, and verify that excursions beyond these limits are not observed. There are no allowances for crossing the high and low limits of the voltage specification. For more information on measurement techniques, see the *Voltage Guidelines for Pentium® Processors with MMX™ Technology* application note (Order Number 243186).

3.1.2.1.2. Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Pentium processor with MMX technology. The Pentium processor with MMX technology, when driving its large address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Pentium processor with MMX technology and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

For the Pentium processor with MMX technology, the power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant State. Another example would be executing a HALT instruction, causing the Pentium processor with MMX technology to enter the AutoHALT Power Down State, or transitioning from HALT to the Normal State. All of these examples may cause abrupt changes in the power being consumed by the Pentium processor with MMX technology. Note that the AutoHALT Power Down feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low Effective Series Resistance (ESR) in the 10Ω to 100Ω range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the Pentium processor with MMX technology on both the V_{CC2} and V_{CC3} plane to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

Detailed decoupling recommendations are provided in the Flexible Motherboard Design Guidelines application note (Order Number 243187)

3.1.2.2. 3.3V Inputs and Outputs

The inputs and outputs of the Pentium processor with MMX technology comply with the 3.3V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the V_{IN3} (max) specification.

System support components which use TTL-compatible inputs will interface to the Pentium processor with MMX technology without extra logic. This is because the Pentium processor drives according to the 5V TTL specification (but not beyond 3.3V).

For Pentium processor with MMX technology inputs, the voltage must not exceed the 3.3V V_{IN3} (max) specification. System support components can consist of 3.3V devices or open-collector devices. In an open-collector configuration, the external resistor should be biased to V_{CC3}.

All pins, including the CLK and PICCLK of the Pentium processor with MMX technology, are 3.3V-tolerant-only. If an 8259A interrupt controller is used, for example, the system must provide level converters between the 8259A and the Pentium processor with MMX technology.

3.1.2.3. NC/INC and Unused Inputs

All NC and INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to V_{SS} (ground).

3.1.2.4. Private Bus

When two Pentium processors with MMX technology are operating in dual processor mode, a "private bus" exists to arbitrate for the processor bus and maintain local cache coherency. The private bus consists of two pinout changes:

1. Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
2. Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC, BE#4.

The new pins are given AC specifications of valid delays at 0 pF, setup times and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must only be met when a dual processor is present in the system.

3.1.3. BUFFER MODELS

The structure of the buffer models for the Pentium processor with MMX technology and the Pentium processor 133/150/166/200 are identical. Some of the values of the components have changed to reflect the minor manufacturing process and package differences between the processors. The system should see insignificant differences between the AC behavior of the Pentium processor with MMX technology and the Pentium processor 133/150/166/200.

Simulation of AC timings using the Pentium processor with MMX technology buffer models is recommended to ensure robust system designs. Pay specific attention to the signal quality restrictions imposed by 3.3V buffers.

3.2. Absolute Maximum Ratings

Table 9 provides stress ratings only. Functional operation at the Absolute Maximum Ratings is not implied or guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with MMX technology contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
	Storage Temperature	–65	150	°C	
	Case Temperature Under Bias	–65	110	°C	
V_{CC3}	V_{CC3} Supply Voltage with respect to V_{SS}	–0.5	4.6	V	
V_{CC2}	V_{CC2} Supply Voltage with respect to V_{SS}	–0.5	3.7	V	
V_{IN3}	3V Only Buffer DC Input Voltage	–0.5	V_{CC3} +0.5 (not to exceed V_{CC3} max)	V	

WARNING

Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the DC specifications is not recommended or guaranteed and extended exposure beyond the DC specifications may affect device reliability.

3.3. DC Specifications

Table 10 and Table 11 list the DC Specifications of the Pentium processor with MMX technology.

Table 10. V_{CC} and T_{CASE} Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Notes
T_{CASE}	Case Temperature	0		70	°C	
V_{CC2}	V_{CC2} Voltage	2.7	2.8	2.9	V	Range = 2.8 ± 3.57%(1)
V_{CC3}	V_{CC3} Voltage	3.135	3.3	3.6	V	Range = 3.3 –5%, +9.09% (1)

NOTES:

1. See the V_{CC} measurement specification section earlier in this chapter.

Table 11. 3.3V DC Specifications
(See Table 10 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level
V_{IH3}	Input High Voltage	2.0	V_{CC3} +0.3	V	TTL Level (3)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1, 4)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (2)

NOTES:

1. Parameter measured at –4 mA.
2. Parameter measured at 3 mA.
3. Parameter measured at nominal V_{CC3} which is 3.3V.
4. In dual processing systems, up to a 10 mA load from the second processor may be observed on the PCHK# signal. Based on silicon characterization data, V_{OL3} of PCHK# will remain less than 400 mV even with a 10 mA load. PCHK# V_{OL3} will increase to approximately 500 mV with a 14 mA load (worst case for a DP system with a 4 mA system load).

Table 12. I_{CC} Specifications
(Measured at V_{CC2}=2.9V and V_{CC3}=3.6V.)

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		6500 5700 4750	mA mA mA	233 MHz 200 Mhz (1) 166 MHz (1)
I_{CC3}	Power Supply Current		750 650 540	mA mA mA	233 MHz 200 MHz (1) 166 MHz (1)

Stop Grant / Auto Halt Powerdown Power		2.61 2.41 2.05	Watts Watts Watts	233 MHz (3) 200 MHz (3) 166 MHz (3)
Stop Clock Power	0.03	< 0.3	Watts	All frequencies (4)

NOTES:

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at V_{CC2} = 2.8V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with V_{CC2} = 2.8V and V_{CC3} = 3.3 and also takes into account the thermal time constants of the package.
3. Stop Grant/Auto Halt Power Down Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. Active Power (typ) is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
6. Active Power (max) is the maximum power dissipation under normal operating conditions at nominal V_{CC2}, worst-case temperature, while executing the worst case power instruction mix. Active power (max) is equivalent to Thermal Design Power (max).

Table 14. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{IL}$, $V_{IH} > V_{IN} > V_{CC}$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{IL}$, $V_{IH} > V_{IN} > V_{CC}$ (1)
I_{IH}	Input Leakage Current		200	µA	$V_{IN} = 2.4V$ (3)
I_{IL}	Input Leakage Current		–400	µA	$V_{IN} = 0.4V$ (2, 5)

NOTES:

1. This parameter is for inputs/outputs without an internal pull-up or pull-down.
2. This parameter is for inputs with an internal pull-up.
3. This parameter is for inputs with an internal pull-down.
4. Guaranteed by design.
5. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).

3.4. AC Specifications

The AC specifications consist of output delays, input setup requirements and input hold requirements. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor with MMX technology operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

Each Pentium processor with MMX technology specified to operate within a single bus-to-core ratio and a specific minimum to maximum bus frequency range (corresponding to a minimum to maximum core frequency range). Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported. For example, the 166 MHz Pentium processor with MMX technology does not operate beyond the 66 MHz bus frequency and only supports the 2/5 bus-to-core ratio; it does not support the 1/3, 1/2, or 2/3 bus-to-core ratios. Table 3 clarifies and summarizes these specifications.

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation

(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz	4	
t_{1a}	CLK Period	15.0	30.0	ns	4	
t_{1b}	CLK Period Stability		±250	ps		Adjacent Clocks (1, 25)
t_2	CLK High Time	4.0		ns	4	2V (1)
t_3	CLK Low Time	4.0		ns	4	0.8V (1)
t_4	CLK Fall Time	0.15	1.5	ns	4	(2.0V–0.8V) (1, 5)
t_5	CLK Rise Time	0.15	1.5	ns	4	(0.8V–2.0V) (1, 5)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	5	
t_{6b}	AP Valid Delay	1.0	8.5	ns	5	
t_{6c}	BE0-7#, LOCK# Valid Delay	0.9	7.0	ns	5	(4)
t_{6d}	ADS# Valid Delay	0.8	6.0	ns	5	
t_{6e}	ADSC#, D/C#, W/R#, SCYC, Valid Delay	0.8	7.0	ns	5	
t_{6f}	M/IO# Valid Delay	0.8	5.9	ns	5	
t_{6g}	A3–A16 Valid Delay	0.5	6.6	ns	5	
t_{6h}	A17–A31 Valid Delay	0.6	6.6	ns	5	

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)
(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	6	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	5	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	5	(4)
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	5	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	5	(4)
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	5	
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	5	
t_{10b}	HITM# Valid Delay	0.7	6.0	ns	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	ns	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	ns	5	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	ns	6	(1)
t_{14}	A5-A31 Setup Time	6.0		ns	7	(26)
t_{15}	A5-A31 Hold Time	1.0		ns	7	
t_{16a}	INV, AP Setup Time	5.0		ns	7	
t_{16b}	EADS# Setup Time	5.0		ns	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	7	
t_{18a}	KEN# Setup Time	5.0		ns	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		ns	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		ns	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	7	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		ns	7	

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)
(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24b}	PEN# Setup Time	4.8		ns	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	7	
t_{25b}	HOLD Hold Time	1.5		ns	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	7	(12, 16)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	7	(13)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	7	(12, 16, 17)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	7	(13)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLK		(15, 17)
t_{31}	R/S# Setup Time	5.0		ns	7	(12, 16, 17)
t_{32}	R/S# Hold Time	1.0		ns	7	(13)
t_{33}	R/S# Pulse Width, Async.	2.0		CLK		15, 17)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	2.8		ns	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		ns	7	
t_{36}	RESET Setup Time	5.0		ns	8	(12, 16)
t_{37}	RESET Hold Time	1.0		ns	8	(13)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLK	8	(17)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	8	(12, 16, 17)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	8	(13)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLK		To RESET falling edge (16)
t_{42b}	Reset Configuration Signals	2.0		CLK		To RESET falling edge

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)
(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	(INIT, FLUSH#, BRDYC#, BUSCHK#) Hold Time, Async.					(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLK		To RESET falling edge (27)
t_{43a}	BF0, BF1, CPUTYP Setup Time	1.0		ms	8	To RESET falling edge (22)
t_{43b}	BF0, BF1, CPUTYP Hold Time	2.0		CLK		To RESET falling edge (22)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLK		To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLK		To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	4	
t_{46}	TCK High Time	25.0		ns	4	2V (1)
t_{47}	TCK Low Time	25.0		ns	4	0.8V (1)
t_{48}	TCK Fall Time		5.0	ns	4	(2.0V–0.8V) (1, 8, 9)
t_{49}	TCK Rise Time		5.0	ns	4	(0.8V–2.0V) (1, 8, 9)
t_{50}	TRST# Pulse Width	40.0		ns	10	Asynchronous (1)
t_{51}	TDI, TMS Setup Time	5.0		ns	9	(7)
t_{52}	TDI, TMS Hold Time	13.0		ns	9	(7)
t_{53}	TDO Valid Delay	2.5	20.0	ns	9	(8)
t_{54}	TDO Float Delay		25.0	ns	9	(1, 8)
t_{55}	All Non-Test Outputs Valid Delay	2.5	20.0	ns	9	(3, 8, 10)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	9	(1, 3, 8, 10)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	9	(3, 7, 10)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	9	(3, 7, 10)
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz	4	
t_{60b}	PICCLK Period	60.0	500.0	ns	4	
t_{60c}	PICCLK High Time	15.0		ns	4	
t_{60d}	PICCLK Low Time	15.0		ns	4	

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)

(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	4	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	4	
t_{60g}	PICD0-1 Setup Time	3.0		ns	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		ns	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	ns	5	From PICCLK (28)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	ns	5	From PICCLK (28)

NOTES:
Please refer to Table 16 for footnotes.

Table 16. Pentium® Processor with MMX™ Technology Dual Processor Mode AC Specifications for 66-MHz Bus Operation
(See Table 10 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT#, PHIT# Flight Time	0.0	2.0	ns	5	(11, 24)
t_{80b}	PHITM# Flight Time	0.0	1.8	ns	5	(11, 24)
t_{83a}	A5-A31 Setup Time	3.7		ns	7	(18)
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	4.0		ns	7	(18, 21)
t_{83c}	ADS#, M/IO# Setup Time	5.8		ns	7	(18, 21)
t_{83d}	HIT#, HITM# Setup Time	6.0		ns	7	(18, 21)
t_{83e}	HLDA Setup Time	6.0		ns	7	(18, 21)
t_{84a}	CACHE#, HIT# Hold Time	1.0		ns	7	(18, 21)
t_{84b}	ADS#, D/C#, W/R#, M/IO#, A5-A31, HLDA, SCYC Hold Time	0.8		ns	7	(18, 21)
t_{84c}	LOCK# Hold Time	0.9		ns	7	(18, 21)
t_{84d}	HITM# Hold Time	0.7		ns	7	(18, 21)
t_{85}	DPEN# Valid Time		10.0	CLK		(18, 19, 23)
t_{86}	DPEN# Hold Time	2.0		CLK		(18, 20, 23)
t_{87}	APIC ID (BE0#-BE3#) Setup Time	2.0		CLK	8	To falling Edge of RESET (23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLK	8	From Falling Edge of RESET (23)
t_{89}	D/P# Valid Delay	1.0	8.0	ns	5	Primary Processor Only

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer models to account for signal flight time delays.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1 V/ns rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK# and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns (CLK input rise/fall time ≤ 8V/ns.
6. 0.3V/ns (input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During debugging, do not use the boundary scan timings (t_{55} to t_{58}).

17. When driven asynchronously, RESET, NMI, FLUSH#, IV3#, INIT and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
18. Timings are valid only when dual processor is present.
19. Maximum time DPEN# is valid from rising edge of RESET.
20. Minimum time DPEN# is valid after falling edge of RESET.
21. The D/C#, M/IO#, W/R#, CACHE# and A5–A31 signals are sampled only on the CLK that ADS# is active.
22. In order to override the internal defaults and guarantee that the BF[1:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pull-up/pull-down resistor to V_{CC3} or ground. Driving these pins with active logic is not recommended unless stability duringt RESET can be guaranteed. Similarly, CPUTYP should also be strapped directly to or through a pull-up/pull-down resistor to V_{CC3} or ground.
23. RESET is synchronous in dual processing mode. All signals which have a setup or hold time with respect to a falling or rising edge of RESET in UP mode, should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing mode.
24. The PHIT# and PHITM# signals operate at the core frequency.
25. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 kHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within ±250 ps. Therefore, the CLK input cannot be changed dynamically.
26. In dual processing mode, timing t14 is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
27. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
28. This assumes an external pull-up resistor to V_{CC} and a lumped capacitive load. The pull-up resistor must be between 300 ohms and 1K ohms, the capacitance must be between 20 pF and 240 pF, and the RC product must be between 6 ns and 36 ns. VOL for PICD0-1 is 0.55V.

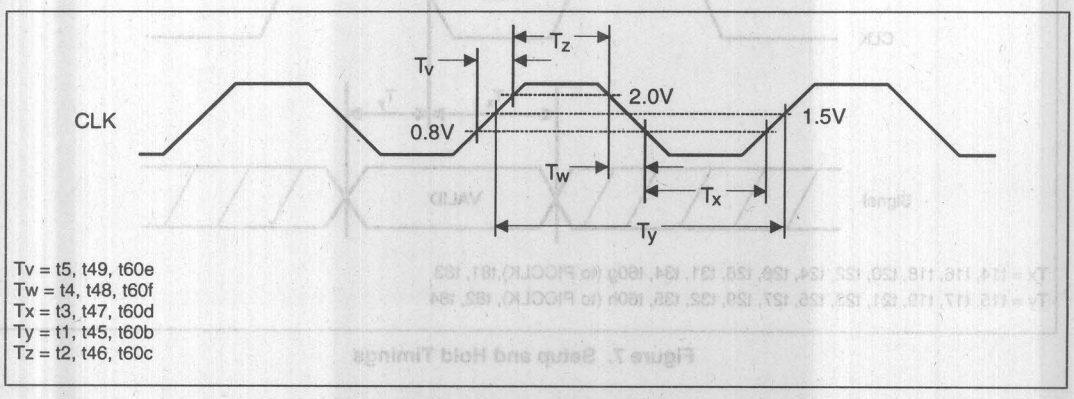


Figure 4. Clock Waveform

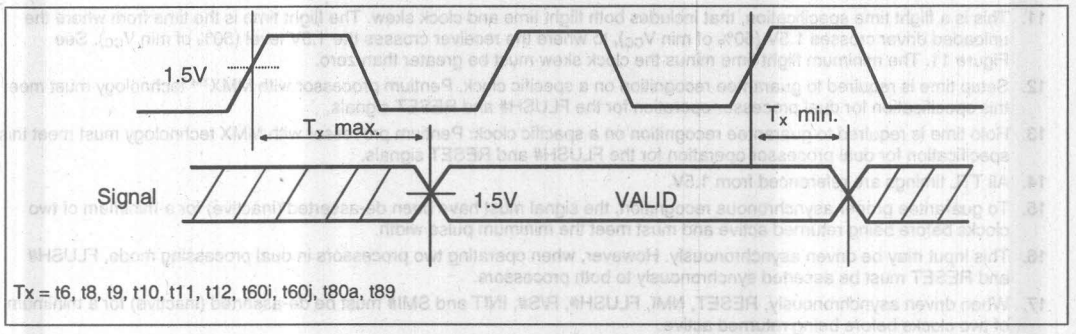


Figure 5. Valid Delay Timings

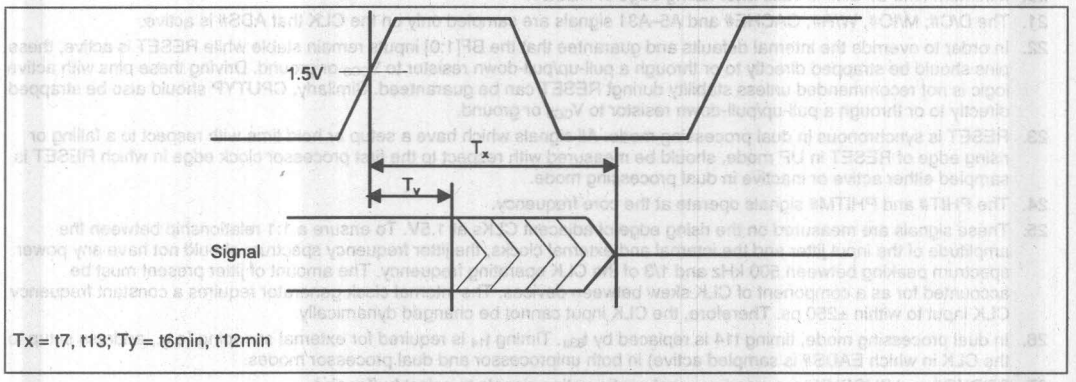


Figure 6. Float Delay Timings

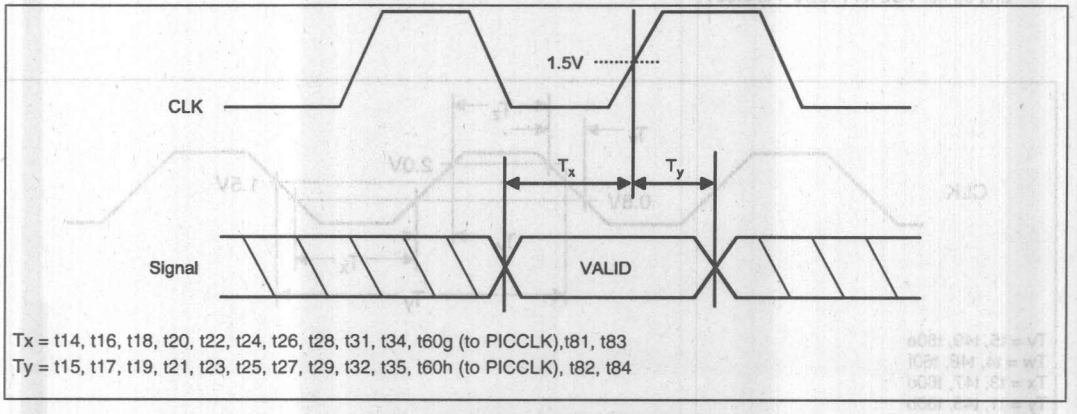
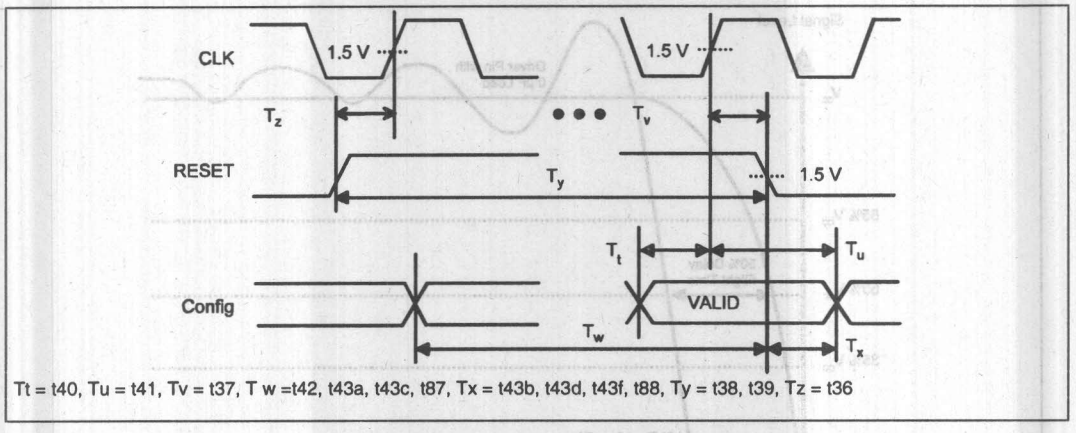
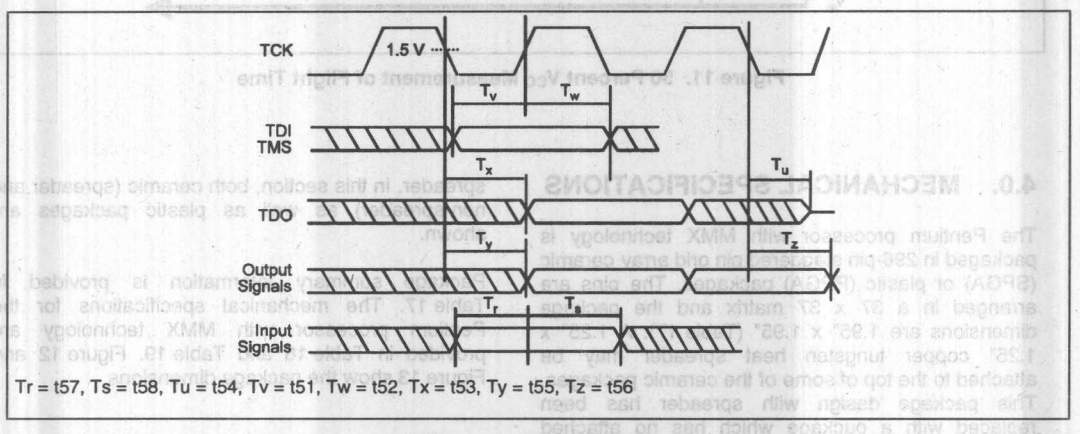


Figure 7. Setup and Hold Timings



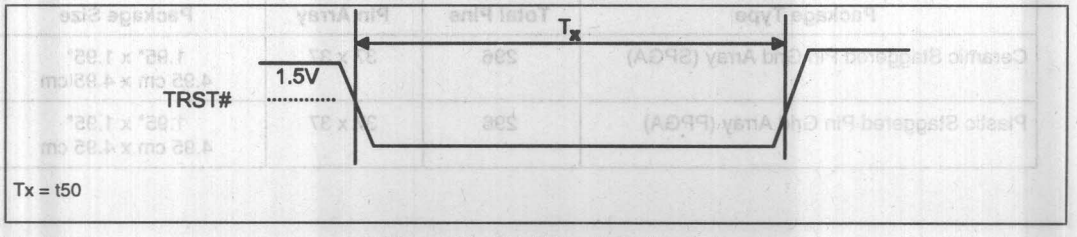
Tt = t40, Tu = t41, Tv = t37, T w =t42, t43a, t43c, t87, Tx = t43b, t43d, t43f, t88, Ty = t38, t39, Tz = t36

Figure 8. Reset and Configuration Timings



Tr = t57, Ts = t58, Tu = t54, Tv = t51, Tw = t52, Tx = t53, Ty = t55, Tz = t56

Figure 9. Test Timings



Tx = t50

Figure 10. Test Reset Timings

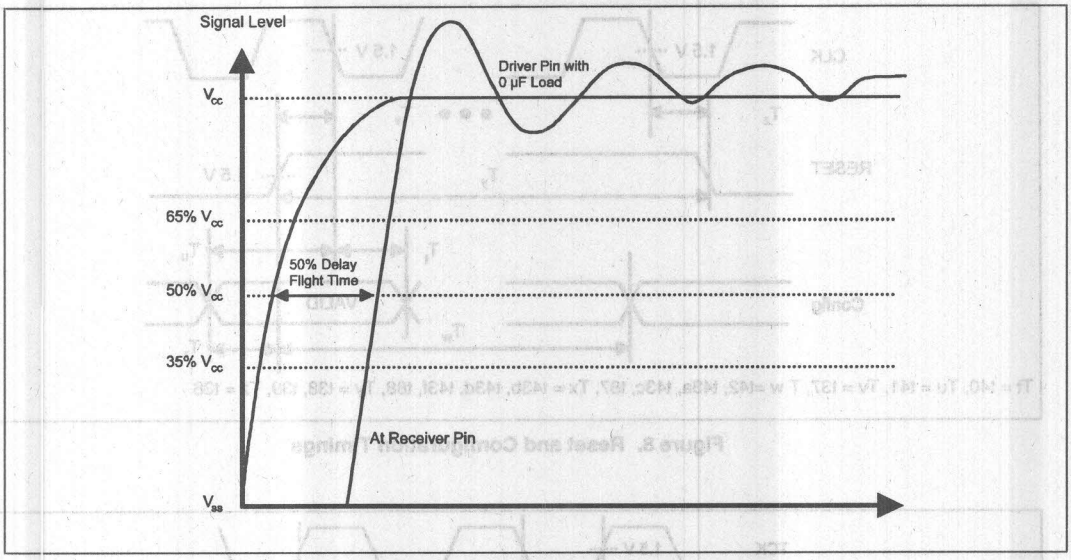


Figure 11. 50 Percent V_{CC} Measurement of Flight Time

4.0. MECHANICAL SPECIFICATIONS

The Pentium processor with MMX technology is packaged in 296-pin staggered pin grid array ceramic (SPGA) or plastic (PPGA) packages. The pins are arranged in a 37 x 37 matrix and the package dimensions are 1.95" x 1.95" (Table 17). A 1.25" x 1.25" copper tungsten heat spreader may be attached to the top of some of the ceramic packages. This package design with spreader has been replaced with a package which has no attached spreader. In this section, both ceramic (spreader and non-spreader) as well as plastic packages are shown.

Package summary information is provided in Table 17. The mechanical specifications for the Pentium processor with MMX technology are provided in Table 18 and Table 19. Figure 12 and Figure 13 show the package dimensions.

Table 17. Package Information Summary for Pentium® Processor with MMX™ Technologty

Package Type	Total Pins	Pin Array	Package Size
Ceramic Staggered Pin Grid Array (SPGA)	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm
Plastic Staggered Pin Grid Array (PPGA)	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

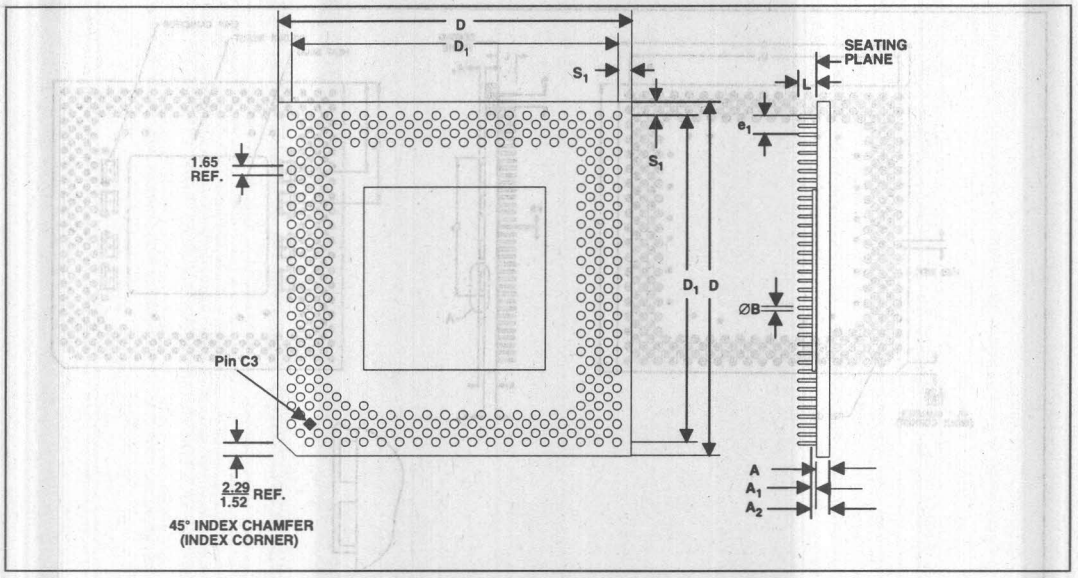


Figure 12. SPGA Package Dimensions

Table 18. SPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.62	2.97		0.103	0.117	
A_1	0.69	0.84	Ceramic Lid	0.027	0.033	Ceramic Lid
A_2	3.31	3.81	Ceramic Lid	0.130	0.150	Ceramic Lid
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

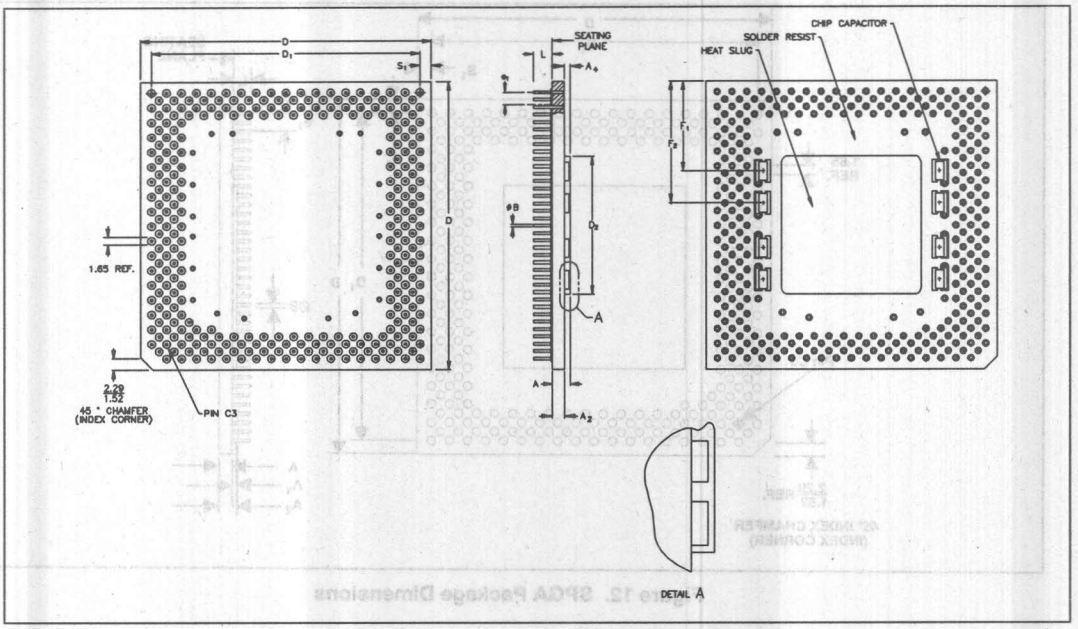


Figure 13. PPGA Package Dimensions

Table 19. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.72	3.33		0.107	0.131	
A_1	1.83	2.23		0.072	0.088	
A_2	1.00			0.039		
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D_1	45.59	45.85		1.795	1.805	
D_2	23.44	23.95		0.923	0.943	
e_1	2.29	2.79		0.090	0.110	
F_1	17.56			0.692		
F_2	23.04			0.907		
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count

Table 19. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
S_1	1.52	2.54		0.060	0.100	

5.0. THERMAL SPECIFICATIONS

The Pentium processor with MMX technology is specified for proper operation when case temperature, T_{CASE}, (T_C) is within the specified range of 0°C to 70°C.

5.1. Measuring Thermal Values

To verify that the proper T_C is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (smaller than 0.150" diameter) should be drilled through the heatsink to allow probing the center of the package. See Figure 14 for an illustration of how to measure TC.

To minimize the measurement errors, it is recommended to use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega* (part number 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number OB-100).
- The thermocouple should be attached at a 90-degree angle as shown in Figure 14.
- The hole size should be smaller than 0.150' in diameter.
- Make sure there is no contact between thermocouple cement and heatsink base. The contact will affect the thermocouple reading.

5.1.1. THERMAL EQUATIONS AND DATA

For the Pentium processor with MMX technology, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that T_C is met. To calculate T_A values, the following equations may be used:

$$T_A = T_C - (P * \Theta_{CA})$$

$$\Theta_{CA} = \Theta_{JA} - \Theta_{JC}$$

Where:

T_A and T_C = Ambient and case temperature. (°C)

Θ_{CA} = Case-to-ambient thermal resistance. (ºC/Watt)

Θ_{JA} = Junction-to-ambient thermal resistance. (ºC/Watt)

Θ_{JC} = Junction-to-case thermal resistance. (ºC/Watt)

P = Maximum power consumption (Watt)

Table 20 and Table 21 list the Θ_{JC} and Θ_{CA} values for the Pentium processor with MMX technology with passive heatsinks. Θ_{JC} is thermal resistance from die to package case. Θ_{JC} values shown in these tables are typical values. The actual Θ_{JC} values depend on actual thermal conductivity and process of die attach. Θ_{CA} is thermal resistance from package case to the ambient. Θ_{CA} values shown in these tables are typical values. The actual Θ_{CA} values depend on the heatsink design, interface between heatsink and package, the air flow in the system, and thermal interactions between processor and surrounding components through PCB and the ambient. Figure 15 and Figure 16 show Table 20 and Table 21 in graphical format.

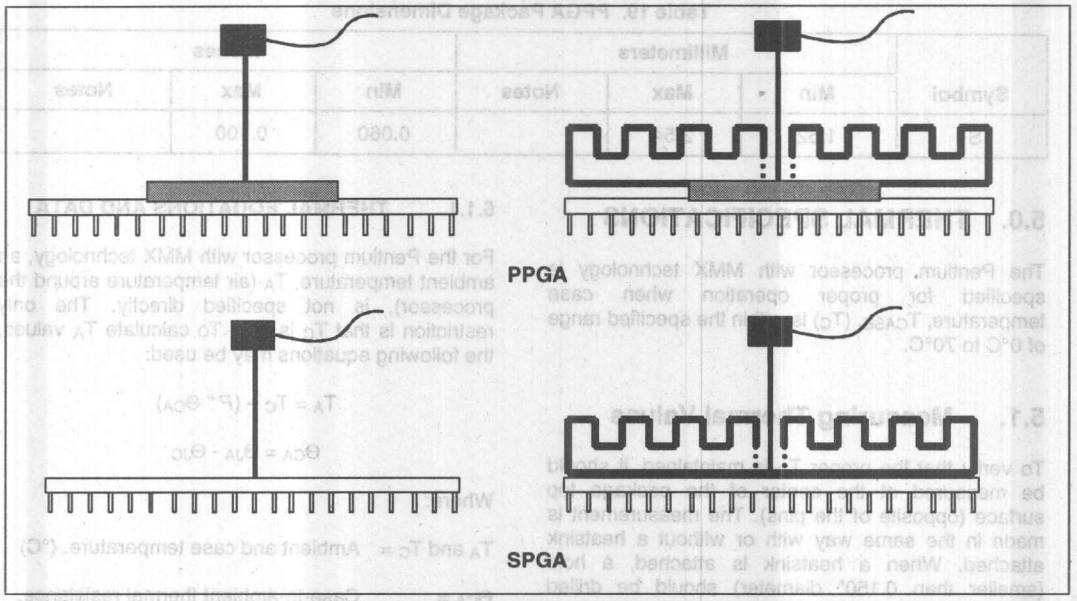


Figure 14. Technique fore Measuring T_C on PPGA and SPGA Packages

Table 20. Thermal Resistance for SPGA Packages

Heatsink Height (inches)	θ_{JC} (°C/Watt)	θ_{CA} (°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.9	9.2	8.1	6.7	4.6	3.7	3.1
0.35	0.9	8.9	7.6	6.1	4.1	3.4	2.9
0.45	0.9	8.5	7.1	5.4	3.7	3.0	2.6
0.55	0.9	8.2	6.6	4.8	3.3	2.7	2.4
0.65	0.9	7.8	6.1	4.4	3.1	2.5	2.2
0.80	0.9	7.1	5.4	4.0	2.9	2.3	2.1
1.00	0.9	6.4	4.8	3.7	2.7	2.2	1.9
1.20	0.9	6.0	4.4	3.4	2.5	2.1	1.9
1.40	0.9	5.5	4.0	3.1	2.3	2.0	1.8
Without Heatsink	1.4	14.4	13.4	12.1	9.7	8.0	7.0

NOTES:

Heatsinks are omni directional pin aluminum alloy.

Features were based on standard extrusion practices for a given height:

Pin size ranged from 50 to 129 mils

Pin spacing ranged from 93 to 175 mils

Based thickness ranged from 79 to 200 mils

Heatsink attach was 0.005" of thermal grease.

Attach thickness of 0.002" will improve performance approximately 0.3ºC/Watt.

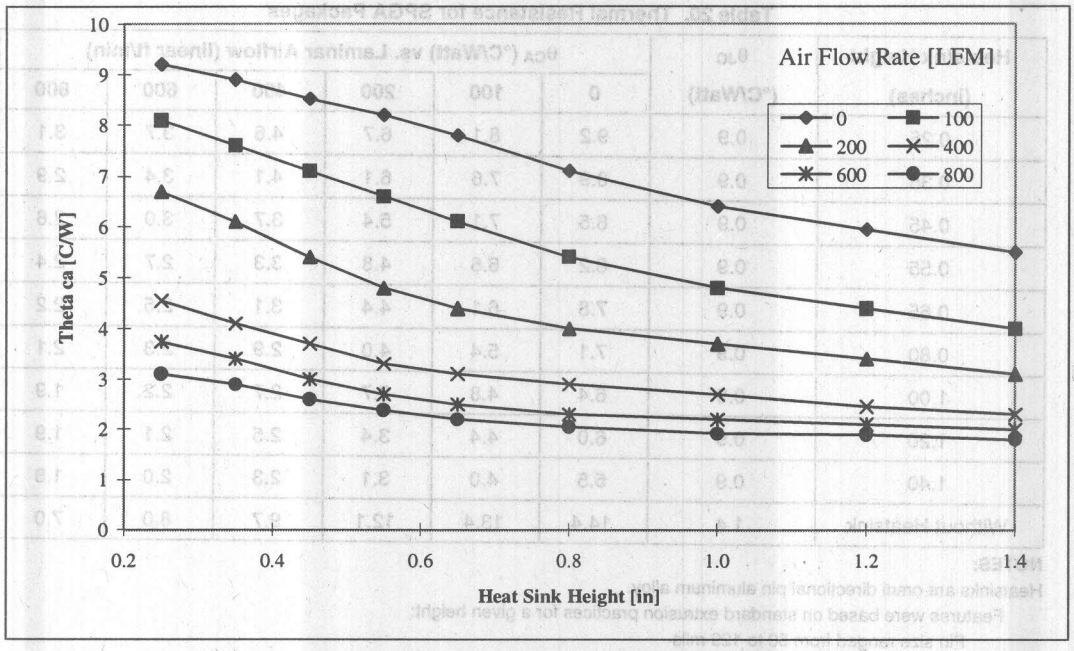


Figure 15. Thermal Resistance vs. Heatsink Height, SPGA Packages

0.65	0.4	7.5	5.8	4.1	2.8	2.2	1.9
0.80	0.4	6.8	5.1	3.7	2.6	2.0	1.8
1.00	0.4	6.1	4.5	3.4	2.4	1.9	1.6
1.20	0.4	5.7	4.1	3.1	2.2	1.8	1.6
1.40	0.4	5.2	3.7	2.8	2.0	1.7	1.5
None	1.2	12.9	12.2	11.2	7.7	6.3	5.4

NOTES:

Heatsinks are omni directional pin aluminum alloy.

Features were based on standard extrusion practices for a given height:

Pin size ranged from 50 to 129 mils

Pin spacing ranged from 93 to 175 mils

Based thickness ranged from 79 to 200 mils

Heatsink attach was 0.005" of thermal grease.

Attach thickness of 0.002" will improve performance approximately 0.3ºC/Watt.

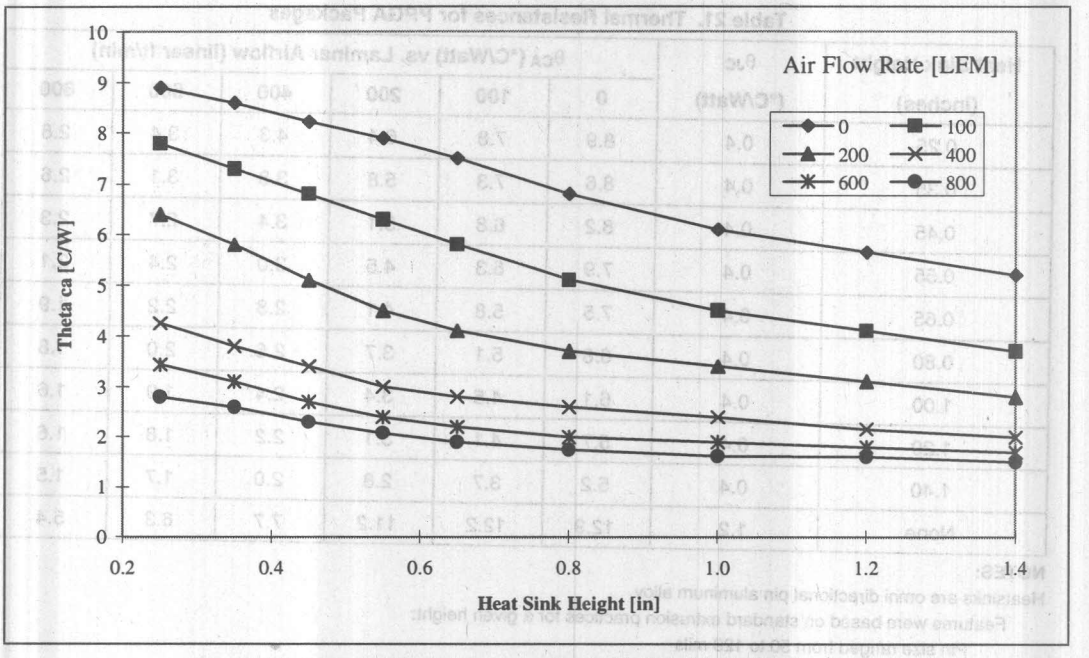


Figure 16. Thermal Resistance vs. Heatsink Height, PPGA Packages

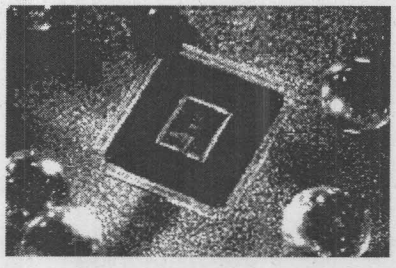
PENTIUM® PROCESSORS WITH VOLTAGE REDUCTION TECHNOLOGY

Max. Operating Frequency	75 MHz	100 MHz	120 MHz	133 MHz	150 MHz
iCOMP® Index 2.0 Rating	67	90	100	111	114

Note: Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

- Compatible with Large Software Base
  - MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit CPU with 64-Bit Data Bus
- Superscalar Architecture
  - Two Pipelined Integer Units Are Capable of 2 Instructions/Clock
  - Pipelined Floating Point Unit
- Separate Code and Data Caches
  - 8K Code, 8K Writeback Data
  - MESI Cache Protocol
- Advanced Design Features
  - Branch Prediction
  - Virtual Mode Extensions
- Low Voltage BiCMOS Silicon Technology
- 4M Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Internal Error Detection Features
- SL Enhanced Power Management Features
  - System Management Mode
  - Clock Control
- Voltage Reduction Technology
  - 2.9V V_{CC} for core supply (75/90/100/120/133 MHz)
  - 3.1V V_{CC} for core supply (150 MHz)
  - 3.3V V_{CC} for I/O buffer supply
- Fractional Bus Operation
  - 75-MHz Core / 50-MHz Bus
  - 100-MHz Core / 66-MHz Bus
  - 120-MHz Core / 60-MHz Bus
  - 133-MHz Core / 66-MHz Bus
  - 150-MHz Core / 60-MHz Bus

The Pentium® processor is fully compatible with the entire installed base of applications for DOS*, Windows*, OS/2*, and UNIX*, and all other software that runs on any earlier Intel 8086 family product. The Pentium processor's superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor with voltage reduction technology has 3.3 million transistors. It is built on Intel's advanced low voltage BiCMOS silicon technology, and has full SL Enhanced power management features, including System Management Mode (SMM) and clock control. The additional SL Enhanced features, 2.9V (3.1V for 150 MHz) core operation along with 3.3V I/O buffer operation, and the option of the TCP, which are not available in the desktop version of the Pentium processor, make the Pentium processor with voltage reduction technology ideal for enabling mobile Pentium processor designs. The Pentium processor may contain design defects or errors known as errata. Current characterized errata are available upon request.



August 1996

Order Number: 242557-005

PENTIUM® PROCESSORS WITH VOLTAGE REDUCTION TECHNOLOGY

Max. Operating Frequency	75 MHz	100 MHz	120 MHz	133 MHz	150 MHz
iCOMP® Index 2.0 Rating	67	90	100	111	114

Note: Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

- Compatible with Large Software Base
  - MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit CPU with 64-Bit Data Bus
- Superscalar Architecture
  - Two Pipelined Integer Units Are Capable of 2 Instructions/Clock
  - Pipelined Floating Point Unit
- Separate Code and Data Caches
  - 8K Code, 8K Writeback Data
  - MESI Cache Protocol
- Advanced Design Features
  - Branch Prediction
  - Virtual Mode Extensions
- Low Voltage BiCMOS Silicon Technology
- 4M Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Internal Error Detection Features
- SL Enhanced Power Management Features
  - System Management Mode
  - Clock Control
- Voltage Reduction Technology
  - 2.9V V_{CC} for core supply (75/90/100/120/133 MHz)
  - 3.1V V_{CC} for core supply (150 MHz)
  - 3.3V V_{CC} for I/O buffer supply
- Fractional Bus Operation
  - 75-MHz Core / 50-MHz Bus
  - 100-MHz Core / 66-MHz Bus
  - 120-MHz Core / 60-MHz Bus
  - 133-MHz Core / 66-MHz Bus
  - 150-MHz Core / 60-MHz Bus

The Pentium® processor is fully compatible with the entire installed base of applications for DOS*, Windows*, OS/2*, and UNIX*, and all other software that runs on any earlier Intel 3086 family product. The Pentium processor's superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while maximizing software transparency. The Pentium processor with voltage reduction technology has 3.3 million transistors built on Intel's advanced low voltage BiCMOS silicon technology and has full SL Enhanced power management features including System Management Mode (SMM) and clock control. The additional SL Enhanced features, 2.9V (3.1V for 150 MHz) core operation along with 3.3V I/O buffer operation, and the option of the TCP, which are not available in the desktop version of the Pentium processor, make the Pentium processor with voltage reduction technology ideal for enabling mobile Pentium processor designs. The Pentium processor may contain design defects or errors known as errata. Current characterized errata are available upon request.

Order Number: 241857-002

August 1996

1.0. INTRODUCTION

Intel is manufacturing a reduced power version of the latest Pentium® processor, the Pentium processor with voltage reduction technology, targeting the mobile market. Voltage reduction technology allows the processor to "talk" to industry standard 3.3-volt components while its inner core, operating at 2.9 volts (current 150-MHz processors inner core is 3.1 volts, with plans to have a 2.9 volt version in the future), consumes less power to promote a longer battery life. The Pentium processor with voltage reduction technology is offered in the Tape Carrier Package (TCP) and the Staggered Pin Grid Array (SPGA) package. It has all the advanced features of the 3.3V Pentium except for the differences listed in sections 3.1 and 7.1.1.

The Pentium processor with voltage reduction technology has several features which allow high-performance notebooks to be designed with the Pentium processor, including the following:

- TCP dimensions are ideal for small form-factor designs.
- TCP has superior thermal resistance characteristics.
- 2.9V (3.1V for 150 MHz) core and 3.3V I/O buffer V_{CC} inputs reduce power consumption significantly, while maintaining 3.3V compatibility externally.
- The SL Enhanced feature set, which was initially implemented in the Intel486™ CPU.

The architecture and internal features of the Pentium processor with voltage reduction technology are identical to the desktop version of the Pentium processor specifications provided in the Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors., except several features not used in mobile applications have been eliminated to streamline it for mobile applications.

This document should be used in conjunction with the following related Pentium processor documents.

- Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors (Order Number: 241428)
- Pentium® Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (Order Number: 241430)

2.0. MICROPROCESSOR ARCHITECTURE OVERVIEW

The Pentium processor with voltage reduction technology extends the Intel Pentium family of microprocessors. It is compatible with a host of other Intel products.

The Pentium processor family consists of the Pentium processor with voltage reduction technology described in this document, the original mobile Pentium processor and the various desktop Pentium processors. "Pentium processor" will be used in this document to refer to the entire Pentium processor family in general.

The mobile Pentium processor family architecture contains all of the features of the Intel486 CPU family, and provides significant enhancements and additions including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 8K Code and 8K Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- Voltage Reduction Technology
- SL Power Management Features

2.1. Mobile Pentium ® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of CPUs.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the Branch Target Buffer (BTB) so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 CPU. Faster algorithms provide up to 10X speed-up for common operations including add, multiply and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache is 8 Kbytes in size, with a 32-byte line size and is 2-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst writeback cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' MMU contains optional extensions to the architecture which allow 2-Mbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

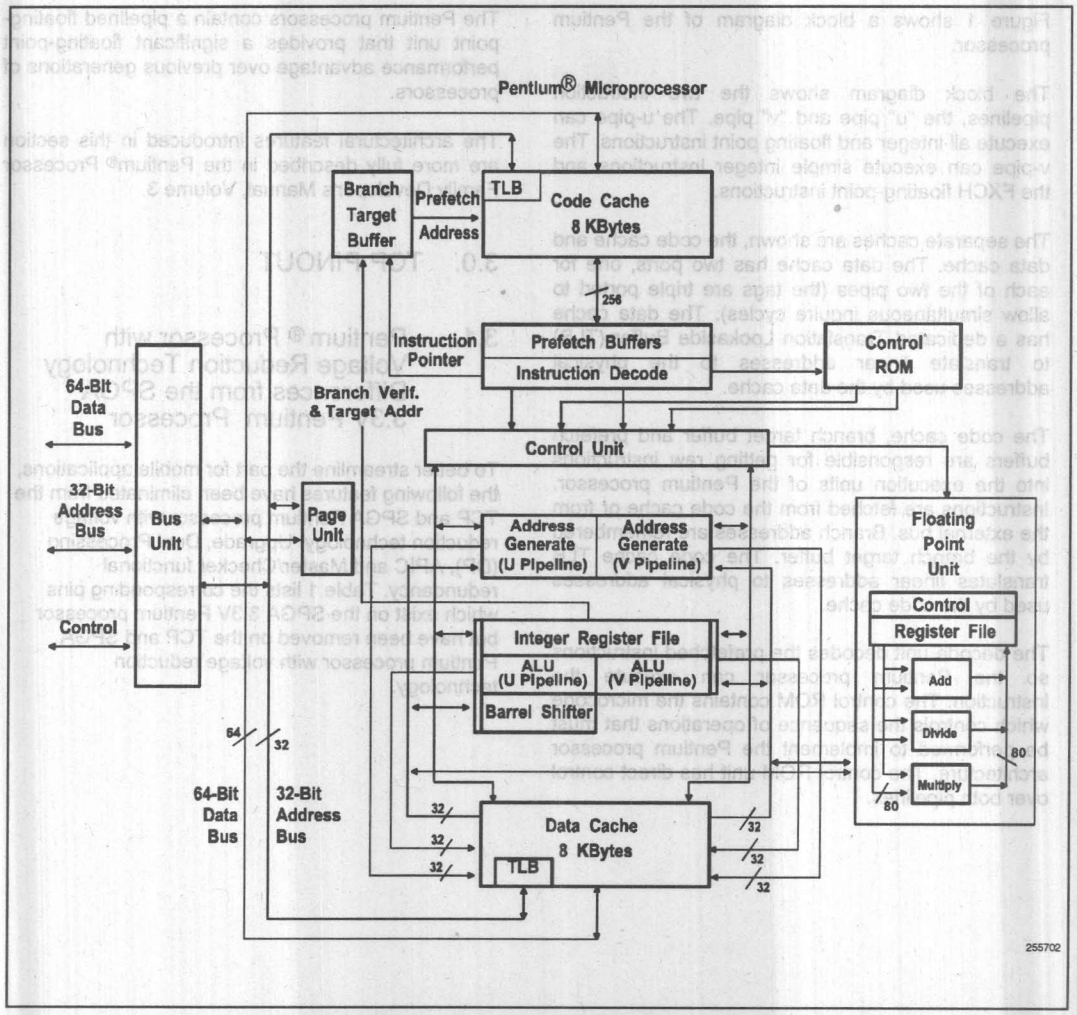


Figure 1. Pentium® Processor Block Diagram

Figure 1 shows a block diagram of the Pentium processor.

The block diagram shows the two instruction pipelines, the "u" pipe and "v" pipe. The u-pipe can execute all integer and floating point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate caches are shown, the code cache and data cache. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

The architectural features introduced in this section are more fully described in the Pentium® Processor Family Developer's Manual, Volume 3.

3.0. TCP PINOUT

3.1. Pentium® Processor with Voltage Reduction Technology Differences from the SPGA 3.3V Pentium Processor

To better streamline the part for mobile applications, the following features have been eliminated from the TCP and SPGA Pentium processor with voltage reduction technology: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins which exist on the SPGA 3.3V Pentium processor but have been removed on the TCP and SPGA Pentium processor with voltage reduction technology.

Table 1. Signals Removed in Pentium ® Processor with Voltage Reduction Technology

Signal	Function
ADSC#	Additional Address Status. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	Additional Burst Ready. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	CPU Type. This signal is used for dual processing systems.
D/P#	Dual/Primary processor identification. This signal is only used for an upgrade processor.
FRCMC#	Functional Redundancy Checking. This signal is only used for error detection via processor redundancy, and requires two Pentium® processors (master/checker).
PBGNT#	Private Bus Grant. This signal is only used for dual processing systems.
PBREQ#	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	Private Hit. This signal is only used for dual processing systems.
PHITM#	Private Modified Hit. This signal is only used for dual processing systems.
PICCLK	APIC Clock. This signal is the APIC interrupt controller serial data bus clock.
PICD0 [DPEN#]	APIC's Programmable Interrupt Controller Data line 0. PICD0 shares a pin with DPEN# (Dual Processing Enable).
PICD1 [APICEN]	APIC's Programmable Interrupt Controller Data line 1. PICD1 shares a pin with APICEN (APIC Enable (on RESET)).

3.2. TCP Pinout and Pin Descriptions

3.2.1. TCP PENTIUM® PROCESSOR PINOUT

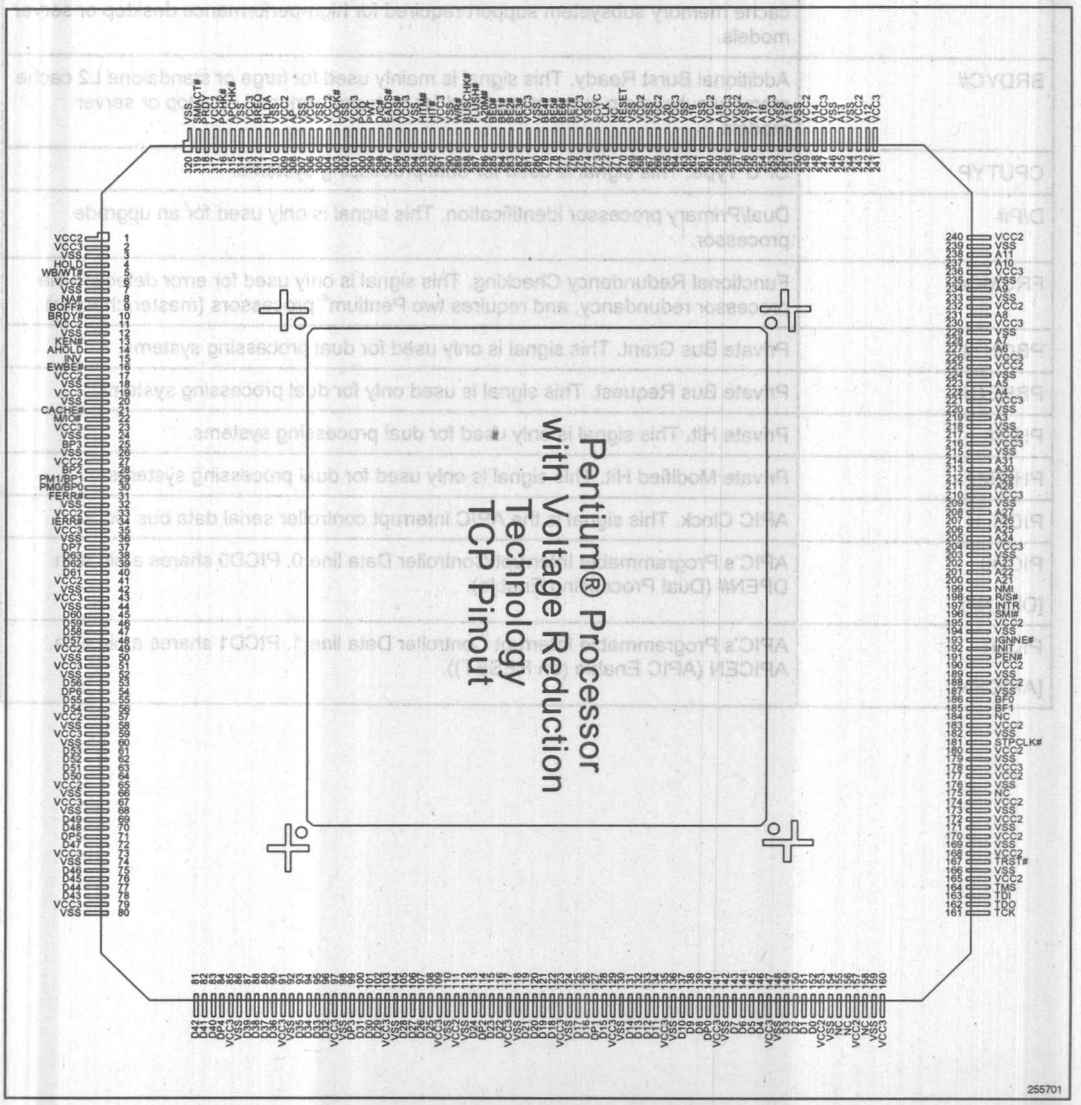


Figure 2. TCP Pentium ® Processor Pinout

3.2.2. TCP PENTIUM ® PROCESSOR PIN CROSS REFERENCE

Table 2. TCP Pin Cross Reference by Pin Name

Address									
A3	219	A9	234	A15	251	A21	200	A27	208
A4	222	A10	237	A16	254	A22	201	A28	211
A5	223	A11	238	A17	255	A23	202	A29	212
A6	227	A12	242	A18	259	A24	205	A30	213
A7	228	A13	245	A19	262	A25	206	A31	214
A8	231	A14	248	A20	265	A26	207		
Data									
D0	152	D13	132	D26	107	D39	87	D52	62
D1	151	D14	131	D27	106	D40	83	D53	61
D2	150	D15	128	D28	105	D41	82	D54	56
D3	149	D16	126	D29	102	D42	81	D55	55
D4	146	D17	125	D30	101	D43	78	D56	53
D5	145	D18	122	D31	100	D44	77	D57	48
D6	144	D19	121	D32	96	D45	76	D58	47
D7	143	D20	120	D33	95	D46	75	D59	46
D8	139	D21	119	D34	94	D47	72	D60	45
D9	138	D22	116	D35	93	D48	70	D61	40
D10	137	D23	115	D36	90	D49	69	D62	39
D11	134	D24	113	D37	89	D50	64	D63	38
D12	133	D25	108	D38	88	D51	63		

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

Control							
A20M#	286	BREQ	312	HITM#	293	PM1/BP1	29
ADS#	296	BUSCHK#	288	HLDA	311	PRDY	318
AHOLD	14	CACHE#	21	HOLD	4	PWT	299
AP	308	D/C#	298	IERR#	34	R/S#	198
APCHK#	315	DP0	140	IGNNE#	193	RESET	270
BE0#	285	DP1	127	INIT	192	SCYC	273
BE1#	284	DP2	114	INTR/LINT0	197	SMI#	196
BE2#	283	DP3	99	INV	15	SMIACT#	319
BE3#	282	DP4	84	KEN#	13	TCK	161
BE4#	279	DP5	71	LOCK#	303	TDI	163
BE5#	278	DP6	54	M/IO#	22	TDO	162
BE6#	277	DP7	37	NA#	8	TMS	164
BE7#	276	EADS#	297	NMI/LINT1	199	TRST#	167
BOFF#	9	EWBE#	16	PCD	300	W/R#	289
BP2	28	FERR#	31	PCHK#	316	WB/WT#	5
BP3	25	FLUSH#	287	PEN#	191		
BRDY#	10	HIT#	292	PM0/BP0	30		
				Clock Control			
				BF0	186	CLK	272
				BF1	185	STPCLK#	181

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

$V_{CC}2$*			
1	111	183	257
6	153	188	260
11	157	190	266
17	165	195	268
27	168	217	304
33	170	225	309
41	172	232	317
49	174	240	
57	177	243	
65	180	249	
$V_{CC}3$**			
2	91	178	258
19	97	204	264
23	103	210	275
35	109	216	281
43	117	221	291
51	123	226	295
59	129	230	301
67	135	236	306
73	141	241	313
79	147	247	
85	160	253	

NOTE:

* These $V_{CC}2$ pins are 2.9V (3.1V for 150 MHz) inputs for the TCP Pentium® processor with voltage reduction technology, but may change to a different voltage on future offerings of this microprocessor family.

** All $V_{CC}3$ pins will remain at 3.3V power inputs for the TCP Pentium processor.

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

V_{SS}						
3	50	104	166	209	250	302
7	52	110	169	215	252	305
12	58	112	171	218	256	307
18	60	118	173	220	261	310
20	66	124	176	224	263	314
24	68	130	179	229	267	320
26	74	136	182	233	269	
32	80	142	187	235	274	
36	86	148	189	239	280	
42	92	154	194	244	290	
44	98	159	203	246	294	
NC						
155	156	158	175	184	271	

Table 3. TCP Pin Cross Reference by Pin Number (Pins 1-160)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	VCC2	41	VCC2	81	D42	121	D19
2	VCC3	42	VSS	82	D41	122	D18
3	VSS	43	VCC3	83	D40	123	VCC3
4	HOLD	44	VSS	84	DP4	124	VSS
5	WB/WT#	45	D60	85	VCC3	125	D17
6	VCC2	46	D59	86	VSS	126	D16
7	VSS	47	D58	87	D39	127	DP1
8	NA#	48	D57	88	D38	128	D15
9	BOFF#	49	VCC2	89	D37	129	VCC3
10	BRDY#	50	VSS	90	D36	130	VSS
11	VCC2	51	VCC3	91	VCC3	131	D14
12	VSS	52	VSS	92	VSS	132	D13
13	KEN#	53	D56	93	D35	133	D12
14	AHOLD	54	DP6	94	D34	134	D11
15	INV	55	D55	95	D33	135	VCC3
16	EWBE#	56	D54	96	D32	136	VSS
17	VCC2	57	VCC2	97	VCC3	137	D10
18	VSS	58	VSS	98	VSS	138	D9
19	VCC3	59	VCC3	99	DP3	139	D8
20	VSS	60	VSS	100	D31	140	DP0
21	CACHE#	61	D53	101	D30	141	VCC3
22	M/IO#	62	D52	102	D29	142	VSS
23	VCC3	63	D51	103	VCC3	143	D7
24	VSS	64	D50	104	VSS	144	D6
25	BP3	65	VCC2	105	D28	145	D5
26	VSS	66	VSS	106	D27	146	D4
27	VCC2	67	VCC3	107	D26	147	VCC3
28	BP2	68	VSS	108	D25	148	VSS
29	PM1/BP1	69	D49	109	VCC3	149	D3
30	PM0/BP0	70	D48	110	VSS	150	D2
31	FERR#	71	DP5	111	VCC2	151	D1
32	VSS	72	D47	112	VSS	152	D0
33	VCC2	73	VCC3	113	D24	153	VCC2
34	IERR#	74	VSS	114	DP2	154	VSS
35	VCC3	75	D46	115	D23	155	NC
36	VSS	76	D45	116	D22	156	NC
37	DP7	77	D44	117	VCC3	157	VCC2
38	D63	78	D43	118	VSS	158	NC
39	D62	79	VCC3	119	D21	159	VSS
40	D61	80	VSS	120	D20	160	VCC3

Table 3. TCP Pin Cross Reference by Pin Number (Pins 161-320) (Contd.)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
161	TCK	201	A22	241	VCC3	281	VCC3
162	TDO	202	A23	242	A12	282	BE3#
163	TDI	203	VSS	243	VCC2	283	BE2#
164	TMS	204	VCC3	244	VSS	284	BE1#
165	VCC2	205	A24	245	A13	285	BE0#
166	VSS	206	A25	246	VSS	286	A20M#
167	TRST#	207	A26	247	VCC3	287	FLUSH#
168	VCC2	208	A27	248	A14	288	BUSCHK#
169	VSS	209	VSS	249	VCC2	289	W/R#
170	VCC2	210	VCC3	250	VSS	290	VSS
171	VSS	211	A28	251	A15	291	VCC3
172	VCC2	212	A29	252	VSS	292	HIT#
173	VSS	213	A30	253	VCC3	293	HITM#
174	VCC2	214	A31	254	A16	294	VSS
175	NC	215	VSS	255	A17	295	VCC3
176	VSS	216	VCC3	256	VSS	296	ADS#
177	VCC2	217	VCC2	257	VCC2	297	EADS#
178	VCC3	218	VSS	258	VCC3	298	D/C#
179	VSS	219	A3	259	A18	299	PWT
180	VCC2	220	VSS	260	VCC2	300	PCD
181	STPCLK#	221	VCC3	261	VSS	301	VCC3
182	VSS	222	A4	262	A19	302	VSS
183	VCC2	223	A5	263	VSS	303	LOCK#
184	NC	224	VSS	264	VCC3	304	VCC2
185	BF1	225	VCC2	265	A20	305	VSS
186	BF0	226	VCC3	266	VCC2	306	VCC3
187	VSS	227	A6	267	VSS	307	VSS
188	VCC2	228	A7	268	VCC2	308	AP
189	VSS	229	VSS	269	VSS	309	VCC2
190	VCC2	230	VCC3	270	RESET	310	VSS
191	PEN#	231	A8	271	NC	311	HLDA
192	INIT	232	VCC2	272	CLK	312	BREQ
193	IGNNE#	233	VSS	273	SCYC	313	VCC3
194	VSS	234	A9	274	VSS	314	VSS
195	VCC2	235	VSS	275	VCC3	315	APCHK#
196	SMI#	236	VCC3	276	BE7#	316	PCHK#
197	INTR	237	A10	277	BE6#	317	VCC2
198	R/S#	238	A11	278	BE5#	318	PRDY
199	NMI	239	VSS	279	BE4#	319	SMIACT#
200	A21	240	VCC2	280	VSS	320	VSS

NOTES:

1. $V_{CC}2$ pins are 2.9V (3.1V for 150 MHz) power inputs to the core.
2. $V_{CC}3$ pins are 3.3V power inputs to the core.

3.3. Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active HIGH inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

3.4. Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the "Hardware Interface" chapter in the Pentium® Processor Family Developer's Manual, Volume 1.

NOTE

All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

The pins are classified as Input or Output based on their function in Master Mode. See the Error Detection chapter of the Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors, for further information.

Table 4. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the address bit 20 mask pin is asserted, the Pentium® processor emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the address lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The address status indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of address hold , the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	Address parity is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The address parity check status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#-BE5# BE4#-BE0#	O I/O	The byte enable pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).
BF[1:0]	I	Bus Frequency determines the bus-to-core ratio. BF[1:0] is sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[1:0] must not change values while RESET is active. See Table 5 for Bus Frequency Selections.
BOFF#	I	The backoff input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The breakpoint pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the performance monitoring pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
BRDY#	I	The burst ready input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The bus request output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The bus check input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception.
CACHE#	O	For processor-initiated cycles, the cache pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The clock input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST# and PICD0-1 are specified with respect to the rising edge of CLK. NOTE: It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.
D/C#	O	The data/code output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63-D0	I/O	These are the 64 data lines for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the data parity pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63-D56; DP0 applies to D7-D0.
EADS#	I	This signal indicates that a valid external address has been driven onto the processor address pins to be used for an inquire cycle.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
EWBE#	I	The external write buffer empty input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The floating point error pin is driven active when an unmasked floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating point error reporting.
FLUSH#	I	When asserted, the cache flush input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. NOTE: If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
HIT#	O	The hit indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The hit to a modified line output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The bus hold acknowledge pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the bus hold request , the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The internal error pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
IGNNE#	I	This is the ignore numeric error input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor initialization input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active maskable interrupt input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The invalidation input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The cache enable pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The bus lock pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The memory/input-output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
NA#	I	An active next address input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The non-maskable interrupt request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The page cache disable pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The parity check output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The parity enable input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the performance monitoring 1 -0 pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The probe ready output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The page writethrough pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The run / stop input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	RESET forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode will be entered or if BIST will be run.
SCYC	O	The split cycle output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
SMI#	I	The system management interrupt causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active system management interrupt active output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the stop clock input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The testability clock input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The test data input is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The test data output is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the test mode select input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the test reset input allows the TAP controller to be asynchronously initialized.
$V_{CC}2$	I	These pins are the 2.9V (3.1V for 150 MHz) power inputs to the Pentium processor with voltage reduction technology.
$V_{CC}3$	I	These pins are the 3.3V power inputs to the Pentium processor with voltage reduction technology.
V_{SS}	I	These pins are the ground inputs to the Pentium processor with voltage reduction technology.
W/R#	O	Write/read is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The writeback/writethrough input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

Table 5. Bus Frequency Selections

Pentium ® Processor Core Frequency (max)	External Bus Frequency (max)	Bus/Core Ratio	BF1	BF0
150 MHz	60 MHz	2/5	0	0
133 MHz	66 MHz	1/2	1	0
120 MHz	60 MHz	1/2	1	0
100 MHz	66 MHz	2/3*	1	1
90 MHz	60 MHz	2/3	1	1
75 MHz	50 MHz	2/3	1	1

NOTE:

- Default setting

3.5. Pin Reference Tables

Table 6. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTE:
- All output and input/output pins are floated during tristate test mode (except TDO).

Table 7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF[1:0]	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

Table 8. Input/Output Pins

Name	Active Level	When Floated	Qualified (when an input)	Internal Resistor
A31-A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown*
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	

NOTES:

- All output and input/output pins are floated during tristate test mode (except TDO).
- *BE3#-BE0# have pulldowns during RESET only.

3.6. Pin Grouping According to Function

Table 9 organizes the pins with respect to their function.

Table 9. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF[1:0]
Address Bus	A31-A3, BE7# - BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

4.0. TCP PENTIUM ® PROCESSOR ELECTRICAL SPECIFICATIONS

4.1. Maximum Ratings

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with voltage reduction technology contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Case temperature under bias ..... –65°C to 110°C

Storage temperature ..... –65°C to 150°C

3V Supply voltage
with respect to V_{SS} ..... –0.5V to +4.6V

2.9V Supply voltage
with respect to V_{SS} ..... –0.5V to +4.1V

3V Only Buffer DC Input
Voltage ..... –0.5V to $V_{CC}3$ +0.5; not to exceed 4.6V (2)

5V Safe Buffer
DC Input Voltage ..... –0.5V to 6.5V (1,3)

NOTES:
1. Applies to CLK.
2. Applies to all Pentium processors with voltage reduction technology inputs except CLK.
3. See Table 11.

WARNING

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

4.2. DC Specifications

Tables 10, 11 and 12 list the DC specifications which apply to the TCP Pentium processor with voltage reduction technology. The Pentium processor with voltage reduction technology core operates at 2.9V (3.1V for 150 MHz) internally while the I/O interface operates at 3.3V. The CLK input may be 3.3V or 5V. Since the 3.3V (5V safe) input levels defined in Table 11 are the same as the 5V TTL levels, the CLK input is compatible with existing 5V clock drivers. The power dissipation specification in Table 13 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

4.2.1. POWER SEQUENCING

There is no specific sequence required for powering up or powering down the $V_{CC}2$ and $V_{CC}3$ power supplies. However, for compatibility with future mobile processors, it is recommended that the $V_{CC}2$ and $V_{CC}3$ power supplies be either both on or both off within one second of each other.

Table 10. 3.3V DC Specifications

T_{CASE} = 0 to 95°C; $V_{CC}2$ = 2.9V (3.1V for 150 MHz) ±165mV; $V_{CC}3$ = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}3$	Input Low Voltage	–0.3	0.8	V	TTL Level (3)
$V_{IH}3$	Input High Voltage	2.0	$V_{CC}3$+0.3	V	TTL Level (3)
$V_{OL}3$	Output Low Voltage		0.4	V	TTL Level (1) (3)
$V_{OH}3$	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}2$	Power Supply Current from 2.9V (3.1V for 150 MHz) core supply		1565 mA 2085 mA 2500 mA 2775 mA 3350 mA		@75 MHz (4) @100 MHz (4) (5) @120 MHz (4) @133 MHz (4) @150 MHz (4)
$I_{CC}3$	Power Supply Current from 3.3V I/O buffer supply		270 mA 355 mA 320 mA 355 mA 320 mA		@75 MHz (4) @100 MHz (4) (5) @120 MHz (4) @133 MHz (4) @150 MHz (4)

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK.
4. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC}+165mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to section 4.3.2.
5. Refer to document 242973 for previous process specification.

Table 11. 3.3V (5V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}5$	Input Low Voltage	–0.3	0.8	V	TTL Level (1)
$V_{IH}5$	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTE:

1. Applies to CLK only.

Table 12. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4V (3)
I_{IL}	Input Leakage Current		–400	µA	V_{IN} = 0.4V (2)

NOTES:
1. This parameter is for input without pull up or pull down.
2. This parameter is for input with pull up.
3. This parameter is for input with pull down.
4. Guaranteed by design.

Table 13. Power Dissipation Requirements for Thermal Design

Parameter	Typical (1)	Max (2)	Unit	Notes
Thermal Design Power (7)		4.4	Watts	@75 MHz (6)
		5.9	Watts	@100 MHz (6)
		7.1	Watts	@120 MHz (5)
		7.9	Watts	@133 MHz
		10.0	Watts	@150 MHz
Active Power (8)	1.7--2.3	N/A	Watts	@75 MHz (6)
	2.0--3.0		Watts	@100 MHz (6)
	2.5--3.5		Watts	@120 MHz (5)
	3.0--4.0		Watts	@133 MHz
	3.8--5.0		Watts	@150 MHz
Stop Grant / Auto Halt Power		0.8	Watts	@75 MHz (3)
		1.2	Watts	@100 MHz (3)
		1.2	Watts	@120 MHz (3)
		1.3	Watts	@133 MHz (3)
		1.4	Watts	@150 MHz (3)
Stop Clock Power	.02	0.05	Watts	(4)

NOTES:

1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at $V_{CC}2$ = 2.9V (3.1V for 150 MHz) and $V_{CC}3$ = 3.3V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using a worst-case instruction mix with $V_{CC}2$ = 2.9V (3.1V for 150 MHz) and $V_{CC}3$ = 3.3V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. The lower power number is due to a process improvement.
6. Refer to document 242973 for previous process specification.
7. Thermal Design Power is the maximum power dissipation under normal operating conditions at nominal $V_{CC}2$ worst case temperature, while executing the worst case power instruction mix.
8. Active Power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.

4.3. AC Specifications

The AC specifications of the TCP Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All TCP Pentium processor with voltage reduction technology AC specifications are valid for $V_{CC}2$ = 2.9V (3.1V for 150 MHz) ±165mV, $V_{CC}3$ = 3.3V ±165mV and Tcase = 0 to 95°C.

4.3.1. POWER AND GROUND

For clean on-chip power distribution, the TCP Pentium processor with voltage reduction technology has 37 $V_{CC}2$ (2.9V power), 42 $V_{CC}3$ (3.3V power) and 72 V_{SS} (ground) inputs. Power and ground connections must be made to all external $V_{CC}2$, $V_{CC}3$ and V_{SS} pins of the Pentium processor with voltage reduction technology. On the circuit board all $V_{CC}2$ pins must be connected to a 2.9V V_{CC2} plane (or island) and all $V_{CC}3$ pins must be connected to a 3.3V $V_{CC}3$ plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 2 for the list of $V_{CC}2$, $V_{CC}3$ and V_{SS} pins.

4.3.2. DECOUPLING RECOMMENDATIONS

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical

performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane and the 2.9V (3.1V for 150 MHz) plane (or island). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3V plane and the 2.9V (3.1V for 150 MHz) plane (or island)) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please contact Intel or refer to the Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems application note (Order Number 242558).

4.3.3. CONNECTION SPECIFICATIONS

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active high inputs should be connected to ground.

4.3.4. AC TIMINGS FOR A 50-MHz BUS

The AC specifications given in Table 14 consist of output delays, input setup requirements and input hold requirements for a 50-MHz external bus. All AC specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 14. TCP Pentium® Processor with Voltage Reduction Technology AC Specifications for 50-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	25.0	50.0	MHz		
t_{1a}	CLK Period	20.0	40.0	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_8	APCHK#, IERR#, FERR#, PCHK# Valid Delay	1.0	8.3	nS	4	(4), (22)
t_{9a}	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)
t_{10b}	HITM# Valid Delay	1.1	6.6	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)

Table 14. TCP Pentium ® Processor with Voltage Reduction Technology
AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{14}	A5-A31 Setup Time	6.5		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	6.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	BOFF# Setup Time	5.5		nS	6	
t_{22a}	AHOLD Setup Time	6.0		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25a}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)

Table 14. TCP Pentium® Processor with Voltage Reduction Technology AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	6	(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs	6	(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)

Table 14. TCP Pentium® Processor with Voltage Reduction Technology AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

4.3.5. AC TIMINGS FOR A 60-MHz BUS

The AC specifications given in Table 15 consists of output delays, input setup requirements and input hold requirements for the 120-MHz Pentium processor. The AC specifications given in Table 16 consists of output delays, input setup requirements and input hold requirements for the 150-MHz Pentium processor. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz		
t_{1a}	CLK Period	16.67	33.33	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_{6e}	A3-A31, Valid Delay	1.1	6.3	nS	4	(22)
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4), (22)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	4	(22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.5		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	3.0		nS	6	
t_{35}	D0–D63, DP0–7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz		
t_{1a}	CLK Period	16.67	33.33	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	PWT, PCD, BE0-7#, D/C#, CACHE#, SCYC, W/R# Valid Delay	0.8	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_{6e}	A3-A16 Valid Delay	0.7	6.3	nS	4	(22)
t_{6f}	M/IO# Valid Delay	0.85	7.0	nS	4	(22)
t_{6g}	ADS# Valid Delay	0.7	8.5	nS	4	(22)
t_{6h}	A17-A31 Valid Delay	0.8	6.3	nS	4	(22)
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	0.85	8.3	nS	4	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4), (22)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	4	(22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{10b}	HITM# Valid Delay	0.9	6.0	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	0.85	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.5		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	3.0		nS	6	
t_{35}	D0–D63, DP0–7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

4.3.6. AC TIMINGS FOR A 66-MHz BUS

The AC specifications given in Table 17 consist of output delays, input setup requirements and input hold requirements for the 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 17. Mobile Pentium ® Processor AC Specifications for 66-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1)
t_{6a}	PWT, PCD, BE0-7#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	nS	4	
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	
t_{6d}	ADS# Valid Delay	1.0	6.0	nS	4	
t_{6e}	A3-A31 Valid Delay	1.1	6.3	nS	4	
t_{6f}	M/IO# Valid Delay	1.0	5.9	nS	4	
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4)
t_{9a}	BREQ Valid Delay	1.0	8.0	nS	4	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	nS	4	(4)

Table 17. Mobile Pentium ® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{9c}	HLDA Valid Delay	1.0	6.8	nS	4	(4)
t_{10a}	HIT# Valid Delay	1.0	6.8	nS	4	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	4	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		nS	6	
t_{24b}	PEN# Setup Time	4.8		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)

Table 17. Mobile Pentium ® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	2.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS	7	To RESET falling edge (1), (21)

Table 17. Mobile Pentium ® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100 percent tested. Guaranteed by design.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1V/nS rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns ≤ CLK input rise/fall time ≤ 8V/ns.
6. 0.3V/ns ≤ input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.

8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings (t_{55-58}).
11. Setup time is required to guarantee recognition on a specific clock.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5V.
14. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF should be strapped to $V_{CC}3$ or left floating.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
21. BUSCHK# is used as a reset configuration signal to select buffer size.
22. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

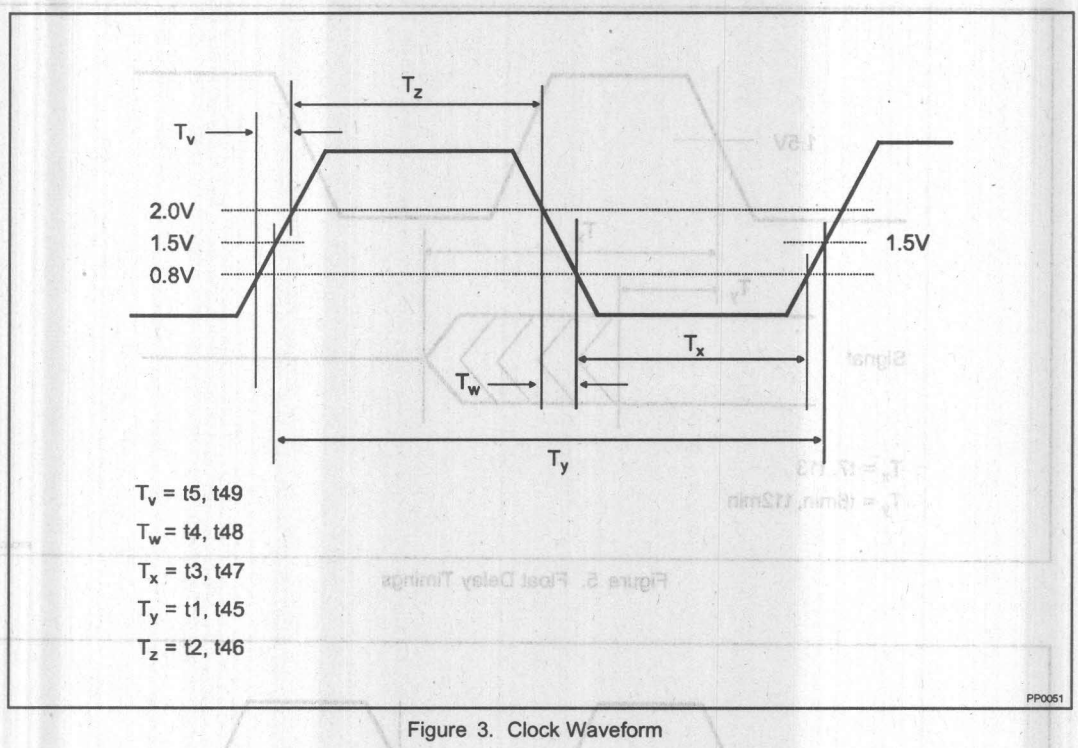


Figure 3. Clock Waveform

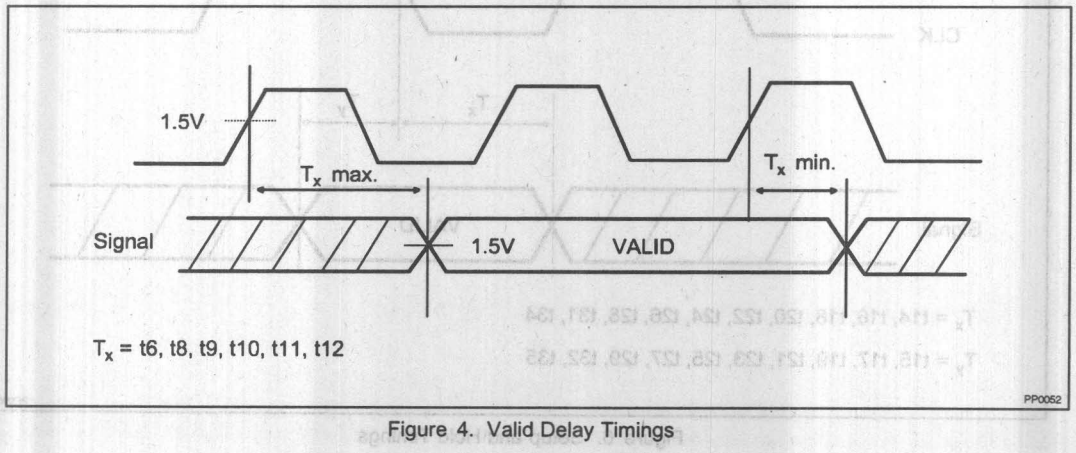


Figure 4. Valid Delay Timings

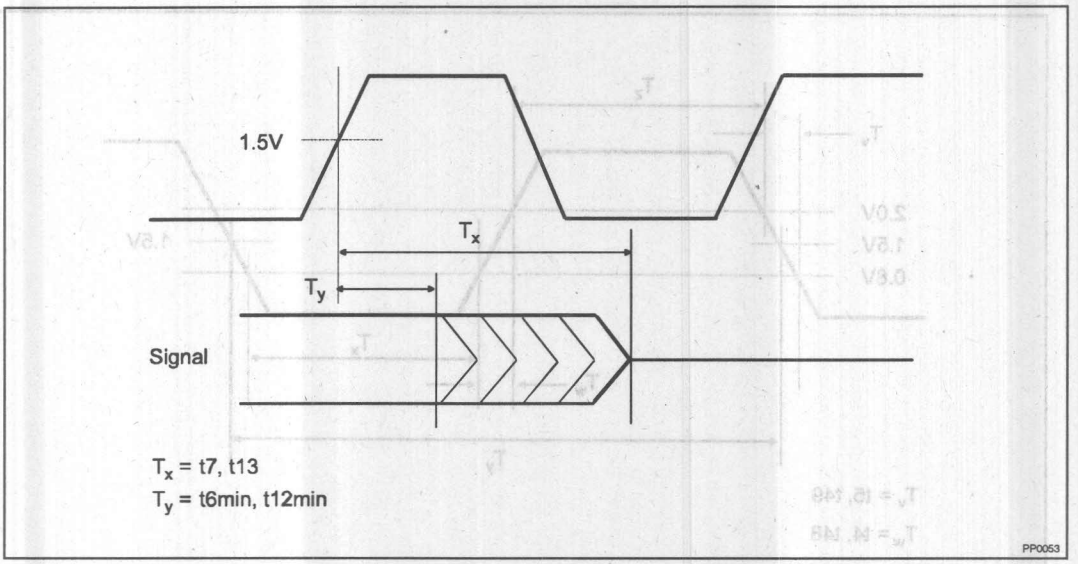


Figure 5. Float Delay Timings

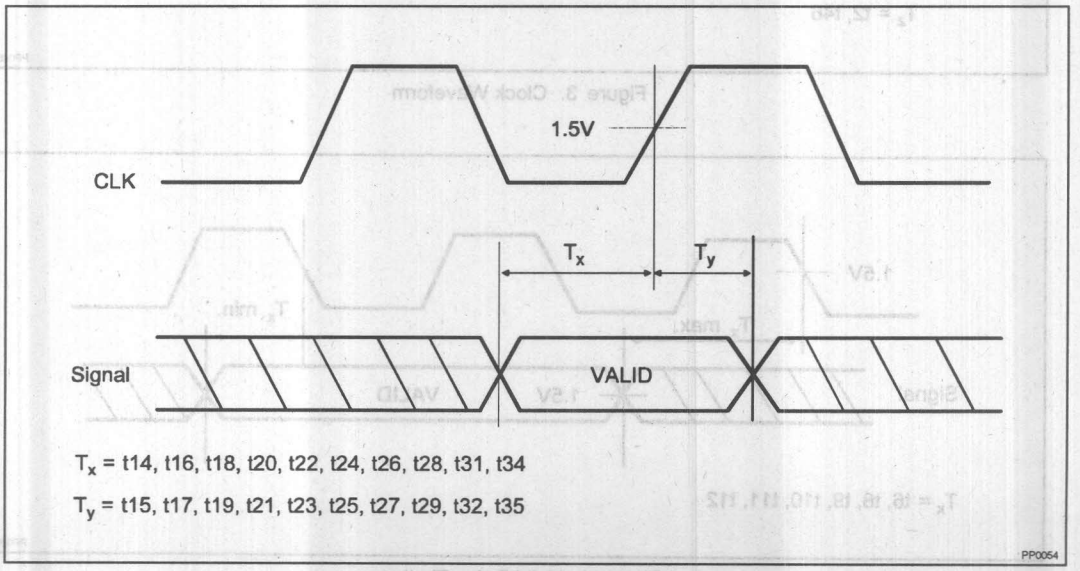


Figure 6. Setup and Hold Timings

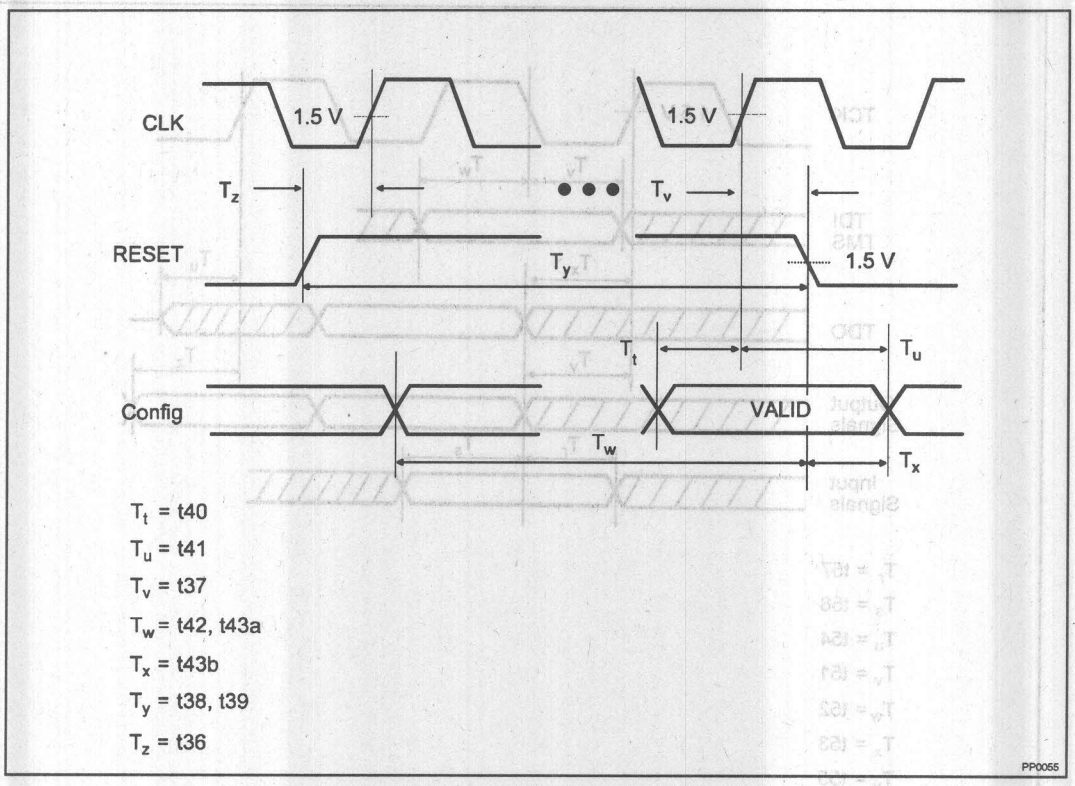


Figure 7. Reset and Configuration Timings

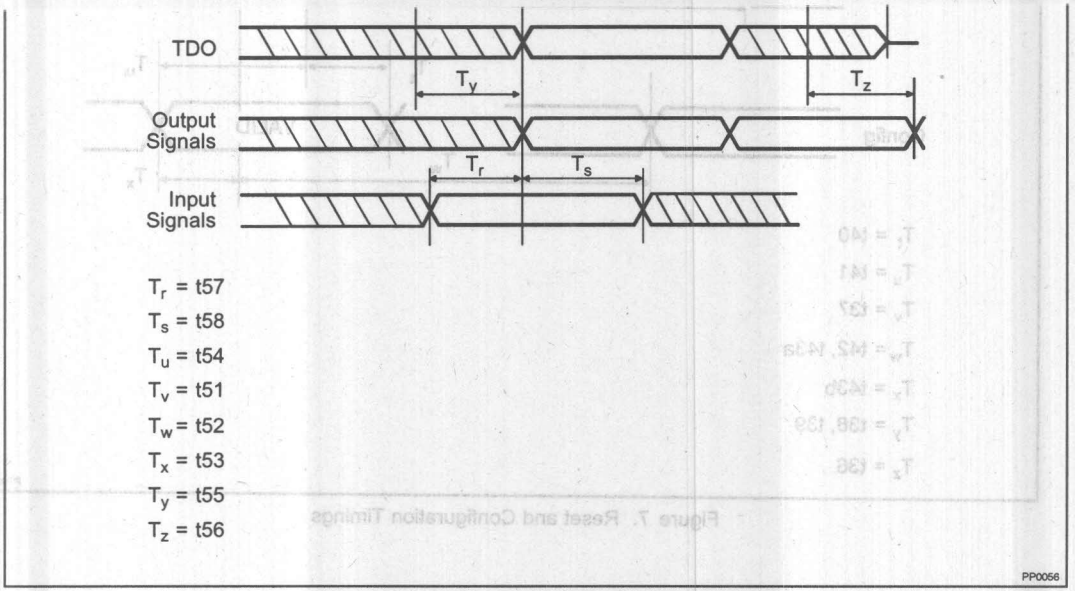


Figure 8. Test Timings

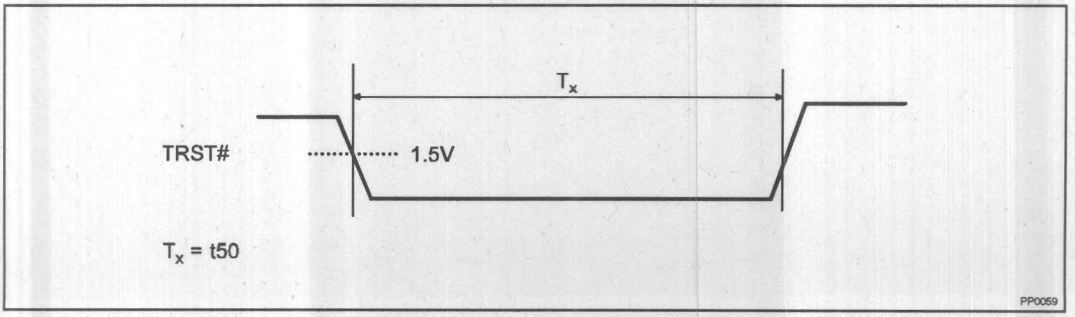


Figure 9. Test Reset Timings

4.4. I/O Buffer Models

This section describes the I/O buffer models of the Pentium processor with voltage reduction technology.

The first order I/O buffer model is a simplified representation of the complex input and output buffers used in the Pentium processor with voltage reduction technology. Figures 10 and 11 show the structure of the input buffer model and Figure 12 shows the output buffer model. Tables 18 and 19 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

The following two models represent the input buffer models. The first model, Figure 10, represents all of the input buffers except for a special group of input buffers. The second model, Figure 11, represents these special buffers. These buffers are the inputs: AHOLD, EADS#, KEN#, WB/WT#, INV, NA#, EWBE#, BOFF# and CLK.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.

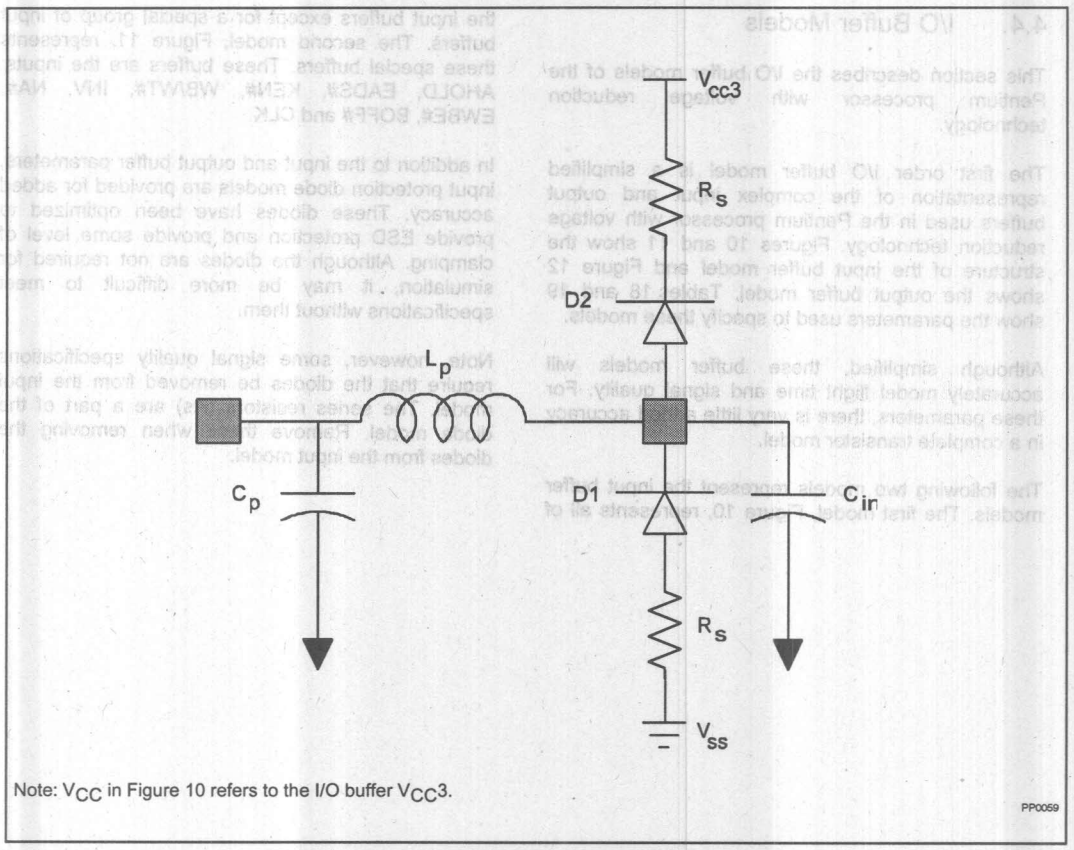


Figure 10. Input Buffer Model, Except Special Group

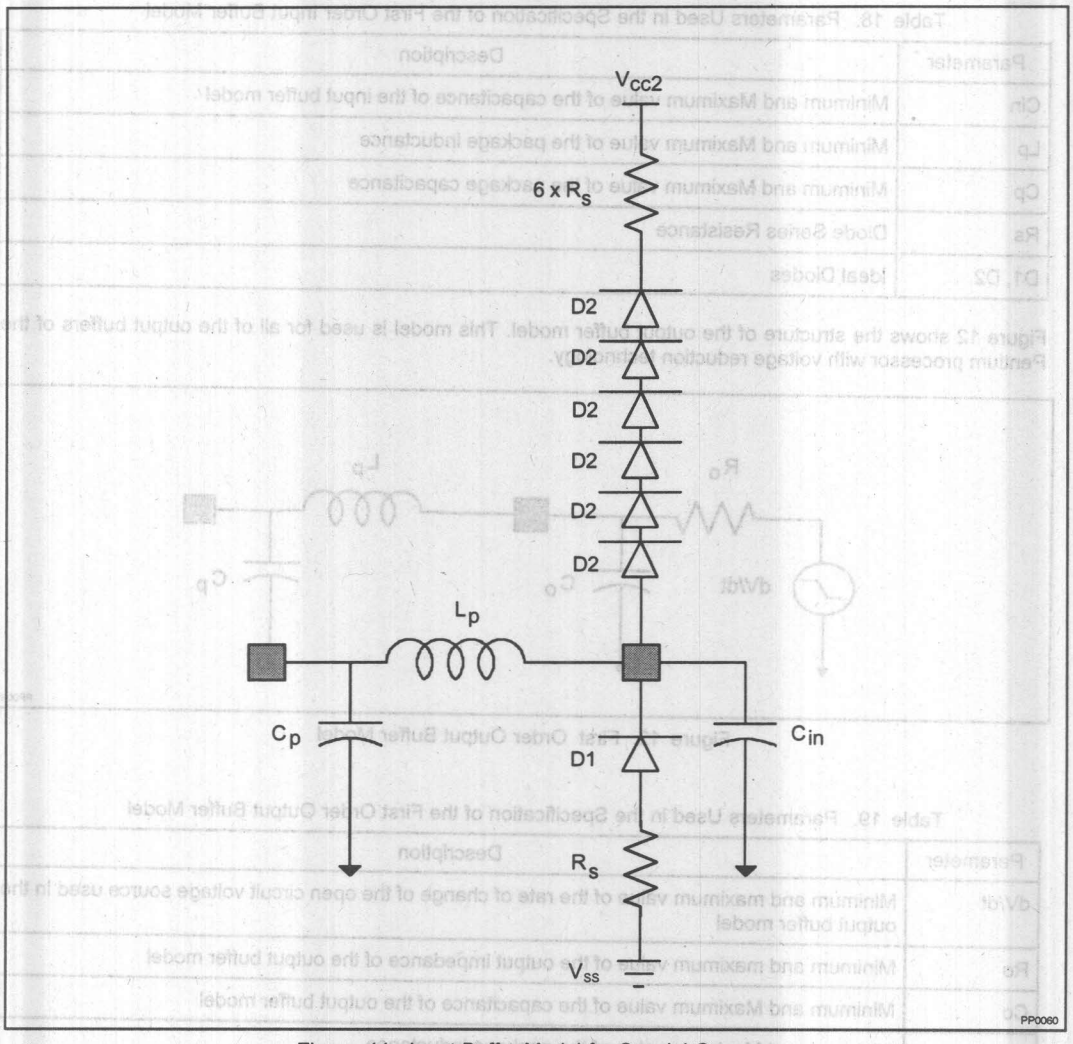


Figure 11. Input Buffer Model for Special Group

Table 18. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
Cin	Minimum and Maximum value of the capacitance of the input buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance
Rs	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 12 shows the structure of the output buffer model. This model is used for all of the output buffers of the Pentium processor with voltage reduction technology.

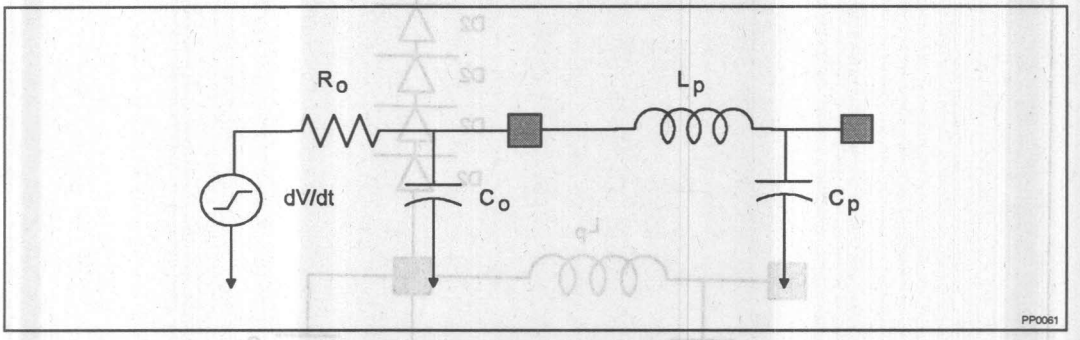


Figure 12. First Order Output Buffer Model

Table 19. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
Ro	Minimum and maximum value of the output impedance of the output buffer model
Co	Minimum and Maximum value of the capacitance of the output buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance

4.4.1. BUFFER MODEL PARAMETERS

This section gives the parameters for each TCP Pentium processor with voltage reduction technology input, output and bidirectional signal, as well as the settings for the configurable buffers.

Some pins on the TCP Pentium processor with voltage reduction technology have selectable buffer sizes. These pins use the configurable output buffer EB2. Table 20 shows the drive level for BRDY# required at the falling edge of RESET to select the buffer strength. The buffer sizes selected should be the appropriate size required; otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices; all of the configurable buffers get set to the same size at the same time.

The input, output and bidirectional buffer values of the TCP Pentium processor with voltage reduction technology are listed in Table 22. This table contains listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the Cin, Cp and Lp values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 21 for the groupings of the buffers.

Table 20. Buffer Selection Chart

Environment	BRDY#	Buffer Selection
Typical Stand Alone Component	1	EB2
Loaded Component	0	EB2A

NOTES:
For correct buffer selection, the BUSCHK# signal must be held inactive (high) at the falling edge of RESET.

Table 21. TCP Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF[1:0], BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE[7:5]#, BP[3:2], BREQ, FERR#, HLDA, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, U/O#	O	ED1	
A[31:21], AP, BE[4:0]#, CACHE#, D/C#, D[63:0], DP[8:0], LOCK#, M/IO#, SCYC	I/O	EB1	EB1
A[20:3], ADS#, HITM#, W/R#	I/O	EB2/EB2A	EB2/EB2A
HIT#	I/O	EB3	EB3

Table 22. TCP Pentium ® Processor Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/nsec)		Ro (Ohms)		Cp (pF)		Lp (nH)		Co/Cin (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0	Rising					0.3	0.4	3.9	5.0	0.8	1.2
(input)	Falling					0.3	0.4	3.9	5.0	0.8	1.2
ER1	Rising					0.2	0.5	3.1	6.0	0.8	1.2
(input)	Falling					0.2	0.5	3.1	6.0	0.8	1.2
ED1	Rising	3/3.0	3.7/0.9	21.6	53.1	0.3	0.6	3.7	6.6	2.0	2.6
(output)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.3	0.6	3.7	6.6	2.0	2.6
EB1	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.5	2.9	6.1	2.0	2.6
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.5	2.9	6.1	2.0	2.6
EB2	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.5	3.1	6.4	9.1	9.7
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.5	3.1	6.4	9.1	9.7
EB2A	Rising	3/2.4	3.7/0.9	10.1	22.4	0.2	0.5	3.1	6.4	9.1	9.7
(bidir)	Falling	3/2.4	3.7/0.9	9.0	21.2	0.2	0.5	3.1	6.4	9.1	9.7
EB3	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.4	3.2	4.1	3.3	3.9
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.4	3.2	4.1	3.3	3.9

Table 23. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e-14A	2.78e-16A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983V	0.967V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

4.4.2. SIGNAL QUALITY SPECIFICATIONS

Signals driven by the system into the Pentium processor with voltage reduction technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: Ringback and Settling Time.

4.4.2.1. Ringback

Excessive ringback can contribute to long-term reliability degradation of the Pentium processor with voltage reduction technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below $V_{CC}3$ (or above V_{SS}) relative to $V_{CC}3$ (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

Maximum Ringback on Inputs = 0.8V (with diodes)

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (Undershoot) is the absolute value of the maximum voltage above $V_{CC}3$ (below V_{SS}). The guideline assumes the absence of diodes on the input.

- Maximum Overshoot/Undershoot on 5V 82497 Cache Controller, and 82492 Cache SRAM Inputs (CLK and PICCLK only) = 1.6V above $V_{CC}5$ (without diodes)
- Maximum Overshoot/Undershoot on 3.3V Pentium processor with voltage reduction technology Inputs (not CLK) = 1.4V above $V_{CC}3$ (without diodes)

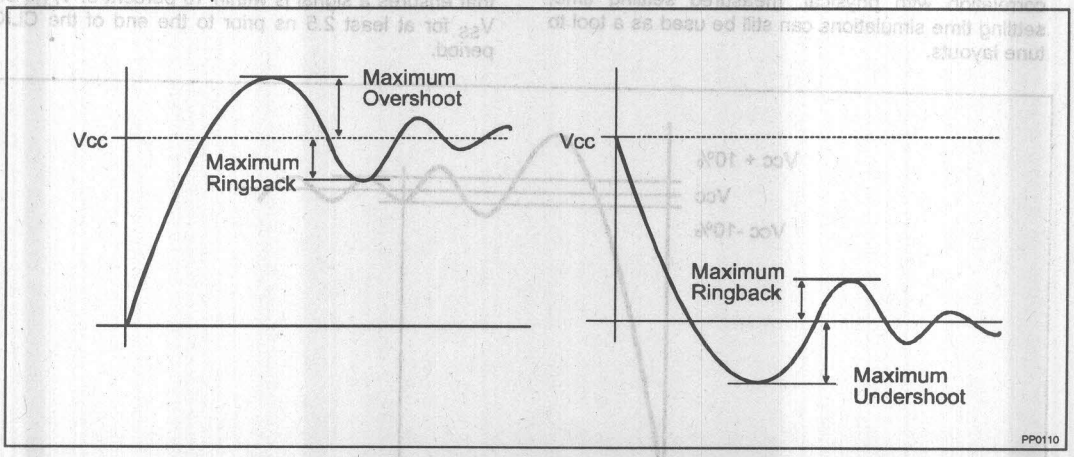


Figure 13. Overshoot/Undershoot and Ringback Guidelines

4.4.2.2. Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10 percent of $V_{CC}3$ or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

- Simulate settling time at the slow corner for a particular signal.
- If settling time violations occur, simulate signal trace with D.C. diodes in place at the receiver pin. The D.C. diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
- If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
- If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.
- Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

A typical design method would include a settling time that ensures a signal is within 10 percent of $V_{CC}3$ or V_{SS} for at least 2.5 ns prior to the end of the CLK period.

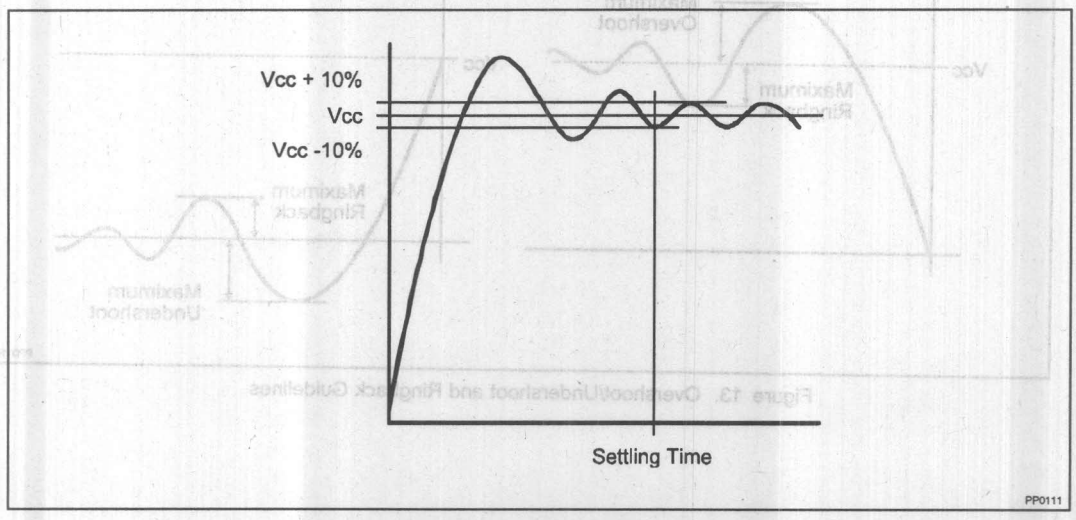


Figure 14. Settling Time

5.0. TCP PENTIUM ® PROCESSOR MECHANICAL SPECIFICATIONS

Today's portable computers face the challenge of meeting desktop performance in an environment that is constrained by thermal, mechanical and electrical design considerations. These considerations have driven the development and implementation of Intel's Tape Carrier Package (TCP). The Intel TCP has been designed to offer a high pin count, low profile, reduced footprint package with uncompromised thermal and electrical performance. Intel continues to provide packaging solutions that meet our rigorous criteria for quality and performance, and this new entry into the Intel package portfolio is no exception.

Key features of the TCP include: surface mount technology design, lead pitch of 0.25 mm, polyimide body size of 24 mm and polyimide up for pick-and-place handling. TCP components are shipped with the leads flat in slide carriers, and are designed to be excised and lead formed at the customer manufacturing site. Recommendations for the manufacture of this package are included in Chapter 12 of the 1996 Packaging Data Book.

Figure 15 shows a cross-sectional view of the TCP as mounted on the Printed Circuit Board. Figures 16 and 17 show the TCP as shipped in its slide carrier, and key dimensions of the carrier and package. Figure 18 shows a cross-section detail of the package. Figure 19 shows an enlarged view of the outer lead bond area of the package.

Tables 24 and 25 provide the Pentium processor with voltage reduction technology TCP dimensions.

5.1. TCP Mechanical Diagrams

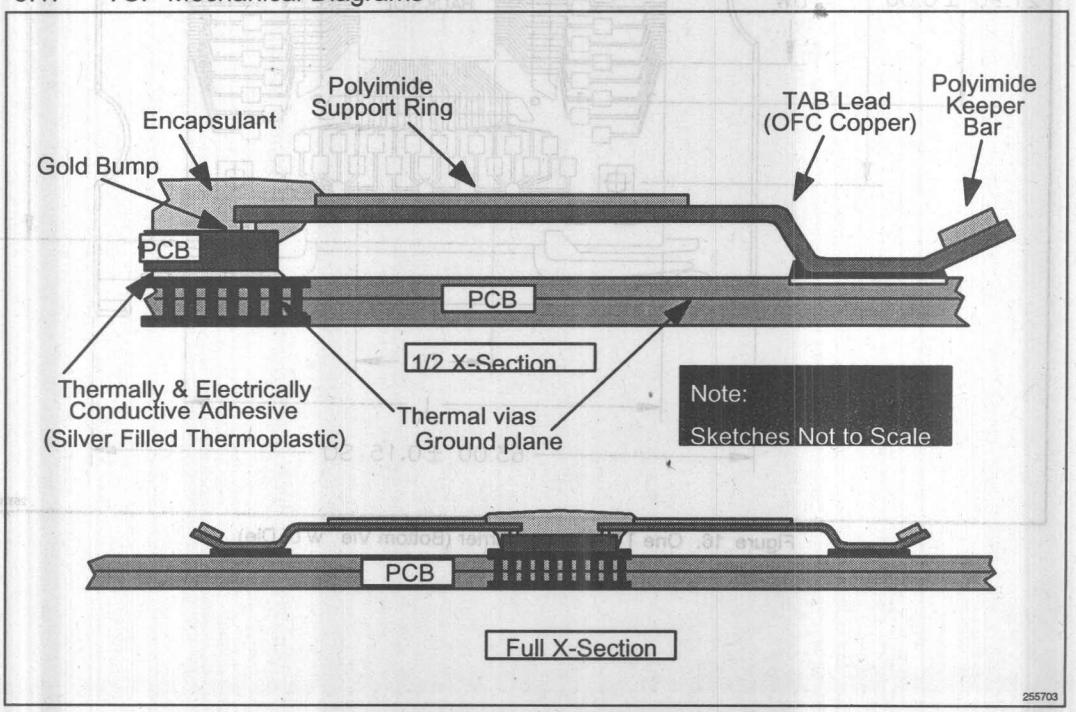


Figure 15. Cross-Sectional View of the Mounted TCP

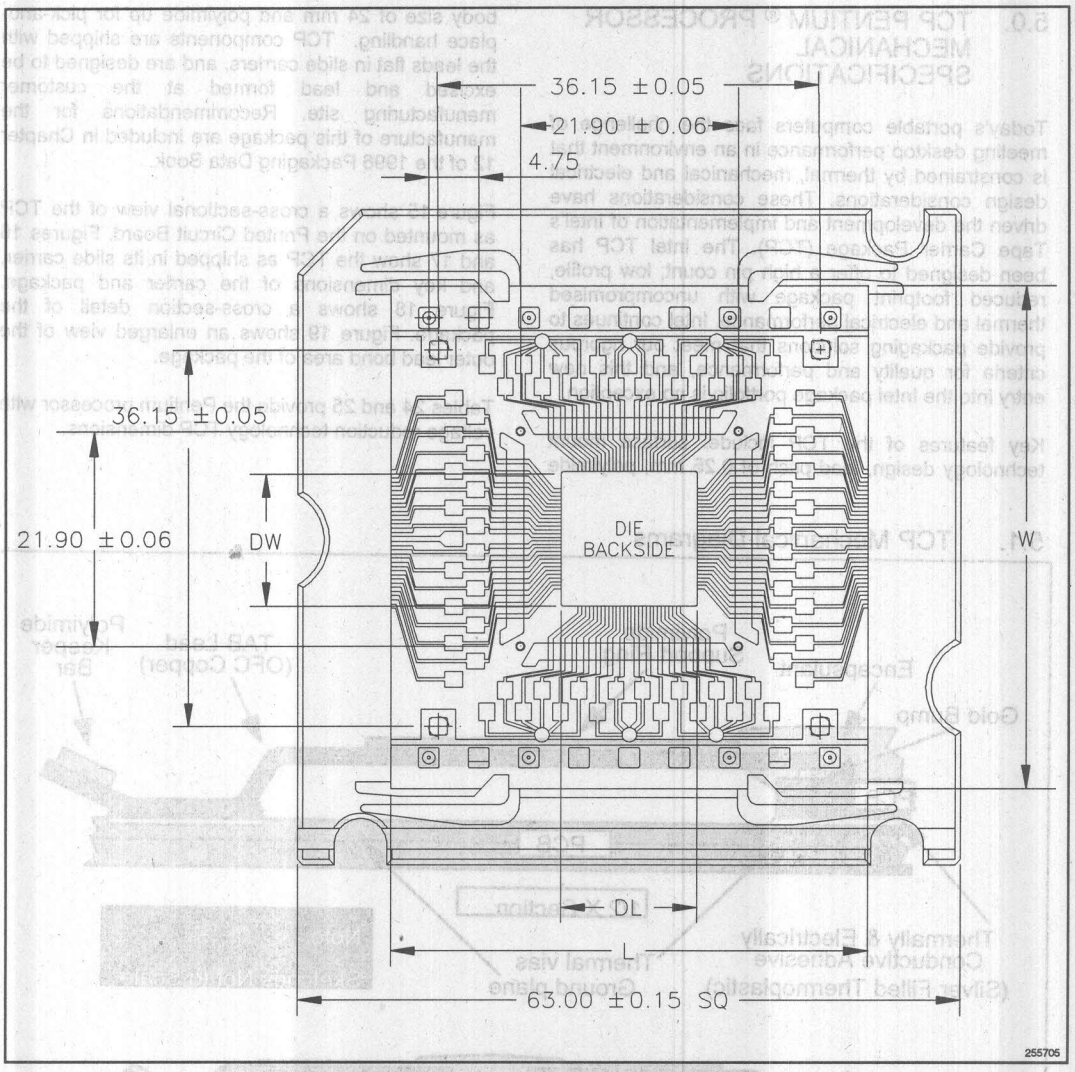


Figure 16. One TCP Site in Carrier (Bottom Vie w of Die)

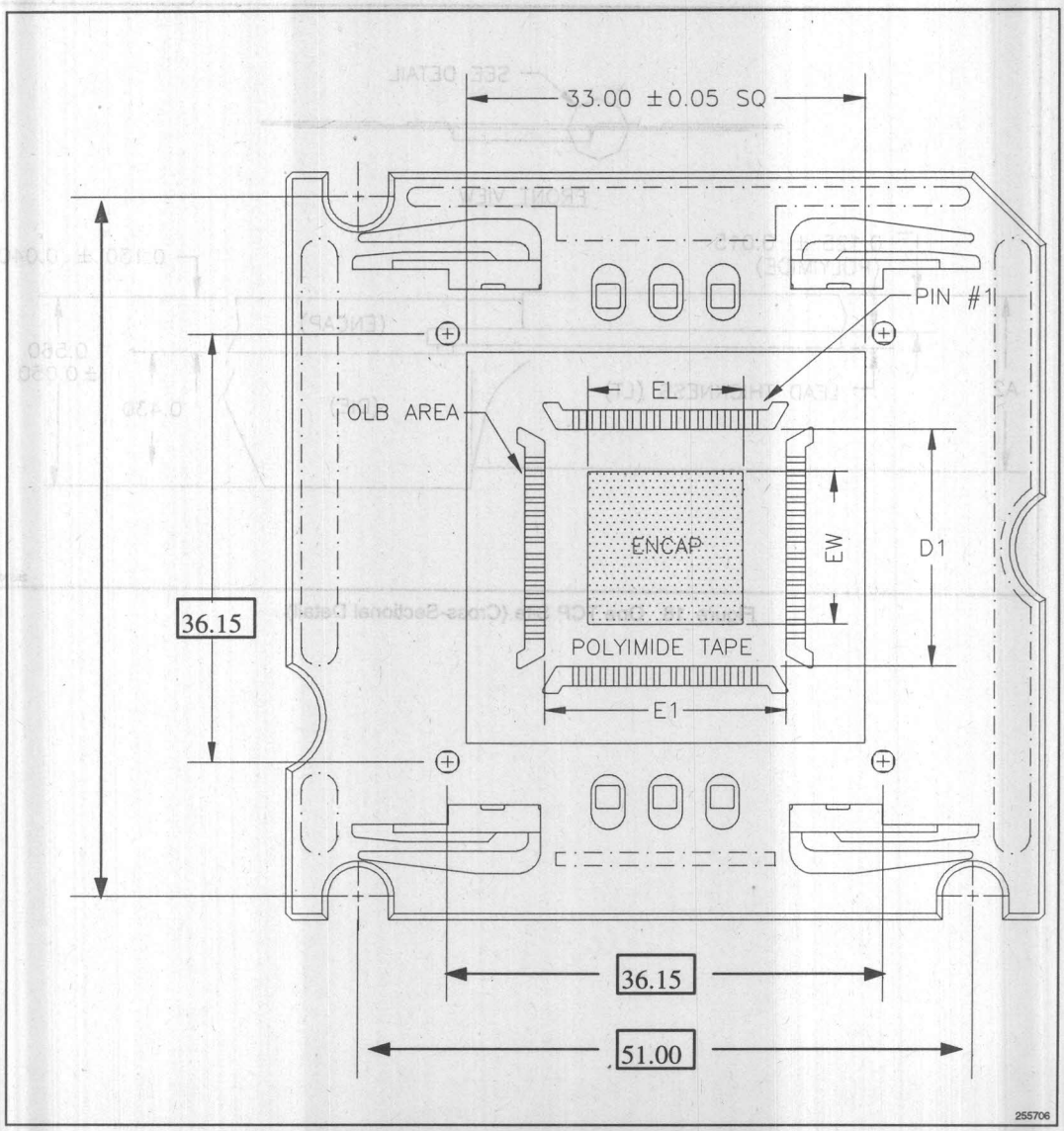


Figure 17. One TCP Site in Carrier (Top View of Die)

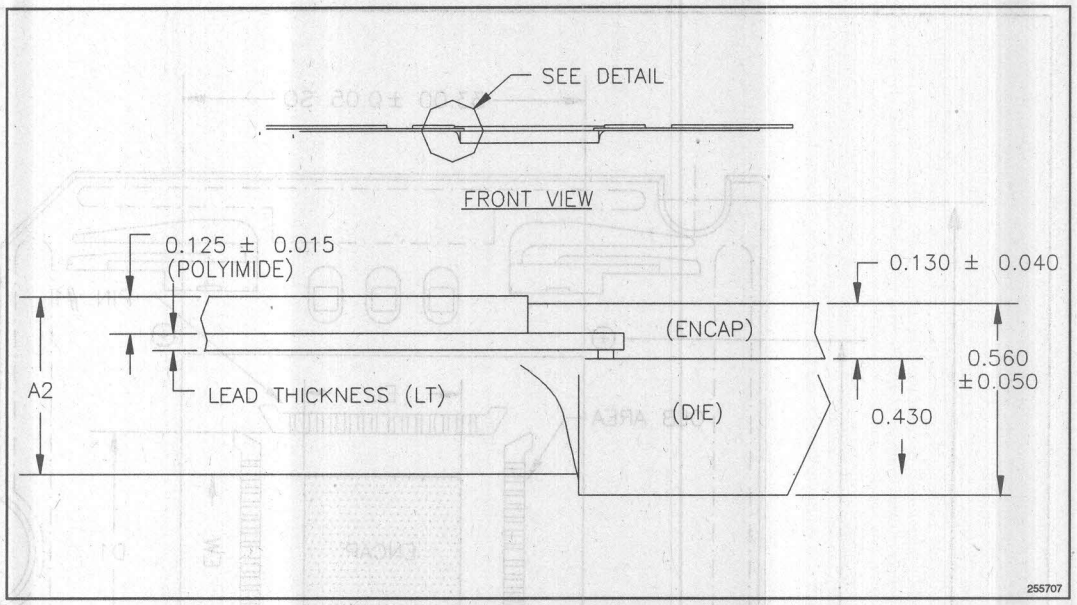


Figure 18. One TCP Site (Cross-Sectional Detail)

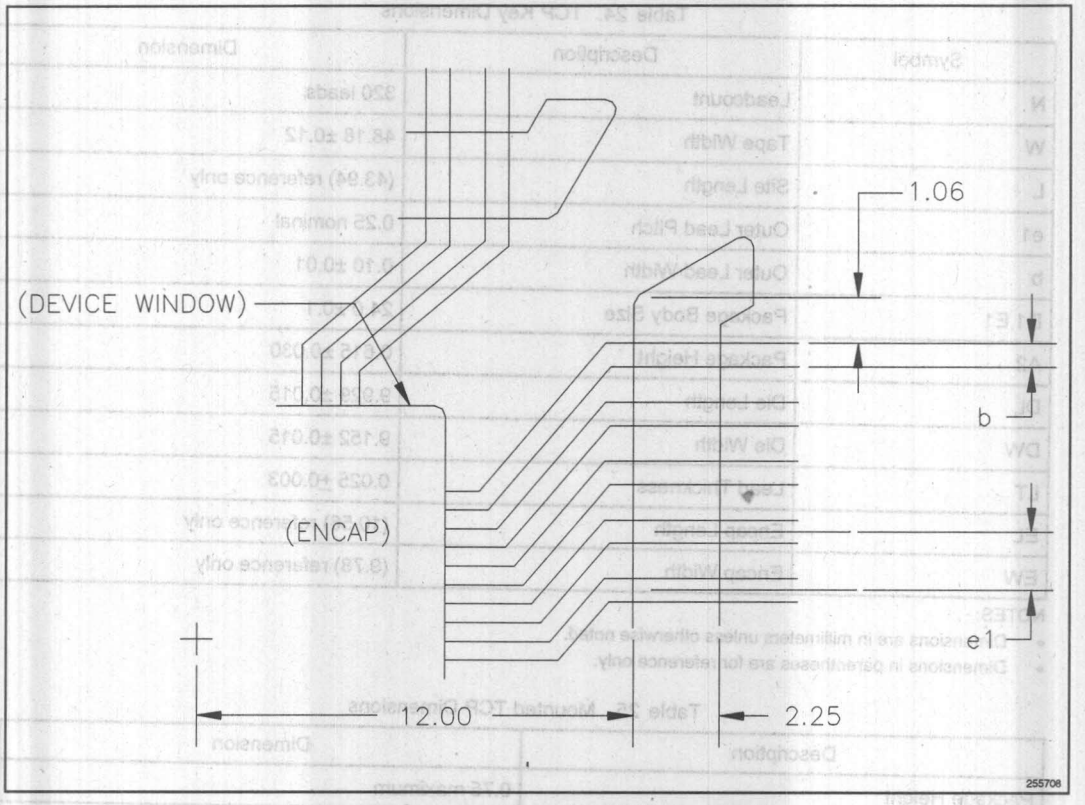


Figure 19. Outer Lead Bond (OLB) Window Detail

Table 24. TCP Key Dimensions

Symbol	Description	Dimension
N	Leadcount	320 leads
W	Tape Width	48.18 ±0.12
L	Site Length	(43.94) reference only
e1	Outer Lead Pitch	0.25 nominal
b	Outer Lead Width	0.10 ±0.01
D1,E1	Package Body Size	24.0 ±0.1
A2	Package Height	0.615 ±0.030
DL	Die Length	9.929 ±0.015
DW	Die Width	9.152 ±0.015
LT	Lead Thickness	0.025 ±0.003
EL	Encap Length	(10.56) reference only
EW	Encap Width	(9.78) reference only

NOTES:
- Dimensions are in millimeters unless otherwise noted.
- Dimensions in parentheses are for reference only.

Table 25. Mounted TCP Dimensions

Description	Dimension
Package Height	0.75 maximum
Terminal Dimension	29.5 nominal
Package Weight	0.5 g maximum

NOTES:
- Dimensions are in millimeters unless otherwise noted.
- Package terminal dimension (lead tip-to-lead tip) assumes the use of a keeper bar.

6.0. TCP PENTIUM ® PROCESSOR THERMAL SPECIFICATIONS

The TCP Pentium processor with voltage reduction technology is specified for proper operation when the case temperature, T_{CASE}, (T_C) is within the specified range of 0 °C to 95 °C.

6.1. Measuring Thermal Values

To verify that the proper T_C (case temperature) is maintained for the Pentium processor, it should be measured at the center of the package top surface (encapsulant). To minimize any measurement errors, the following techniques are recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using highly thermally conductive cements. Intel's laboratory testing was done by using Omega Bond (part number: OB-100).
- The thermocouple should be attached at a 90° angle as shown in Figure 20.

6.2. Thermal Equations

For the Pentium processor with voltage reduction technology, an ambient temperature (T_A) is not specified directly. The only requirement is that the case temperature (T_C) is met. The ambient temperature can be calculated from the following equations:

$$T_J = T_C + P \times \theta_{JC}$$

$$T_A = T_J - P \times \theta_{JA}$$

$$T_A = T_C - (P \times \theta_{CA})$$

$$T_C = T_A + P \times [\theta_{JA} - \theta_{JC}]$$

$$\theta_{CA} = \theta_{JA} - \theta_{JC}$$

where,

T_A and T_C are ambient and case temperatures (°C)

θ_{CA} = Case-to-Ambient thermal resistance (°C/W)

θ_{JA} = Junction-to-Ambient thermal resistance (°C/W)

θ_{JC} = Junction-to-Case thermal resistance (°C/W)

P = maximum power consumption (Watts)

P (maximum power consumption) is specified in section 4.2.

6.3. TCP Thermal Characteristics

The primary heat transfer path from the die of the TCP is through the back side of the die and into the PC board. There are two thermal paths traveling from the PC board to the ambient air. One is the spread of heat within the board and the dissipation of heat by the board to the ambient air. The other is the transfer of heat through the board and to the opposite side where thermal enhancements (e.g., heat sinks, pipes) are attached. Solder-side heat sinking, compared to TCP component-side heat sinking, is the preferred method due to reduced risk of die damage, easier mechanical implementation and larger surface area for attachment. However, component-side heat sinking is possible. The design requirements in a component-side thermal solution are: no direct loading of inner lead bonds on the TCP, a maximum force of 4.5 kgf on the center of a clean TCP, no direct loading of the TAB tape or outer lead bonds and controlled board deflection.

6.4. PC Board Enhancements

Copper planes, thermal pads, and vias are design options that can be used to improve heat transfer from the PC board to the ambient air. Tables 26 and 27 present thermal resistance data for copper plane thickness and via effects. It should be noted that although thicker copper planes will reduce the θ_{CA} of a system without any thermal enhancements, they have less effect on the θ_{CA} of a system with thermal enhancements. However, placing vias under the die will reduce the θ_{CA} of a system with and without thermal enhancements.

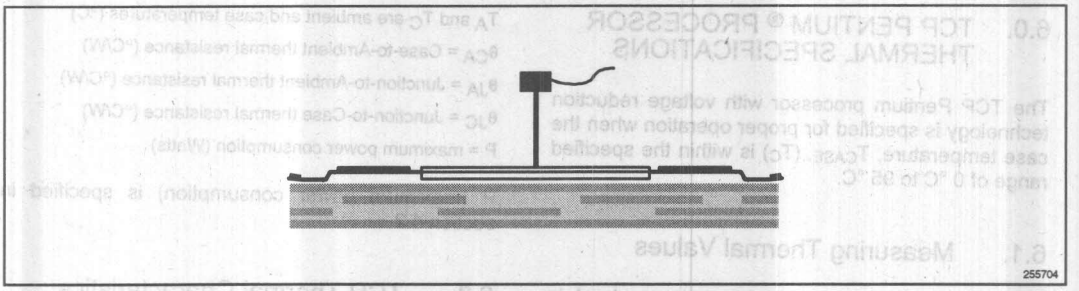


Figure 20. Technique for Measuring Case Temperature (T_C)

Table 26. Thermal Resistance vs. Copper Plane Thickness with and without Enhancements

Copper Plane Thickness*	θ_{CA} (°C/W) No Enhancements	θ_{CA} (°C/W) With Heat Pipe
1 oz. Cu	18	8
3 oz. Cu	14	8

NOTES:
*225 vias underneath the die
(1 oz = 1.3 mil)

Table 27. Thermal Resistance vs. Thermal Vias underneath the Die

Thermal Via Configuration	θ_{CA} (°C/W) No Enhancements
No thermal vias	15
20 mil drill on 40 mil pitch	13

Table 28. Pentium® Processor TCP Thermal Resistance without Enhancements

	θ_{JC} (°C/W)	θ_{CA} (°C/W)
Thermal Resistance without Enhancements	0.8	13.9

Table 29. Pentium ® Processor TCP Thermal Resistance with Enhancements (without Airflow)

Thermal Enhancements	θ_{CA} (°C/W)	Notes
Heat sink	11.7	1.2"x1.2"x.35"
Al Plate	8.7	4"x4"x.030"
Al Plate with Heat Pipe	7.8	0.3"x1"x4"

Table 30. Pentium ® Processor TCP Thermal Resistance with Enhancements (with Airflow)

Thermal Enhancements	θ_{CA} (°C/W)	Notes
Heat sink with Fan @ 1.7 CFM	5.0	1.2"x1.2"x.35" HS 1"x1"x.4" Fan
Heat sink with Airflow @ 400 LFM	5.1	1.2"x1.2"x.35" HS
Heat sink with Airflow @ 600 LFM	4.3	1.2"x1.2"x.35" HS

NOTES:
HS = heat sink
LFM = Linear Feet/Minute
CFM = Cubic Feet/Minute

6.4.1. STANDARD TEST BOARD CONFIGURATION

All TCP thermal measurements provided in the tables were taken with the component soldered to a 2" x 2" test board outline. This six-layer board contains 13.5 mil drill on 40 mil pitch vias (underneath the die) in the die attach pad which are connected to two 3 oz. copper planes located at layers two and five. For the TCP Pentium processor with voltage reduction technology, the vias in the die attach pad should be connected without thermal reliefs to the ground plane(s). The die is attached to the die attach pad using a thermally and electrically conductive adhesive. This test board was designed to optimize the heat spreading into the board and the heat transfer through to the opposite side of the board.

NOTE

Thermal resistance values should be used as guidelines only, and are highly system dependent. Final system verification should always refer to the case temperature specification.

7.0. SPGA PENTIUM ® PROCESSOR WITH VOLTAGE REDUCTION TECHNOLOGY SPECIFICATIONS

7.1. SPGA Pentium ® Processor with Voltage Reduction Technology Differences from 3.3V Pentium Processor

All SPGA Pentium processor with voltage reduction technology specifications, except the differences described in this section, are identical to those of the 3.3V Pentium processor.

7.1.1. FEATURES REMOVED

The following features have been removed for the Pentium processor with voltage reduction technology: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins which exist on the 3.3V Pentium processor but have been removed on the Pentium processor with voltage reduction technology.

7.1.2. MAXIMUM RATING

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the SPGA Pentium processor with voltage reduction technology contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Case temperature under bias ..... –65°C to 110°C

Storage temperature ..... –65°C to 150°C

3V Supply voltage
with respect to V_{SS} ..... –0.5V to +4.6V

2.9V Supply voltage
with respect to V_{SS} ..... –0.5V to +4.1V

3V Only Buffer DC Input Voltage..... ...–0.5V to $V_{CC}3$ ..... +0.5; not to exceed 4.6V (2)

5V Safe Buffer
DC Input Voltage.....–0.5V to 6.5V (1,3)

NOTES:
1. Applies to CLK.
2. Applies to all SPGA Pentium processor with voltage reduction technology inputs except CLK.
3. See Table 32.

WARNING

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

7.1.3. DC SPECIFICATIONS

Tables 31, 32 and 33 list the DC specifications which apply to the SPGA Pentium processor with voltage reduction technology. The SPGA Pentium processor with voltage reduction technology core operates at 2.9V (3.1V for 150 MHz) internally while the I/O interface operates at 3.3V. The CLK input may be at 3.3V or 5V. Since the 3.3V (5V safe) input levels defined in Table 32 are the same as the 5V TTL levels, the CLK input is compatible with existing 5V clock drivers. The power dissipation specification in Table 34 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

Table 31. SPGA 3.3V DC Specifications

T_{CASE} = 0 to 85°C; $V_{CC}2$ = 2.9V ±165mV; $V_{CC}3$ = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level (3)
V_{IH3}	Input High Voltage	2.0	$V_{CC}3$+0.3	V	TTL Level (3)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1) (3)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}2$	Power Supply Current from 2.9V core supply		2085 2500 2775	mA mA mA	@100 MHz (4) @120 MHz (4) @133 MHz (4)
$I_{CC}3$	Power Supply Current from 3.3V I/O buffer supply		355 320 355	mA mA mA	@100 MHz (4) @120 MHz (4) @133 MHz (4)

NOTES:
1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK.
4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and $V_{CC}2$ = 2.9V ± 165mV and $V_{CC}3$ = 3.3V± 165mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes.

Table 32. 3.3V (5V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	–0.3	0.8	V	TTL Level (1)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTES:
1. Applies to CLK only.

Table 33. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4V (3)
I_{IL}	Input Leakage Current		–400	µA	V_{IN} = 0.4V (2)

NOTES:
1. This parameter is for input without pull up or pull down.
2. This parameter is for input with pull up.
3. This parameter is for input with pull down.
4. Guaranteed by design.

Table 34. Power Dissipation Requirements for Thermal Design

Parameter	Typical (1)	Max (2)	Unit	Notes
Thermal Design Power (5)		5.9	Watts	@100 MHz
		7.1	Watts	@120 MHz
		7.9	Watts	@133 MHz
Active Power (6)	2.0--3.0	N/A	Watts	@100 MHz
	2.5--3.5		Watts	@120 MHz
	3.0--4.0		Watts	@133 MHz
Stop Grant / Auto Halt Power		1.2	Watts	@100 MHz (3)
		1.2	Watts	@120 MHz (3)
		1.3	Watts	@133 MHz (3)
Stop Clock Power	.02	0.05	Watts	(4)

NOTES:

1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at $V_{CC}2$ = 2.9V (3.1V for 150 MHz) and $V_{CC}3$ = 3.3V running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum Active Power Dissipation. It is determined using a worst-case instruction mix with $V_{CC}2$ = 2.9V (3.1V for 150 MHz) and $V_{CC}3$ = 3.3V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. Thermal Design Power is the maximum power dissipation under normal operating conditions at nominal $V_{CC}2$ worst case temperature, while executing the worst case power instruction mix.
6. Active Power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.

7.1.3.1. Power Sequencing

There is no specific sequence required for powering up or powering down the $V_{CC}2$ and $V_{CC}3$ power supplies. However, for compatibility with future mobile processors, it is recommended that the $V_{CC}2$ and $V_{CC}3$ power supplies be either both on or both off within one second of each other.

7.1.4. AC SPECIFICATIONS

The AC specifications of the SPGA Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All SPGA Pentium processor with voltage reduction technology AC specifications are valid for $V_{CC}2$ = 2.9V (3.1V for 150 MHz) $\pm$ 165mV, $V_{CC}3$ = 3.3V $\pm$ 165mV, and T_{CASE} = 0 to 85°C.

7.1.4.1. Power and Ground

For clean on-chip power distribution, the SPGA Pentium processor with voltage reduction technology has 25 $V_{CC}2$ (2.9V power), 28 $V_{CC}3$ (3.3V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external $V_{CC}2$, $V_{CC}3$ and V_{SS} pins of the SPGA Pentium processor with voltage reduction technology. On the circuit board all $V_{CC}2$ pins must be connected to a 2.9V (3.1V for 150 MHz) $V_{CC}2$ plane (or island) and all $V_{CC}3$ pins must be connected to a 3.3V $V_{CC}3$ plane. All V_{SS} pins must be connected to a V_{SS} plane. Refer to Table 35 for a listing of $V_{CC}2$ and $V_{CC}3$.

7.1.4.2. Decoupling Recommendations

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane and the 2.9V plane (or island). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3V plane and the 2.9V (3.1V for 150 MHz) plane (or island)) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed informations, please contact Intel or refer to the Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems application note (Order Number 242558).

7.1.4.3. Connection Specifications

All NC pins must remain unconnected. Refer to Table 35 for a listing of NC pins.

All RESERVED pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active high inputs should be connected to ground.

7.1.4.4. AC Timings

Follow Table 15 or 16 for the SPGA Pentium processor with voltage reduction technology AC timing changes for 60-MHz bus operation. Follow Table 17 for the SPGA Pentium processor with voltage reduction technology AC timing for 66-MHz bus operation.

7.1.5. THERMAL SPECIFICATIONS

The SPGA Pentium processor with voltage reduction technology is specified for proper operation when the case temperature, T_{CASE} (T_C) is within the specified range of 0 °C to 85 °C.

7.1.6. SPGA PACKAGE DIFFERE NCES

The SPGA Pentium processor with voltage reduction technology package has a pin array that is mechanically identical to the SPGA version of the 3.3V Pentium, but some pins need to be connected differently. Also, there are small differences in the package dimensions.

7.1.6.1. Pinout

Table 35 lists the SPGA Pentium processor with voltage reduction technology pins that are different from the SPGA 3.3V Pentium processor. Figure 21 depicts the pin side SPGA pinout diagram. The $V_{CC}2$ pins are 3.3V V_{CC} pins for the 3.3V Pentium processor, but will be 2.9V (3.1V for 150 MHz) $V_{CC}2$ pins for the SPGA Pentium processor with voltage reduction technology. The NC pins correspond to the unused (for mobile) functions listed in Table 1. They should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings. For a brief functional description of the remaining pins, please refer to Tables 3 and 4. For Input and Output pins reference, please refer to Table 6, 7 and 8.

7.1.6.2. Package Dimensions

The Pentium processor with voltage reduction technology implements an SPGA package that removes the Heat spreader from the top of the package. The package is mechanically equivalent to the package used on the 3.3V Pentium processor C2 stepping except that the SPGA Pentium processor with voltage reduction technology will use the metal lid instead of a ceramic lid, and has the dimensions shown in Figure 22.

7.1.7. I/O BUFFER MODELS

The I/O buffer models provided in Section 4.4 of this document apply to both the TCP and SPGA Pentium processor with voltage reduction technology packages, although the capacitance (C_P) and inductance (L_P) parameter values differ between the two packages. For SPGA Pentium processor with voltage reduction technology values, refer to the Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors.

Table 35. SPGA Pentium ® Processor with Voltage Reduction Technology $V_{CC}2$ and $V_{CC}3$ Pins

$V_{CC}2$*				
A17	A07	Q01	AA01	AN11
A15	G01	S01	AC01	AN13
A13	J01	U01	AE01	AN15
A11	L01	W01	AG01	AN17
A09	N01	Y01	AN09	AN19

$V_{CC}3$						
A19	A27	AE37	AN25	G37	N37	U33
A21	A29	AG37	AN27	J37	Q37	U37
A23	AA37	AN21	AN29	L33	S37	W37
A25	AC37	AN23	E37	L37	T34	Y37

NC**				
A37	AE03	AN35	Q35	W33
AA03	AE35	H34	R34	W35
AC03	AL19	J33	S33	Y03
AD04	AM02	L35	S35	Y35

NOTE:

*These $V_{CC}2$ pins are 3.3V V_{CC} pins for the SPGA 3.3V Pentium® processor. For the SPGA Pentium processor with voltage reduction technology, these pins are 2.9V (3.1V for 150 MHz) $V_{CC}2$ supplies for the SPGA core.

**These NC pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

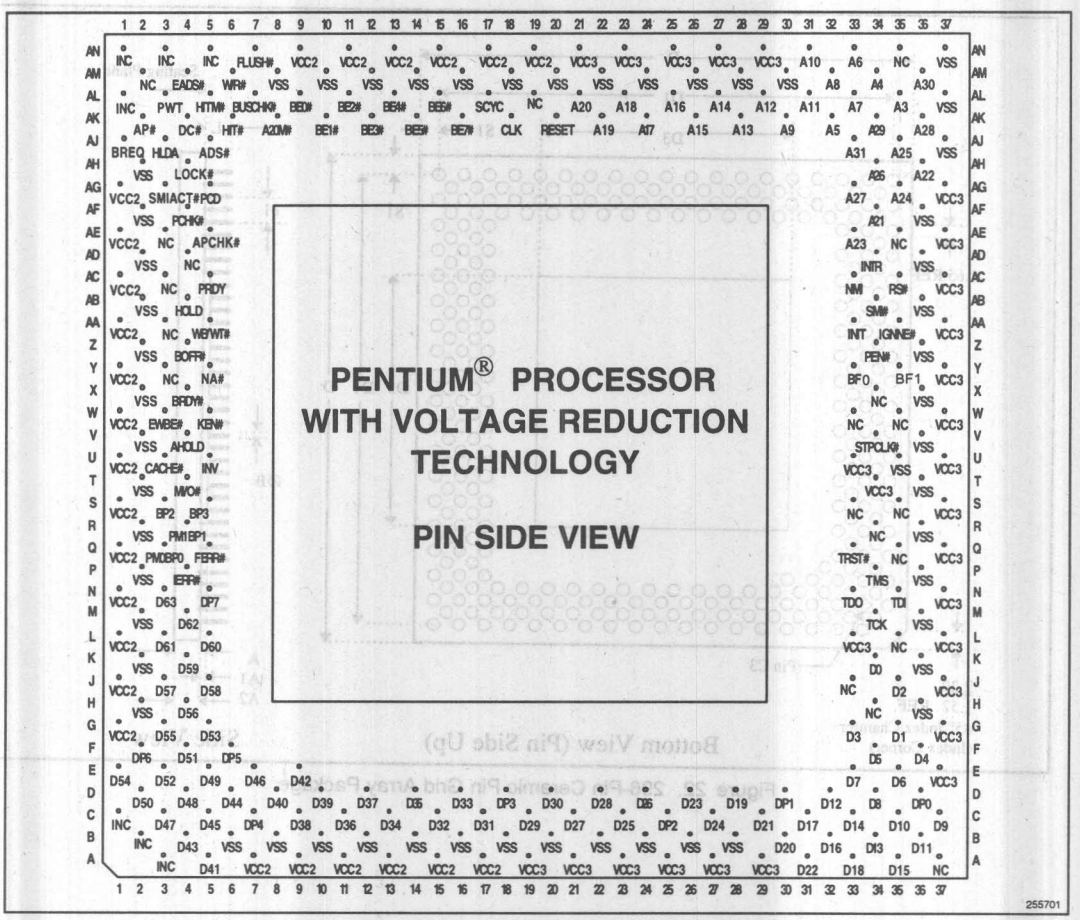


Figure 21. SPGA Pentium ® Processor with Voltage Reduction Technology Pinout

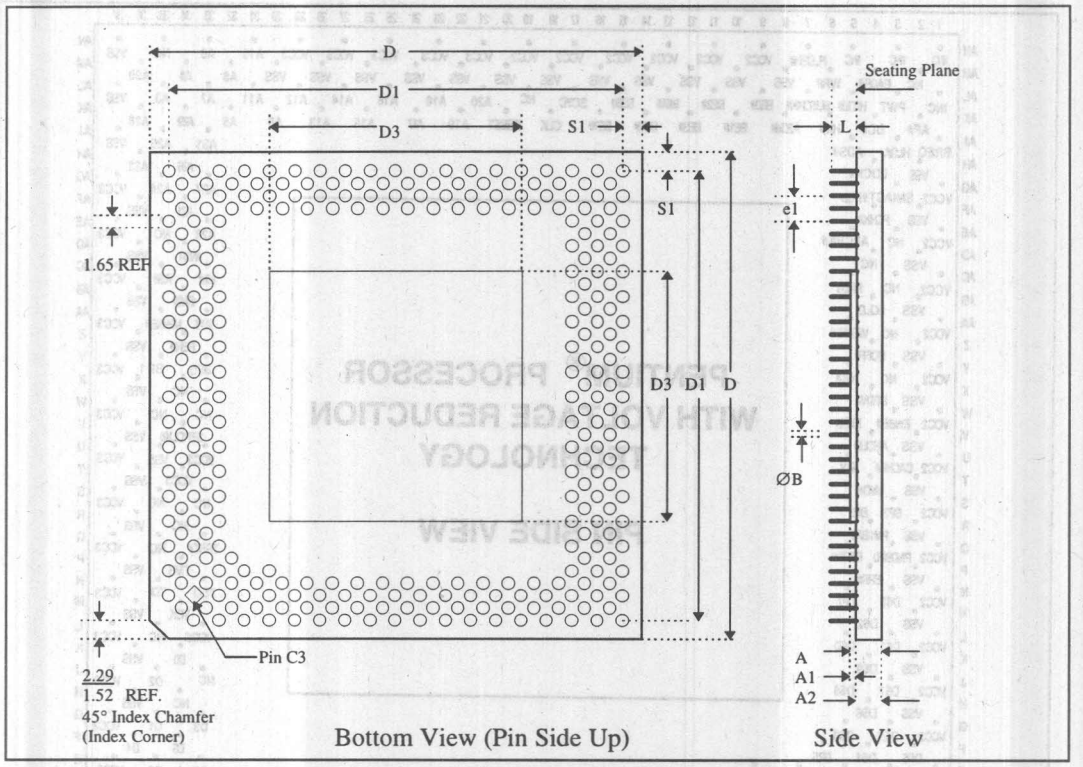


Figure 22. 296-Pin Ceramic Pin Grid Array Package

Table 36. **296-Pin Ceramic Pin Grid Array: The Pac**kage Dimensional Specification

	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.27	3.83	Ceramic Lid	0.129	0.151	Ceramic Lid
A1	0.66	0.86	Ceramic Lid	0.026	0.034	Ceramic Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	1.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.27	3.63	Ceramic Lid	0.129	0.143	Ceramic Lid
A1	0.86	0.96	Ceramic Lid	0.025	0.034	Ceramic Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.29	49.78		1.940	1.960	
D1	48.59	48.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	

Table 35. 296-Pin Ceramic Pin Grid Array: The Package Dimensional Specification

intel®

AP-580

APPLICATION NOTE

Voltage Guidelines for Pentium® Processors with MMX™ Technology

June 1997

Order Number: 243186-003

intel®

AP-580

APPLICATION
NOTE

Voltage Guidelines for Pentium® Processors with MMX™ Technology

June 1997

Order Number 243768-002

1.0. INTRODUCTION

This document explains the voltage specifications, recommends solutions for supplying consistent power, and suggests validation techniques to ensure robust Pentium® processor with MMX™ technology-based systems.

The Pentium processor with MMX technology uses a split power plane with separate voltage islands for the core and I/O. The split power plane has separate Vcc_2 pins connected to the core voltage island, while the Vcc_3 pins are connected to the I/O voltage island.

This document contains guidelines for measuring Vcc noise levels on the Vcc_2 (2.8V) plane of the Pentium processor with MMX technology. The document outlines measurement procedures for a Pentium processor with MMX technology system running at 233 MHz. The Vcc_2 specification for the core is the 2.7V to 2.9V range. The Vcc_3 specification for the I/O voltage island uses the standard 3.3V range from 3.135V to 3.6V. For voltage transient measurement information on Pentium processors, refer to the application note, *Implementation Guidelines for Pentium® Processors with VRE Specifications*, Order Number 242687.

This document contains six key sections:

1. Section 2.0 discusses the core and I/O specifications. This chapter also gives an overview of some important system design and voltage measurement considerations associated with V_{CC}. The consequences of specification violations are also discussed.
2. Section 3.0 deals with the power supply and regulation. It contains voltage regulator and power supply recommendations to ensure a robust system design. In addition, this chapter contains detailed bulk and high-speed decoupling recommendations for Pentium processor designs.
3. Section 4.0 explains the proper measurement techniques to verify that systems meet their respective voltage specifications. These measurement techniques apply to all Pentium processors. Sample measurement results are shown in this chapter.
4. Appendix A provides information on how to obtain and use the recommended "stress" code for voltage noise measurements.
5. Appendix B provides a list of third party vendors. These vendors include suppliers of regulators, resistors, capacitors, and sockets
6. Appendix C provides worksheets for recording measurements.

2.0. SPECIFICATIONS

2.1. The Core and I/O Specification

The Pentium processor with MMX technology has a split power plane with the core operating at 2.8V and the I/O operating at 3.3V. The VCC2DET# pin defined on the Pentium processor with MMX technology is used to indicate to the voltage regulator the correct processor core voltage of 2.8V (Vcc_2 plane). The I/O should meet the standard 3.3V specifications for the voltage supply requirements. Both the core and I/O have strict V_{CC} requirements and are very sensitive to voltage supply noise and transients.

NOTE

Any overshoot or undershoot beyond the voltage range (at a measurement bandwidth of 20 MHz) is outside specifications. Transient excursions beyond the specified voltage range may result in unstable system behavior. The measuring techniques are also specified in Section 4.0 and should be followed to ensure consistent and accurate measurements. The complete specifications shown above must be met to ensure a robust Pentium processor with MMX technology-based platform.

All measurements must be made and guaranteed at the back of the motherboard at the processor socket pins. The voltage specifications assume an oscilloscope measurement bandwidth of 20 MHz. For complete measurement specifications, see Section 4.4.

To compensate for the small transient tolerance, platforms must use accurate voltage regulators and adequate local decoupling capacitors. During worst-case transient conditions (transition into and out of Stop-Grant mode or HALT Power Down mode), current supplied to the processor can change by several amperes in tens of nanoseconds. Since power supply units and voltage regulators can, at best, respond in a time frame on the

required to act as current reservoirs until the power supply unit or voltage regulators compensate for the new load. Due to the high-speed operation of the Pentium processor, high-frequency capacitors are also required to filter the excessive noise components. Failure to provide adequate power regulation during any transient conditions may result in undershoot and overshoot beyond the voltage specifications of the processor.

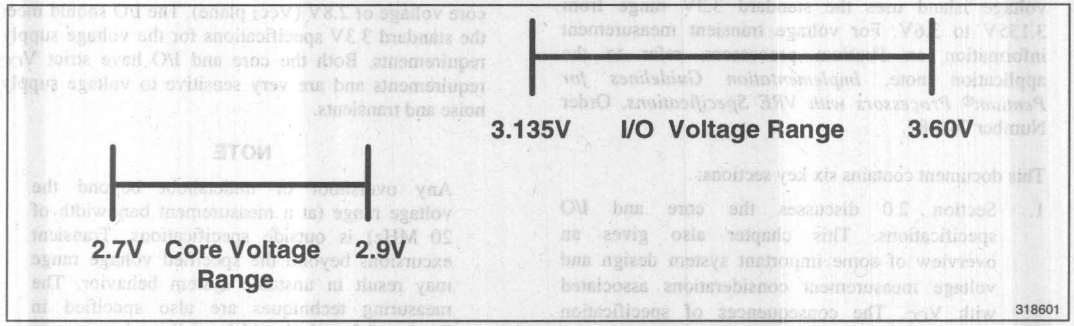


Figure 1. The Core and I/O Voltage Specifications for Pentium® Processors with MMX™ Technology

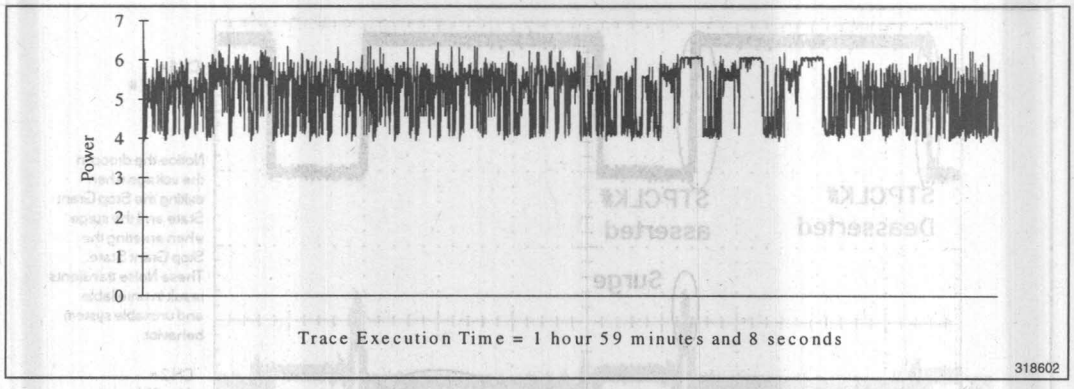


Figure 2. Rapid Fluctuations of System Power during Active Operation (BAPCo93*)

2.2. Typical Application Behavior

Poorly designed desktop and server systems will violate voltage specifications during normal operation. An unusual application instruction mix can cause large current spikes from clock cycle to clock cycle. Figure 2 shows the rapid fluctuations of system power during execution of a BAPCo93* benchmark trace on the Pentium processor (BAPCo93 is a system benchmark used for measuring system performance). These quick transitions in current occur in a shorter time frame than that in which the power supply unit or voltage regulator may be able to respond. Worst-case transients occur during the transition into or out of a low power state. Figure 3 shows an oscilloscope trace of a system using STPCLK# assertion/deassertion to enter/exit the Stop-Grant state. When STPCLK# is deasserted, the supply voltage "droops" due to ESL and ESR effects (see Section 3.6), and because the voltage regulator cannot respond quickly enough to the large, instantaneous change in current. Similarly, when STPCLK# is asserted, the system enters Stop-Grant state, and the supply voltage "surges" because of ESL/ESR effects and the large instantaneous changes in current. Droops and surges also occur in systems with proper decoupling, but to a lesser extent. The system also has high-frequency noise due to high operation speed of the internal core.

NOTE

Violating the voltage specifications by undershooting or overshooting the voltage range will result in unreliable and unstable behavior.

The consequences of voltage specification violations are explained in the next section. In Section 3.0, recommended techniques for providing accurate regulation and proper decoupling to ensure a robust platform are reviewed.

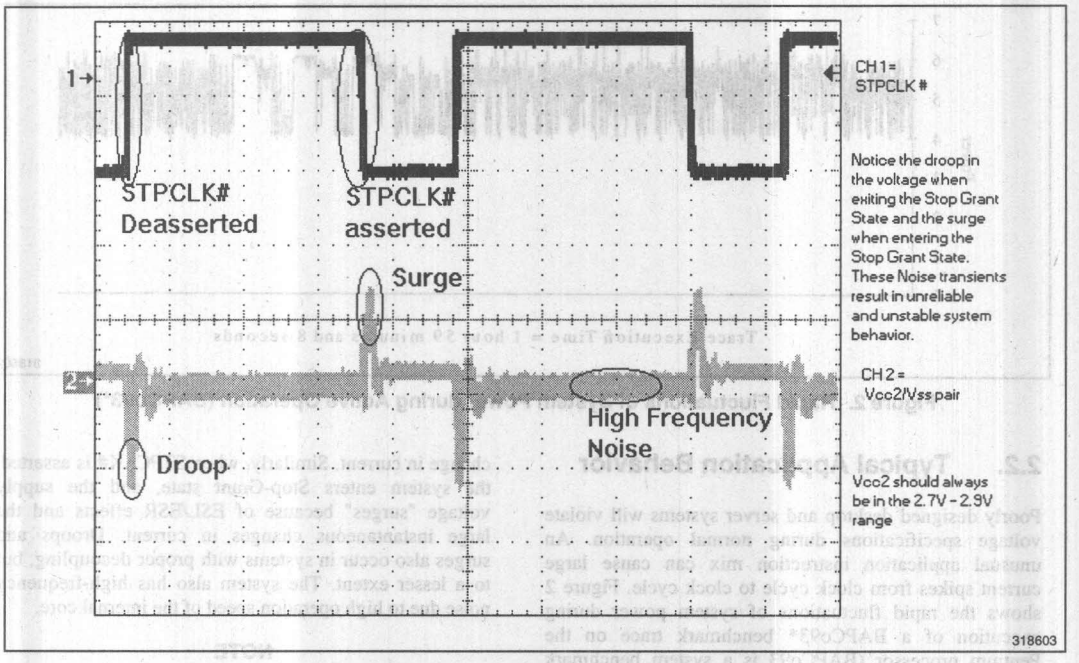


Figure 3. Voltage "Droop" and "Surge" when Toggling STPCLK#

2.3. Voltage Specification Violations

Transient excursions outside of the specified voltage range may result in unstable system behavior. Excessive and sustained surges can cause hot electron related effects and compromise the reliability of the device. Transients may also cause timing violations, which in turn may lead to a failure in the system.

We have seen instances of a system failure because of excessive V_{CC} transient noise.

Extensive die probing experiments show the frequency components of noise that can be damped on a motherboard by adding decoupling capacitors. Data collected through these experiments showed that only noise components less than 20 MHz were reduced on the die by decoupling capacitors added externally. As a result, the recommended oscilloscope measurement bandwidth has been adjusted to 20 MHz (see Section 4.2 for details).

3.0. THE POWER SUPPLY

Unless using a 2.8V power supply, supplying power to the 2.8V core of the Pentium processor with MMX technology requires a 5V to 2.8V voltage regulator or a 3.3V to 2.8V voltage regulator. The power supply pins on the Pentium processor with MMX technology are separated into Vcc_2 and Vcc_3 pins. These pins must be connected appropriately to the processor core voltage island and the processor I/O voltage island on the motherboard. The Pentium processor with MMX technology requires 6.5A at 2.8V (233 MHz) for its core from the supply voltage solution. The 3.3V I/O voltage has to be supplied by the system (either through the 3.3V power supply or through a 3.3V voltage regulator on the motherboard).

Robust local decoupling must be provided to accommodate the transition to and from low-power modes. It is important to select the components for the voltage regulation circuitry to be as accurate as possible. As shown below, selecting accurate components will allow larger voltage transients.

V_{CC} Specs =	Voltage Regulator Accuracy
	+ Support Component Accuracy
	+ Thermal Drift and Aging Effects
	+ Measured Voltage Transient

The Vcc_2 specification allows a total voltage budget of 200 mV. It is important to understand the voltage budget must include any deviation in the voltage regulator, the inaccuracy of its supporting components, and other non-ideal behavior of real components. When designing a platform, these DC factors must be subtracted from the total V_{CC} budget. The remaining allowance should be targeted when measuring the voltage transient (an example is shown in Section 4.5). It is important to select accurate voltage regulators and precise support components to allow maximum voltage transients.

3.1. Selecting an Accurate Power Supply Unit

The power supply unit must provide a minimum setpoint equal to, or higher than, the minimum input voltage required by the regulator. Off-the-shelf 5V power supply units with a 5% accuracy specification can meet the typical 4.75V requirement of most regulators. Figure 4 shows that a 5V power supply unit with an accuracy of 10% may provide a setpoint as low as 4.5V and fail the minimum input requirement of a voltage regulator. If using a less accurate power supply unit, the minimum setpoint must be raised to meet or exceed the minimum input voltage required by the voltage regulator. If a voltage regulator requires an input voltage higher than 4.75V, consider choosing a more accurate power supply unit to raise the minimum setpoint.

Sufficient decoupling must be provided between the power supply unit and the voltage regulator to minimize any noise. The disturbance on the 5V power supply unit may exceed the specification of TTL logic devices if the decoupling capacitance is insufficient.

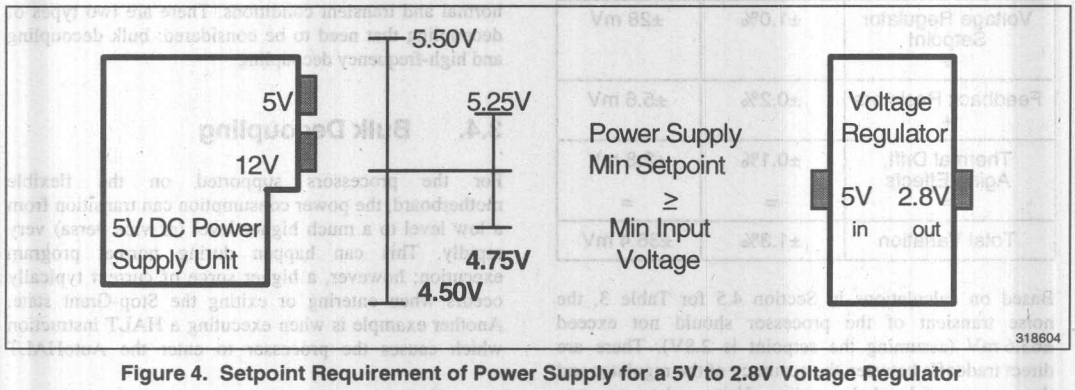


Figure 4. Setpoint Requirement of Power Supply for a 5V to 2.8V Voltage Regulator

3.2. Selecting an Accurate Voltage Regulator

There are two types of voltage regulators: switching and linear. Switching regulators provide power by pulsing the voltages and currents to the load, thus resulting in lower heat dissipation and higher efficiency. Switching regulators are however generally more expensive and require more supporting components than linear regulators. Linear regulators essentially are voltage dividers and provide power by "dividing down" the 5V/3.3V inputs to 2.8V outputs. Linear regulators dissipate more power, but are less expensive and typically require only two additional (feedback) resistors.

Unless the system has strict thermal requirements, linear regulators generally are suited for high-volume designs. Both types of regulators can meet the Vcc_2 voltage range if they have accurate outputs and precise supporting components. Table 2 compares the two types of voltage regulators and shows that linear regulators are cheaper than switching regulators and also require less additional components, but dissipate more power.

An inaccurate regulator leaves little room for transient tolerance. For example, Vcc_2 specifications allow a voltage regulator solution to deviate only ±3.5 percent (2.7V to 2.9V) from the nominal regulator setpoint of 2.8V. Static specifications such as line regulation,

temperature drift, and the initial setpoint must be held to 1% if any transient is to be permitted at all. Table 3 shows sample voltage regulator module accuracy for a Pentium processor with MMX technology-based platform.

Table 2. Comparison of Voltage Regulators

	Linear Regulator		Switching Regulator	
Characteristics (Typical)	**5V to 3.3V**	**5V to 2.8V**	**5V to 3.3V**	**5V to 2.8V**
Maximum Efficiency	67%	56%	95%	90%
Maximum Power Dissipation	33%	44%	5%	10%
Supporting Components	2 to 6 (feedback resistors)	2 to 6 (feedback resistors)	5 to 12 (feedback resistors, MOSFET switches, inductor, diode, caps)	5 to 12 (feedback resistors, MOSFET switches, inductor, diode, caps)
Approximate Total Cost	Moderate	Moderate	Moderately High	Moderately High

Table 3. Recommendations for Linear Voltage Regulator

Parameters	Total Accuracy	Maximum Deviation
Voltage Regulator Setpoint	±1.0%	±28 mV
+		
Feedback Resistors	±0.2%	±5.6 mV
+		
Thermal Drift, Aging Effects	±0.1%	±2.8 mV
=	=	=
Total Variation	±1.3%	±36.4 mV

Based on calculations in Section 4.5 for Table 3, the noise transient of the processor should not exceed ±63.6 mV (assuming the setpoint is 2.8V). There are direct tradeoffs between the accuracy of the regulator and the amount of local decoupling. Using a less accurate regulator requires more accurate dividing resistors and more decoupling. Conversely, using high-ESR, quick-aging capacitors necessitates accurate regulators. The next section recommends the bulk and high-speed decoupling required to ensure a robust Pentium processor with MMX technology-based platform. The recommendations were based on extensive simulations and empirical measurements.

3.3. Decoupling

The small size of the processor core voltage island, its isolation from the motherboard power plane, and support of varied voltage requirements make proper decoupling of the island power plane voltage and ground plane essential. Appropriate decoupling capacitors are required on the voltage island near the processor to ensure that the processor voltage stays within specified limits during normal and transient conditions. There are two types of decoupling that need to be considered: bulk decoupling and high-frequency decoupling.

3.4. Bulk Decoupling

For the processors supported on the flexible motherboard, the power consumption can transition from a low level to a much higher level (or vice versa) very rapidly. This can happen during normal program execution; however, a higher surge of current typically occurs when entering or exiting the Stop-Grant state. Another example is when executing a HALT instruction which causes the processor to enter the AutoHALT

Power Down state, or transition from HALT back to the Normal state. (Note that the AutoHALT Power Down feature is always enabled even when other power management features are not implemented.) All of these examples may cause abrupt changes in the power consumed by the processor. As the voltage supply (regulator) cannot respond to a sudden load change instantaneously, bulk storage capacitors with low ESR (Effective Series Resistance) are required to maintain the regulated supply voltage during the interval that falls between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

3.5. High-Frequency Decoupling

High-frequency decoupling is required to provide a short, low impedance path to high-frequency components such as high current spikes in order to minimize noise. The processor driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

For high-frequency decoupling, low inductance capacitors and interconnects are recommended for best high-speed electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. Surface mount capacitors are preferable, as capacitors with long leads add inductance to the circuit. The capacitors should be of RF grade, with low ESR and low inductance to reduce spikes.

3.6. Decoupling Recommendations

Table 4 shows the processor decoupling recommendations for the flexible motherboard for both the processor core and I/O voltage islands. This is based on simulation and testing of the voltage transients from the processor and the effects of motherboard decoupling.

Spice modeling (modeling worst case current transients including the processor package inductance, capacitance, routing, decoupling, voltage regulator output inductance, etc.) should be used to estimate the amount of decoupling capacitance required for the processor voltage island.

It is advised that before committing to any change from the decoupling capacitor recommendation, the new solution be simulated for the variety of variables in components, temperature and lifetime degradation.

Table 4. Decoupling Recommendations for Processor Core and I/O Voltage Islands

	Quantity	Value	ESR	ESL	Type
Processor Core Voltage Island	4	100 µF	25 mOhms (1)	0.45 nH (3)	Tantalum
	25	1.0 µF	0.6 mOhms (2)	0.084 nH (4)	X7R dielectric, ceramic
Processor I/O Voltage Island (5)	12	0.1 µF			603 Type

NOTES:
1. ESR per capacitor should be less than 100 mOhms.
2. ESR per capacitor should be less than 15 mOhms.
3. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.7 nH.
4. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.1 nH.
5. This does not include decoupling for components other than the processor in the 3.3V I/O voltage island.

For bulk decoupling, tantalum capacitors are recommended over electrolytic capacitors. In general, electrolytic capacitors degrade at a much faster rate, are not as accurate, and are not as stable over temperature as tantalum capacitors.

For high-speed decoupling in the processor core voltage island, low inductance, 1µF capacitors of X7R dielectric are recommended. These capacitors not only decouple the processor core for high-frequency noise but also control the voltage during very fast transients (less than 100 ns.)

3.7. Placement of Decoupling Capacitors

Figure 5 shows an example of how the recommended processor decoupling capacitors shown in Table 4 would be placed on the respective voltage islands on the flexible motherboard. The bulk capacitors should be placed near the processor inside the voltage island to ensure that the supply voltage stays within specified limits during changes in the supply current during operation. The 1µF, X7R capacitors should be evenly distributed inside the processor core voltage island inside and around the processor footprint.

Figure 5 also shows the twelve 0.1 µF capacitors evenly placed around the processor, close to the processor V_{CC3} pins inside the processor I/O voltage island.

In this example, all the capacitors were placed on one side of the board. If components are assembled on both sides of the board, then these capacitors can be distributed between the top and bottom sides. If done this way, vias connecting the capacitor pads to the power and ground layer can be shared between the capacitors on the top and bottom sides. This can help reduce the total overall capacitor inductance. The traces connecting the vias to the capacitor pads should be kept as short as possible. In cases where it is difficult to reduce the length of the circuit board trace, the trace should be made wider so as to reduce the trace inductance.

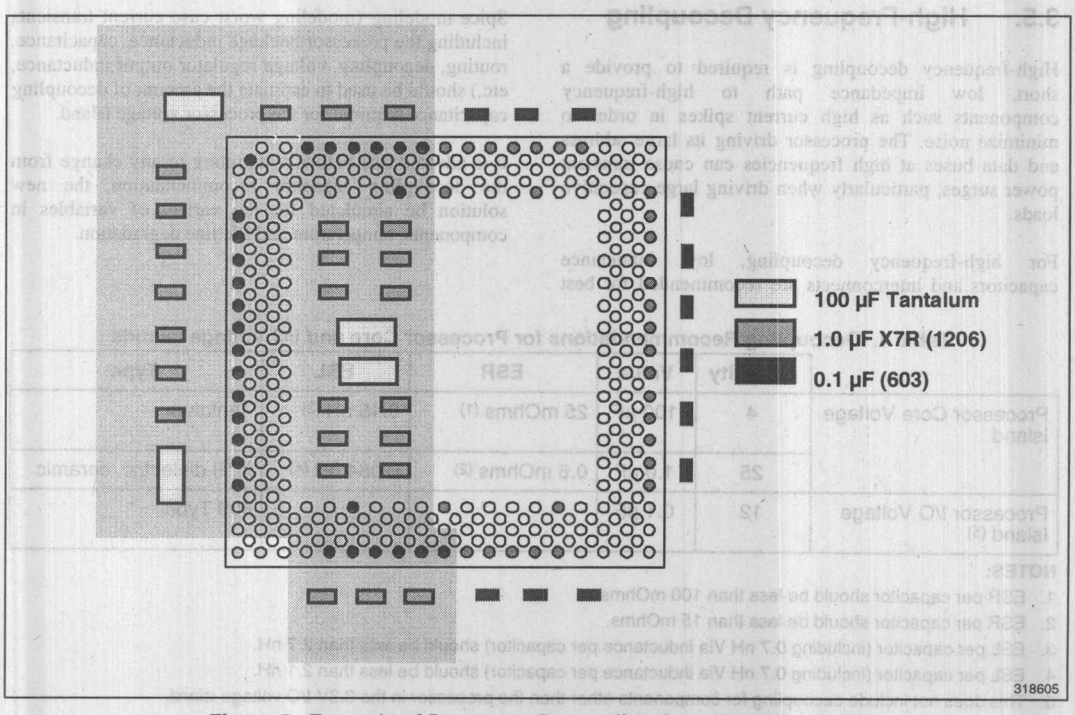


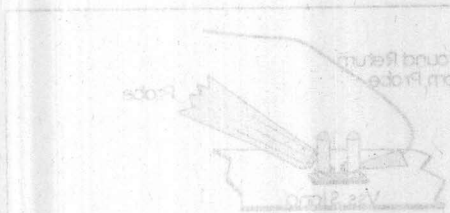
Figure 5. Example of Processor Decoupling Capacitor Placement

3.8. ESR and ESL: Why Less is Better

Effective Series Resistance (ESR) and Effective Series Inductance (ESL) are elements of non-ideal behavior of real components. The ESR and ESL determine how quickly a capacitor can source current to regulate a new load. More importantly, the ESR must be low enough at high frequencies to not offset the desired filtering effects of bulk decoupling capacitors. For a given current transient, the voltage transient is proportional to the ESL and ESR. The use of capacitors with high ESR and ESL hence contributes to higher voltage transients and may cause overshooting or undershooting. Aluminum

electrolytic capacitors degrade at a relatively low frequency. Low ESR tantalum caps can retain ESR specifications up to about 1 MHz to 10 MHz. Low ESR ceramic capacitors can retain ESR specifications up to 100 MHz.

Do not reduce the quantity of capacitors shown in Table 4 if substituting with capacitors with a larger value. When placed in parallel, two 220 µF tantalum capacitors may have higher ESR than four 100 µF capacitors. Placing capacitors in parallel reduces the maximum overall ESR. Therefore, many caps in parallel may be required to ensure a low enough overall ESR.



4.0. TAKING VOLTAGE MEASUREMENTS

4.1. Creating Worst-Case Transient Excursion

The recommendations for regulators and local decoupling can be validated by creating worst-case supply transient conditions and measuring accurately. Worst-case transients may be generated by toggling the STPCLK# and executing the "hi_pwr2.exe" program on a Pentium processor with MMX technology (refer to Appendix A for an explanation of the "hi_pwr2.exe" program). Table 5 contains a summary of the procedure explaining the steps for creating the worst-case transient conditions.

Table 5. Summary for Creating Worst-Case Transient

Step	Action
A	Install 233 MHz Pentium® processor with MMX™ technology.
B	Set up the measurement system as described in Figure 9.
C	Set oscilloscope as shown in Table 6 to obtain the voltage transient
D	Assert and deassert STPCLK#.
E	Measure V_{CC} as shown in Table 7 to obtain the voltage transient. The voltage transient must not overshoot 2.9V, or dip lower than 2.7V for V_{CC2} planes.
F	Assert and deassert STPCLK# while the "hi_pwr2.exe" program is executing. Measure V_{CC} transients as in Step Five.

4.2. Measurement Technique

All transient measurements must be taken at the back of the motherboard at the processor pins. Measuring transients at a different location will result in inaccurate readings. For accurate readings, all probe connections must be clean. Shorten the ground lead of the probe to minimize any extra inductance. Figure 6A proposes a solution by providing a short loop of wire around the ground shield of the probe.

NOTE

Figure 6B is an example of how not to perform measurements; the ground cable of the probe will add significant noise to the transient measurements.

Table 6. Recommended Oscilloscope Settings to Capture Voltage Transients

Bandwidth	20 MHz
Sampling Rate	≥ 100 Million Samples / Second
Vertical Reading	≤ 20 mV / division
Horizontal Reading	≥ 500 ns / division
Display	Infinite Persistence / Envelope Mode

The Pentium processor specifications outline a set of 12 pins for voltage measurements. The Vcc_2/V_{SS} pairs to be measured are A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2, AN13/AM10. The Vcc_3/V_{SS} pins that should be measured according to the specifications are AN21/AM18, AN29/AM26, AC37/Z36, U37/R36, L37/H36, A25/B28. These pins are a subset of all V_{CC}/V_{SS} pairs, and hence should not be singled out when placing decoupling capacitors.

The scope settings shown in Table 6 are recommended for accurate measurements. Extensive die probing experiments were performed on Pentium processors with MMX technology. These experiments concluded that any noise components less than 20 MHz could be reduced on die by decoupling capacitors added externally. Therefore, the measurement bandwidth of the scope should be set at

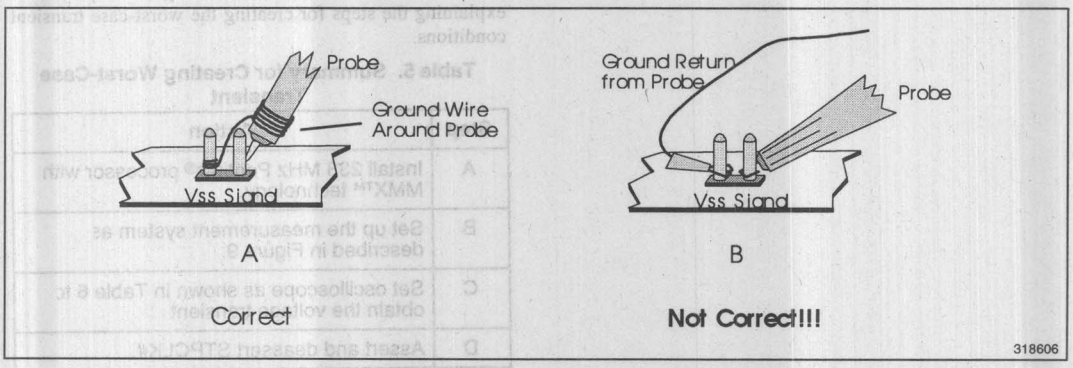


Figure 6. Correct and Incorrect Probe Connections for Measuring Vcc Transients

20 MHz, although a probe with a bandwidth of at least 250 MHz should be used. This high bandwidth probe ensures a total effective bandwidth of 20 MHz. The trigger point should be set in the middle of the range and slowly moved to both the high and low ends of the voltage specification range. A vertical reading of 20 mV/division ensures an accurate reading and display of the transient waveform. The display should be set either on infinite persistence or envelope mode. The advantage of using infinite persistence as compared to envelope mode for this measurement is that random noise points can be ignored in infinite persistence readings. Envelope mode makes the display crispier and the cursor can be positioned more accurately.

4.3. STPCLK# Toggling

It is necessary to assert and deassert the STPCLK# signal while executing the "hi_pwr2.exe" program to create the worst-case transient conditions. Asserting the STPCLK# signal will place the processor into the Stop-Grant state (consuming about 15% of active current). Deasserting the STPCLK# signal will return the processor to the Normal state. To simulate actual system behavior, V_{CC} should be stabilized before asserting or deasserting STPCLK# as shown in Figure 7. Asserting and deasserting STPCLK# too rapidly may generate unrealistic voltage transients. There are no minimum time specifications required to stabilize V_{CC} since the estimated time is highly dependent on the system (length

of current instruction, outstanding write cycles, response time of voltage regulator, and accuracy and quantity of decoupling). In general, STPCLK# should be asserted and deasserted at a rate of 200 Hz to 100 kHz.

STPCLK# toggling is most easily accomplished using a standard function generator. Empirical measurements show that frequency variations from 200 Hz to 100 kHz do not impact V_{CC} measurements. For ease of measurement, toggling the STPCLK# between those frequencies is recommended. For toggling the STPCLK# with a standard frequency generator, a square wave should be generated with 3.3V peak, and a duty cycle in the 25% to 75% range.

If a function generator is not available, alternative means may be used for toggling the STPCLK#. Figure 8 illustrates a simple 555 Timer circuit which can be used to produce a square wave with its duty cycle determined by R2 and R1 and the frequency controlled by the capacitor C.

- Duty Cycle = (R1 + R2) / (R1 + 2R2) * 100
- Frequency = 1.44 / (R1 + 2 * R2) /(R2 * C)

Empirical results have shown that the 555 timer is adequate at toggling the STPCLK#. Experiments done using the 555 timer circuitry have been successful in making accurate voltage transient measurements.

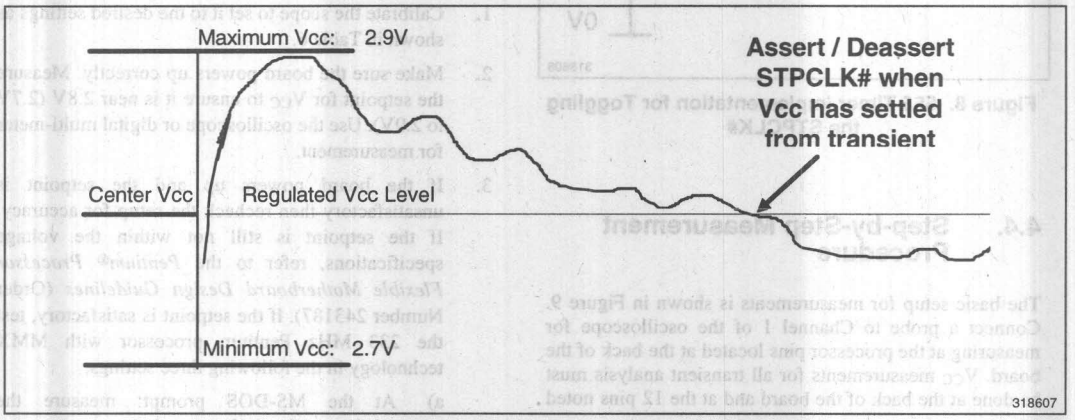


Figure 7. Toggle STPCLK# when V_{CC} Transient has Settled

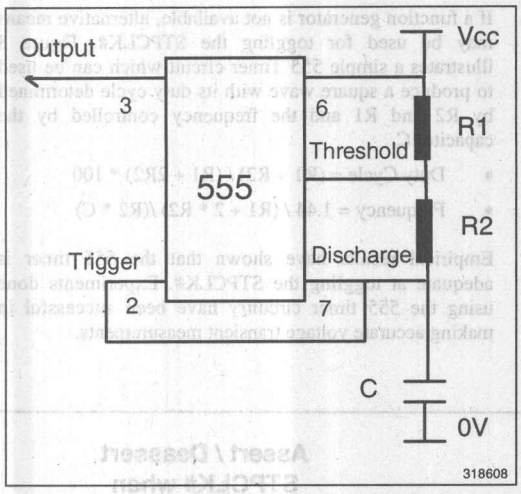


Figure 8. 555 Timer Implementation for Toggling the STPCLK#

4.4. Step-by-Step Measurement Procedure

The basic setup for measurements is shown in Figure 9. Connect a probe to Channel 1 of the oscilloscope for measuring at the processor pins located at the back of the board. V_{CC} measurements for all transient analysis must be done at the back of the board and at the 12 pins noted in Section 4.2. The STPCLK# pin at the back of the board is soldered to a wire for ease of toggling the STPCLK#.

Connect the Signal generator output to the soldered STPCLK# pin on the board using a 50 Ohm coaxial cable. The frequency generator should output a 3.3V peak signal with a 25% to 75% duty cycle. Connect another oscilloscope probe to the soldered STPCLK# pin wire (for trigger). Make sure not to ground this oscilloscope probe to the board ground, because this may cause excess noise. Instead, the probe ground can be wrapped around the probe ground shield such as shown in Figure 6.

Then follow these basic instructions:

1. Calibrate the scope to set it to the desired settings as shown in Table 6.
2. Make sure the board powers up correctly. Measure the setpoint for V_{CC} to ensure it is near 2.8V (2.7V to 2.9V). Use the oscilloscope or digital multi-meter for measurement.
3. If the board powers up and the setpoint is unsatisfactory then recheck the setup for accuracy. If the setpoint is still not within the voltage specifications, refer to the *Pentium® Processor Flexible Motherboard Design Guidelines* (Order Number 243187). If the setpoint is satisfactory, test the 233 MHz Pentium processor with MMX technology in the following three settings:

   a) At the MS-DOS prompt: measure the min/max voltage (for set point).

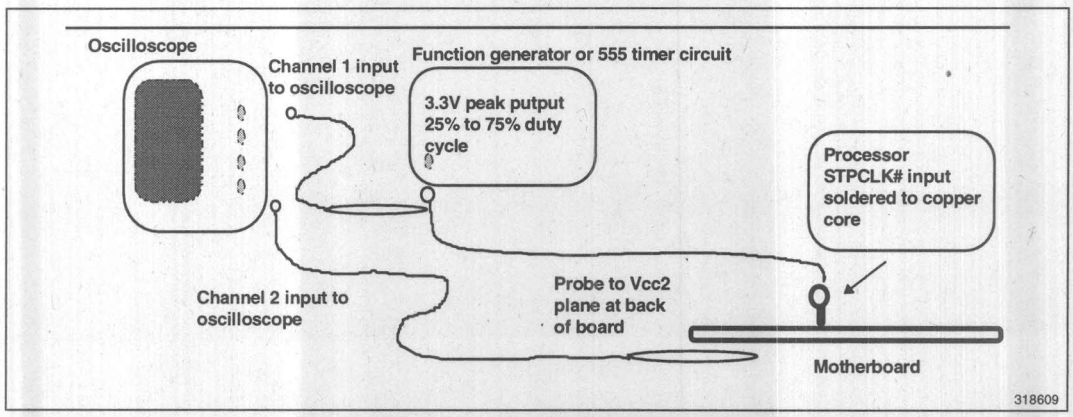


Figure 9. Setup for Measuring V_{CC} Transients at the Back of the Board

b) At the MS-DOS prompt and with STPCLK# toggling: measure the min/max voltage (for 2.8V VCC plane margining).

c) With the stress code (Hi_pwr2.exe) running and the STPCLK# toggling: measure the min/max voltage (for corner cases of V_{CC} spikes and drops).

Measure V_{CC} transients at the six Vcc_2/V_{SS} measurement pairs as discussed in Section 4.2. Tables for documenting these measurements are provided in Appendix C. The next section evaluates each of the measurement settings in significantly more detail. For each of the measurements, document the following for the Data Table in Appendix C.

- Total Δ
- Average V_{CC}
- Absolute Minimum Vcc_c
- Absolute Maximum V_{CC}

4.4.1. PROCEDURE A

At the MS-DOS prompt without the pulse generator connected to the STPCLK# pin, make sure the scope is set to the settings in Table 7 and is triggered at the STPCLK# edge. Measure the difference from the top of the V_{CC} / V_{SS} signal to the bottom as shown in the sample oscilloscope plot in Figure 10. The purpose of this measurement is to get the Min/Max voltage for setpoint. Fill in the table in Appendix C.

Table 7. Measurement Technique Summary

Measurement Bandwidth (1)	20 MHz
Probe Bandwidth	> 250 MHz
Board Location	At the back of the board, at Socket pins
Pin Locations	6 pins for Vcc_2 measurements (listed below) A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2, AN13/AM10

NOTES:

1. Signals should be attenuated by no more than 3 dB at 20 MHz and 6 dB at 40 MHz.

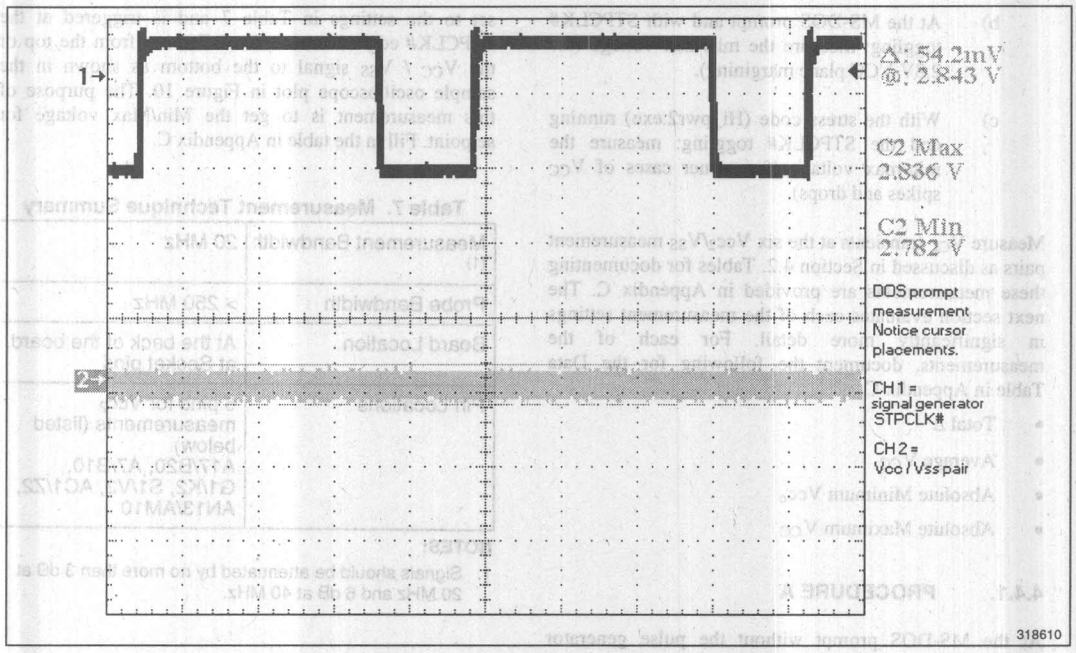


Figure 10. Measuring Min/Max Voltage for Setpoint at MS-DOS* Prompt

4.4.2. PROCEDURE B

At the MS-DOS prompt with the pulse generator "on" and connected to STPCLK# for Vcc_2 plane margining, make sure the scope is set to the setting in Table 7 and is triggered at each edge from the frequency generator. Measure the difference from the top of the surge to the bottom of the droop as shown in the sample oscilloscope plot in Figure 11. Document the following in the data table in Appendix C.

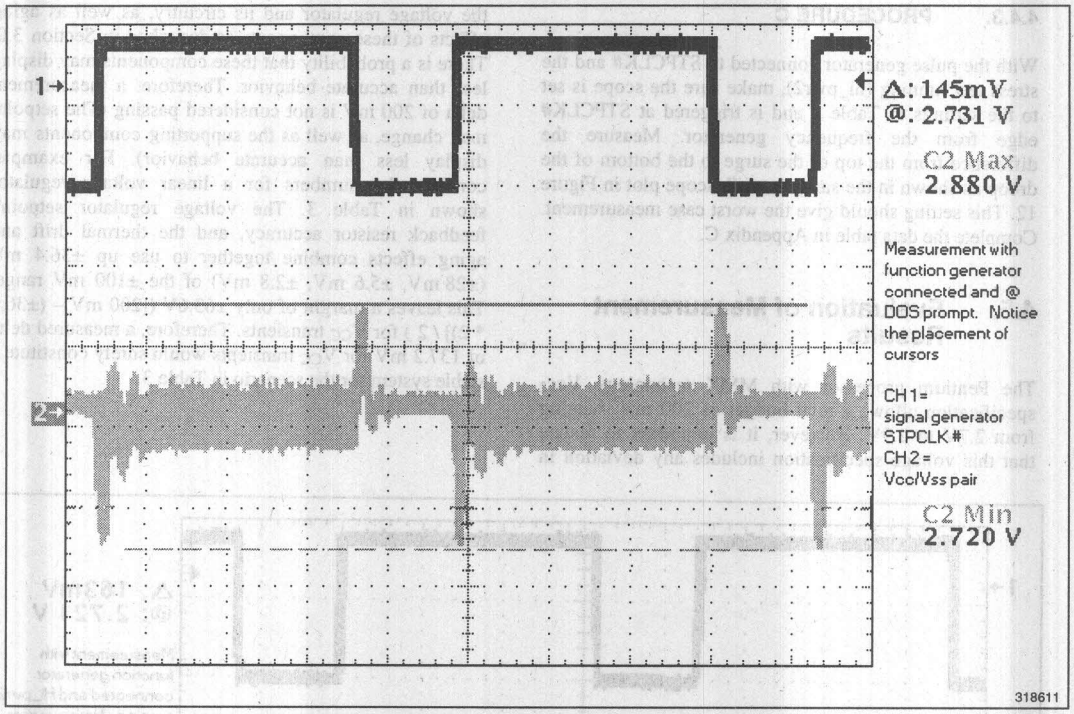


Figure 11. Measuring Min/Max Voltage for Setpoint at MS-DOS* Prompt with STPCLK# Toggling

4.4.3. PROCEDURE C

With the pulse generator connected to STPCLK# and the stress test running (hi_pwr2), make sure the scope is set to the settings in Table 7 and is triggered at STPCLK# edge from the frequency generator. Measure the difference from the top of the surge to the bottom of the droop as shown in the sample oscilloscope plot in Figure 12. This setting should give the worst case measurement. Complete the data table in Appendix C.

4.5. Evaluation of Measurement Results

The Pentium processor with MMX technology Vcc_2 specification allows a total budget of 200 mV, ranging from 2.7V to 2.9V. However, it is important to realize that this voltage specification includes any deviation in the voltage regulator and its circuitry, as well as aging effects of these components as described in Section 3.0. There is a probability that these components may display less than accurate behavior. Therefore, a measurement delta of 200 mV is not considered passing (The setpoint may change, as well as the supporting components may display less than accurate behavior). For example, consider the numbers for a linear voltage regulator shown in Table 3. The voltage regulator setpoint, feedback resistor accuracy, and the thermal drift and aging effects combine together to use up ±36.4 mV (±28 mV, ±5.6 mV, ±2.8 mV) of the ±100 mV range. This leaves a margin of only ±63.6V ([200 mV – (±36.4 * 2)] / 2) for V_{CC} transients. Therefore, a measured delta of 137.2 mV for V_{CC} transients would surely constitute a stable system for the scenario in Table 3.

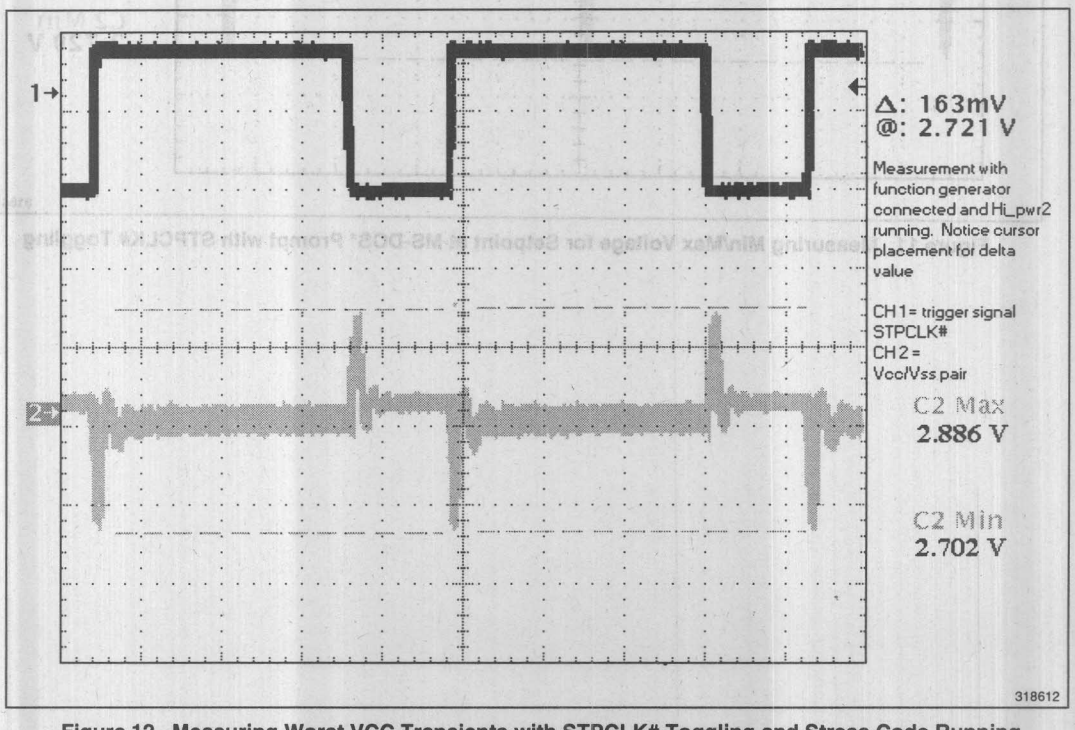


Figure 12. Measuring Worst VCC Transients with STPCLK# Toggling and Stress Code Running

The hi_pwr2.exe code is used for V_{CC} transient analysis and to validate the processors thermal design for the Pentium processor with MMX technology. To get maximum current draw in the system, after the initial setup, the code runs a loop of instructions.

An average Pentium processor with MMX technology in a typical system may dissipate slightly less power than the specification while executing this code. This is because Intel has allowed for process variations between wafers of processors, system variations, and test instrumentation guardbands. Since we can not be sure what power this code will draw in a particular customer system, the actual power drawn by the processor in the particular system should be measured.

The file hi_pwr2.exe contains a short loop of Intel Architecture intensive code. This code uses the most power of any stable, MS-DOS executable program that Intel has tested on Pentium processors with MMX technology.

This code has been optimized for use only with Pentium processors with MMX technology. Any power testing on a Pentium processor without MMX technology should be done with hi_pwr.exe (STR4Y) code.

To use this code for V_{CC} transient analysis:

1. Execute the code.
2. While the code is executing, toggle the STPCLK# signal (i.e. externally since the code itself will not toggle STPCLK#).
3. Measure the noise transients according to the methodology found in this application note.

To use the code to validate a Pentium processor with MMX technology thermal design:

1. Execute the code and measure the power dissipation.
2. If the processor power dissipation falls short of the maximum Thermal Design Power specification, the V_{CC} level may be increased (within its specified range) to attempt to reach the maximum value.
3. If the power dissipation still does not reach the specified maximum value, a thermal linear projection to the guaranteed worst case of the Thermal Design Power should be performed.

Since this program runs in an infinite loop and disables all interrupts, a hard reboot of the system is necessary to exit out of the code.

This program is copyrighted by Intel Corporation. To obtain the code, contact your local Intel Sales office.

Vendor	Part Number	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (max) (A)	Power (max) (W)	Remote Sense	Package	Samp	Prod
Cherry	CS5206	5	2.8	6	17	No	TO-220/D²Pak	Now	Now
		5	3.3/VRE	6	20				
	CS5207A	5	2.8	7	20	Yes	TO-220	Now	Now
		5	3.3/VRE	7	23				
Linear Tech	LT1575	3.3	2.8	10	5	Yes	8-pin SOIC	Now	Now
	(+ ext FET)	5	2.8	10	22				
		5	3.3/VRE	10	27				
	LT1577	5	2.8	10	22	Yes	16-pin SOIC	Now	Now
	(Dual)	5	3.3/VRE	10	27				
	LT1580	5	2.8	7	15.4	Yes	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	LT1584	5	2.8	7	15.4	No	TO-220/TO-263	Now	Now
		5	3.3/VRE	7	11.9				
	LT1585A	5	3.3	5	8.5	No	TO-220/TO-263	Now	Now
Linfinity	LX8384	5	3.3/VRE	5	8.5	No	TO-220/TO-263	Now	Now
	LX8585	5	3.3/VRE	4.6	7.82	No	TO-220/TO-263	Now	Now
	LX8586	5	2.8	6	13.2	No	TO-220/TO-247	Now	Now
		5	3.3/VRE	6	10.2				
National	LM2951	5	2.8	7	15.4	No	SO-8	Now	Now
		5	3.3/VRE	7	11.9				
	LM3411	5	3.3/VRE	7	11.9	No	SO-8/5-pin SOT 23	Now	Now

2.8V/3.3V/VRE Linear Regulator Solutions (Cont'd)

Vendor	Part Number	Electrical				Remote Sense	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (max) (A)	Power (max) (W)			Samp	Prod
Raytheon	RC5102	5	2.8	7	15.4	Yes	8-pin SOIC	Now	Now
	(Dual)	5	3.3/VRE	7	11.9				
	EZ1083/A	5	2.8	7.5	16.5	No	TO-220 or	Now	Now
		5	3.3/VRE	7.5	12.75		TO-247		
	EZ1082	5	2.8	10	22.0	No	TO-220 or	Now	Now
		5	3.3/VRE	10	17		TO-247		
Semtech	EZ1584A	5	2.8	7	15.4	No	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1900	5	2.8	7	15.4	No	8-pin SOIC	Now	Now
	(Dual)	5	3.3/VRE	7	11.9				
	EZ1580	5	2.8	7	15.4	Yes	5-pin TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1585D	5	2.8	6	13.2	No	TO-220	Now	Now
		5	3.3/VRE	6	10.2				
Unisem	US1080	5	2.8	8	17.6	No	TO-220/TO-263	Now	Now
		5	3.3/VRE	8	13.6				

2.8V/3.3V/VRE Switching Regulator Solutions

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (max) (A)	Solution Efficiency (Typical)			Samp	Prod
Raytheon	UCC3881		3.3/VRE				16-pin SOIC or		
Cherry	CS5120	5	2.8	5.7	92%	2	14-pin PDIP	Now	Now
		5	3.3/VRE	5.7	92%		14-pin SOIC		
Harris	HIP5010	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5011	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5010	5	2.8	6	89%	2	7-pin TO-220	Now	Now
		5	3.3/VRE	6	92%		or 7-pin D^2Pak		
	HIP5016	5	2.8	6	89%	2	7-pin TO-220	Now	Now
		5	3.3/VRE	6	92%		or 7-pin D^2Pak		
Linear Tech	LTC1266	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
	LTC1430	5	2.8	15	93%	2	16-pin SOIC or	Now	Now
		5	3.3	15	95%		8-pin SOIC		
	LTC1435	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
Linfinity	LX1660/1	5	2.8	12	85%	2	SO-16	Now	Now
		5	3.3/VRE	12	85%				
Maxim	MAX797	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				
	MAX798	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				
National	LM3578 & LM3411	5	3.3/VRE	10	88%	1	SO-8 or 5-pin SOT23	Now	Now

2.8V/3.3V/VRE Switching Regulator Solutions (Cont'd)

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (max) (A)	Solution Efficiency (Typical)			Samp	Prod
Raytheon	RC5036 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5031	5	2.8	10	87%	1	14-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5035 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
Siliconix	Si9140	5	2.8	6	90%	2	16-pin SOIC	Now	Now
		5	3.3	6	90.5%				
	Si9145	5	2.8	6	82%	1	16-pin SOIC or 16-pin TSSOP	Now	Now
		5	3.3/VRE	6	83%				
Unitrode	UC3886	5	2.8	10	85%	1	16-pin SOIC or 16-pin DIP	Now	Now
		5	3.3/VRE	10	85%				
	UCC3881	5	2.8	10	85%	1	16-pin SOIC or 16-pin DIP	Now	Now
		5	3.3/VRE	10	85%				
	UCC3880	5	2.8	10	85%	1	20-pin SOIC or 20-pin DIP	Now	Now
		5	3.3/VRE	10	85%				
	UC3874	5	2.8	10	90%	2	18-pin SOIC or 18-pin DIP	Now	Now
		5	3.3/VRE	10	90%				
Unisem	US2050	5	2.8	10	85%	1	7-pin TO-220 or TO-263	Now	Now
		5	3.3/VRE	10	85%				

On-Board Regulators

Vendor	North America	Europe	Asia	Japan
Cherry	Dennis Gatano Tel: (401) 886-3305 Fax: (401) 885-5786			
Harris	Dean Henderson Tel: (919) 405-3603 Fax: (919) 405-3651	Robert Lahaye Tel: (33) 1 346 54046 Fax: (33) 1 394-64054	Jason Lin Tel: (886) 2 716 9310 Fax: (886) 2 715 3029	Masaru Agano Tel: (81) 3 3265 7571 Fax: (81) 3 3265 7575
Linear Tech	Bob Scott Tel: (408) 432-1900 Fax: (408) 434-0507	Fred Killinger Tel: (49) 89-9642550 Fax: (49) 89-963147	Dave Quarrels Tel: (65) 753 2692 Fax: (65) 754 4112	
Linfinity	Andrew Stewart Tel: (714) 898-8121 Fax: (714) 893-2570			
Maxim	David Timm Tel: (408) 737-7600 Fax: (408) 737-7194	David Watson Tel: (44) 17 3430 3388 Fax: (44) 17 3430 5511	Steve Huang Tel: (886) 2558 6801 Fax: (886) 2555 6348	Tadi Kodairo Tel: (81) 3 3232 6141 Fax: (81) 3 3232 6149
National	Venkatesh Shan Tel: (408) 721-3753 Fax: (408) 721-8763	Werner Obermaier Tel: (49) 81 4135 1331 Fax: (49) 81 4135 1220	Vincent Lin Tel: (852) 2737 1616 Fax: (852) 2736 9931	Mark Kachmerak Tel: (81) 43 299 2373
Raytheon	David McIntyre Tel: (415) 966-7734 Fax: (415) 966-7742	David Frye Tel: (44) 17 0566 5555 Fax: (44) 17 0566 3355	Mike Wisnia Tel: (81) 3 3406 5998 Fax: (81) 3 3406 5998	
Semtech	Gene Krzwinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Siliconix	Erik Ogren Tel: 408-970-5543 Fax: 408-567-8910	Sean Montgomery Tel: (44) 344 485757 Fax: (44) 344 427371	Serge Jaunay Tel: (852) 2378 9715 Fax: (852) 2375 5733	Tony Grizelj Tel: (81) 3 5562 3321 Fax: (81) 3 5562 3316
Unitrode	John O'Connor Tel: (603) 429-8504 Fax: (603) 429-8963	David Wells Tel: (44) 181 318 1431 Fax: (44) 181 318 2549	Wilkie Wong Tel: 8522-722-1101 Fax: 8522-369-7596	
Unisem	Reza Amirani Tel: (714) 453-1008 Fax: (714) 453-8748			

B2.0. Voltage Regulator Modules

Vendor	North America	Europe	Asia	Japan
Ambit	Leonard Kao Tel: (886) 35-7849575 Fax: (886) 35-782924			
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 1753-67-6800 Fax: (44) 1753-67-6801	Joe Navin Tel: (81) 44-813-8507 Fax: (81) 44-813-8500	
C-MAC	Dave Holmes Tel: (407) 881-2321 Fax: (407) 881-2342			
Corsair	John Beckley Tel: (408) 559-1777 Fax: (408) 559-4294			
Semtech	Gene Krzywinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Raytheon	David McIntyre Tel: (415) 966-7734 Fax: (415) 966-7742	David Frye Tel: 44 17 0566 5555 Fax: 44 17 0566 3355	Mike Wisnia Tel: 81 3 3406 5998 Fax: 81 3 3406 5998	
VXI	Joseph Chang Tel: (503) 652-7300 Fax: (503) 786-5011			

B3.0. Decoupling Capacitors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1 µF, X7S	Dennis Lienemann Tel: (803) 946-0616 Fax: (803) 946-6678	Steve Chan (Singapore) Tel: (65) 258-2833 Fax: (65) 258-8221 K.J. Kim (Korea) Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
	TPSD107K010R0100	100 µF, Tantalum		
Johanson Dielectrics	160R18W105K4	1 µF, X7R	Dave Lopez Tel: (818) 364-9800 Fax: (818) 364-6100 --- NCTR (California only) Tel: (510) 624-8900 Fax: (510) 624-8905	Bill Yu (Taiwan) Nanco Electronics Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Sales Dept (Hong Kong) Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100 µF, Tantalum	Richey-Cypress Elect. Tel: (408) 654-9100 Fax: (408) 566-0160	Warren Marshall Tel: (800) 421-7258 Fax: (714) 713-0129
Murata Electronics	GRM40X7R105J016	1 µF, X7R	Sales Department Tel: (770) 436-1300 Fax: (770) 436-3030	Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483 Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (847) 803-6100 Fax: (847) 803-6296	Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108 Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090

APPENDIX C TEST RESULTS

These tables are provided for you to record your test results.

At MS-DOS* Prompt

Processor Points V_{CC}/V_{SS} Pairs	Average V_{CC} (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B20				
A7/B10				
G1/K2				
S1/V2				
AC1/C2				
AN13/AM10				

In MS-DOS Mode with STPCLK# Toggling

Processor Points V_{CC}/V_{SS} Pairs	Average V_{CC} (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B20				
A7/B10				
G1/K2				
S1/V2				
AC1/C2				
AN13/AM10				

Running Stress Code (hi_pwr2) with STPCLK# Toggling

Processor Points V_{CC}/V_{SS} Pairs	Average V_{CC} (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B20				
A7/B10				
G1/K2				
S1/V2				
AC1/C2				
AN13/AM10				

APPENDIX C TEST RESULTS

These tables are provided for you to record your test results.

At MS-DOS* Prompt

Processor Points Vcc/Vss Pairs	Average Vcc (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B29				
A7/B10				
G1/K2				
S1/V2				
AC1/C2				
AN1/AM19				

In MS-DOS Mode with STPCLK# Toggling

Processor Points Vcc/Vss Pairs	Average Vcc (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B29				
A7/B10				
G1/K2				
S1/V2				
AC1/C2				
AN1/AM19				

Running Stress Code (hl_pwr2) with STPCLK# Toggling

Processor Points Vcc/Vss Pairs	Average Vcc (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B29				
A7/B10				
G1/K2				
S1/V2				
AC1/C2				
AN1/AM19				

intel®

AP-579

APPLICATION NOTE

Pentium® Processor Flexible Motherboard Design Guidelines

June 1997

Order Number: 243187-002

Pentium® Processor Flexible Motherboard Design Guidelines

1.0. INTRODUCTION

This document provides guidelines for designing a Pentium® processor family flexible motherboard. The Pentium processor family flexible motherboard, as shown in Figure 1, is a single motherboard design that can support the various members of the Pentium processor family including Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium processors with MMX™ technology, Pentium OverDrive® processors, and future Pentium OverDrive processors with MMX technology.

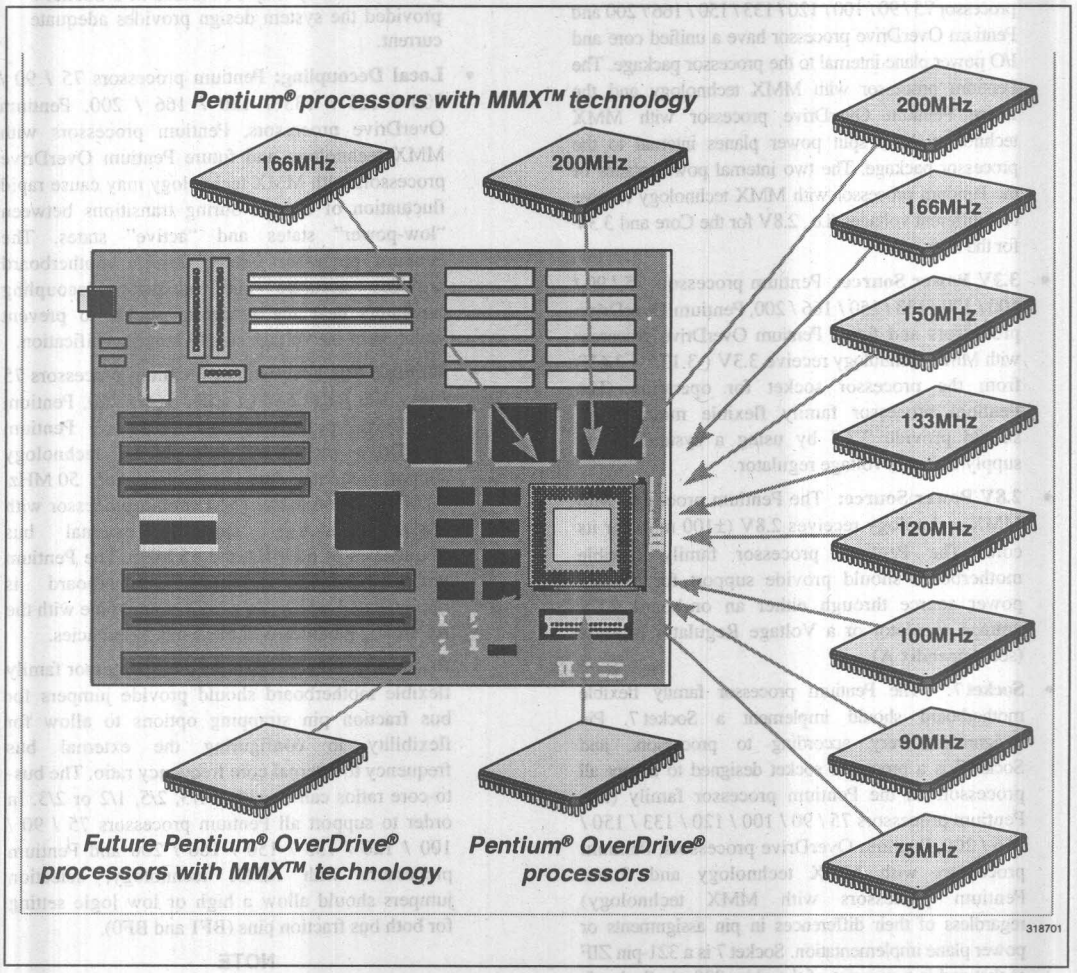


Figure 1. Pentium® Processor Flexible Motherboard

The Pentium processor family flexible motherboard should support the following features:

- **Split Power Islands:** The Pentium processor family flexible motherboard should accommodate split (separate) power islands to accept processors that have split core and I/O voltage planes. The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium OverDrive processor have a unified core and I/O power plane internal to the processor package. The Pentium processor with MMX technology and the future Pentium OverDrive processor with MMX technology have split power planes internal to the processor package. The two internal power planes of the Pentium processor with MMX technology receive two different voltages (i.e., 2.8V for the Core and 3.3V for the I/O).
- **3.3V Power Source:** Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors and future Pentium OverDrive processor with MMX technology receive 3.3V (3.135 – 3.6V) from the processor socket for operation. The Pentium processor family flexible motherboard should provide 3.3V by using a system power supply unit or a voltage regulator.
- **2.8V Power Source:** The Pentium processor with MMX technology receives 2.8V (±100 mV) for its core. The Pentium processor family flexible motherboard should provide support for a 2.8V power source through either an on-board 2.8V voltage regulator or a Voltage Regulator Module (see Appendix A).
- **Socket 7**: The Pentium processor family flexible motherboard should implement a Socket 7. Pin assignments vary according to processors, and Socket 7 is a processor socket designed to accept all processors in the Pentium processor family (i.e., Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium processors with MMX technology) regardless of their differences in pin assignments or power plane implementation. Socket 7 is a 321-pin ZIF socket and is a superset of the older 320-pin Socket 5. Socket 7 provides the option and capability to support both unified-plane processors and split-plane, dual-voltage supply processors and requires that CLK and PICCLK be driven at 3.3V levels. Socket 7 electrical specifications list the maximum current for the future Pentium processors with MMX technology upgradability as 5.0A at 3.3V; however, the Pentium processor with MMX technology has a core current draw of 5.7A at 2.8V.

NOTE

The current draw is processor dependent and any processor belonging to the Pentium processor family may be utilized in a Socket 7 provided the system design provides adequate current.

- **Local Decoupling:** Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology may cause rapid fluctuation of current during transitions between "low-power" states and "active" states. The Pentium processor family flexible motherboard provides accurate and adequate decoupling capacitors near the processor socket to prevent violation of the voltage supply range specification.
- **Multiple Bus Frequencies:** Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, and future Pentium OverDrive processors with MMX technology support external bus frequencies of 50 MHz, 60 MHz and 66 MHz. The Pentium processor with MMX technology supports external bus frequencies of 60 MHz and 66 MHz. The Pentium processor family flexible motherboard is implemented with system logic compatible with the AC timing parameters at these bus frequencies.
- **Bus-to-Core Ratio:** The Pentium processor family flexible motherboard should provide jumpers for bus fraction pin strapping options to allow for flexibility in configuring the external bus frequency to internal core frequency ratio. The bus-to-core ratios can be either 1/3, 2/5, 1/2 or 2/3. In order to support all Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium processors with MMX technology, selection jumpers should allow a high or low logic setting for both bus fraction pins (BF1 and BF0).

NOTE

Not all Pentium OverDrive processors and future Pentium OverDrive processors with MMX technology internally configure the bus fraction, and jumper changes are not required when a Pentium OverDrive processor or a future Pentium OverDrive processor with MMX technology is installed in a Socket 7 system.

- **Thermal and Mechanical Specifications:** The Pentium processor family flexible motherboard should be designed to meet the thermal and mechanical specifications of the Socket 7 Specification, Rev. 3.0.
- **BIOS Support:** Each processor stepping is assigned a unique identification and feature signature. The execution of the CPUID instruction will retrieve these signatures for identification. The Pentium processor family flexible motherboard provides a system BIOS capable of supporting all Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium processors with MMX technology steppings. Through the use of the CPUID instruction, the BIOS can determine whether the processor supports certain features like APIC or MMX technology. (For more details, refer to application note AP-485, *Intel Processor Identification with the CPUID Instruction*. See Appendix E.)
- **3.3V Clock Drivers:** Clock inputs on Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology can accept 3.3V clock drivers but not all are 5V tolerant. The Pentium processor family flexible motherboard provides a 3.3V clock driver (for CLK and PICCLK) to ensure compatibility with all Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology.

1.1. Benefits of a Flexible Motherboard

Producing a flexible motherboard design for the Pentium processor family offers several benefits:

- **Offers various price/performance options:** One flexible design, when populated by different members of the Pentium processor family, can provide a wide range of price/performance options. Flexibility can also be achieved through assembly time options for other components on the motherboard. For example, external caches may use asynchronous SRAM for cost effectiveness or pipelined burst SRAM for higher performance. Synchronous burst DRAM may replace extended data out (EDO) DRAM as main memory to maintain performance in cost-effective platforms with optional external cache memory.
- **Reduces design and validation effort associated with multiple designs:** The board does not have to be revised for every proliferation of the processor thus reducing design and validation efforts. Instead, one board is designed to accept various processors that can be populated at build-time.
- **Reduces inventory and manufacturing costs:** Only one motherboard design has to be manufactured and has to be maintained in inventory. This reduces the overall inventory management and manufacturing costs. For a varying product demand, the board can be populated with the appropriate processor to meet the current market demand.
- **Reduces debug and technical support costs:** Instead of several, only one motherboard has to be debugged. The field engineers and other support personnel need only to be trained on one base motherboard design thus reducing overall technical support efforts.

2.0. PROCESSOR DESIGN CONSIDERATIONS

This chapter describes the differences between the various processors that need to be considered when designing a Pentium processor family flexible motherboard.

2.1. Overview of the Pentium® Processor Family

Table 1 shows the members of the Pentium processor family that are supported on the flexible motherboard and highlights their respective electrical/thermal specifications. The following is a brief description of the Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology processors that are supported on the flexible motherboard. Please refer to Appendix E in order to obtain specifications for each processor.

The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 is a 3.3V processor that operates at 75, 90, 100, 120, 133, 150, 166 and 200 MHz core speeds (50, 60, and 66 MHz external bus speeds). This is a unified plane processor that uses 3.3V [Standard (3.135V – 3.6V) or VRE (3.4V – 3.6V) voltage] for all V_{CC} pins.

The Pentium processor with MMX technology 166/200 is the newest addition to the Pentium processor family. Several architectural enhancements have been made: the internal data and code cache sizes have each been doubled from 8 Kbytes to 16 Kbytes, the branch prediction has been improved, and support for Intel MMX technology has been added. MMX technology is an extension to the Intel Architecture (IA) instruction set which adds 57 new opcodes and a new MMX register set. The Pentium processor with MMX technology operates at core frequencies of 166 and 200 MHz (60 and 66 MHz external bus speeds). The Pentium processor with MMX technology uses 2.8V for its internal core while its I/O operates at 3.3V (to provide full compatibility with existing chipset and SRAM). It is pin, package, and functionally compatible with the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and is operating system transparent. The Pentium processor with MMX technology's CLK and PICCLK buffers are not 5V tolerant and should only use 3.3V clock inputs.

The Pentium OverDrive processor 125/150/166 is the upgrade processor for the Pentium processor 75/90/100-based systems. It plugs into either Socket 5 or Socket 7 based designs. Pentium OverDrive processors are end-user, single-chip processor upgrade products for Pentium processor systems that speed up nearly all software applications and are binary compatible with the Pentium processor.

The future Pentium OverDrive processor with MMX technology 125/150/166/180/200 is the end-user, single chip, processor upgrade for the Pentium processor 75/90/100/120/133-based Socket 5 or Socket 7 designs. The future Pentium OverDrive processor with MMX technology 180/200 can also upgrade Pentium processor 150/166/180/200-based designs to MMX technology, but with a lower overall performance increase. The 200 MHz future Pentium OverDrive processor with MMX technology will only be supported by Socket 7-based designs.

2.2. Pinout Considerations

For the processors that are supported on the flexible motherboard, most of the signals are compatible to each other. The differences are noted below:

- **V_{CC2} , V_{CC3} :** On the Pentium processor with MMX technology, the internal bus logic is isolated from the core logic so that the core can run at a lower voltage (2.8V) in order to obtain faster core frequencies and reduce overall power consumption. The bus logic remains at 3.3V to remain compatible with existing chipsets and cache SRAM. The voltage for the core logic is supplied through the V_{CC2} pins and the voltage for the bus logic is supplied through the V_{CC3} pins. The motherboard design therefore splits the processor power plane into a separate 2.8V core voltage island and a 3.3V I/O voltage island.
- **VCC2DET#**: This is a new signal defined on the Pentium processor with MMX technology to indicate to the system that the processor installed in the processor socket uses an isolated 2.8V core supply on the V_{CC2} pins. This pin is internally connected to ground on the Pentium processor with MMX technology. On Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, and future Pentium OverDrive processors with MMX technology, this pin is defined as INC (Internal No Connect). This signal is pulled high externally on the flexible motherboard or left as a no connect otherwise.

Table 1. Pentium® Processors and Pentium OverDrive® Processors and Their Key Differences

	Pentium® Processor	Pentium Processor with MMX™ Technology	Pentium OverDrive® Processor	Future Pentium OverDrive Processor with MMX Technology
Core Frequency	75, 90, 100, 120, 133 150, 166, 200	166, 200	125, 150, 166	125, 150, 166, 180, 200 (7)
Bus Frequency	50, 60, 66	60, 66	50, 60, 66	50, 60, 66
Frequency Ratio	1/2, 2/3, 2/5,1/3	2/5,1/3	2/5 (4)	2/5, 1/3 (4)
Clock Level	3.3V or 5V	3.3V	3.3V or 5V	3.3V or 5V (7)
Core Supply	3.135V – 3.60V (STD); 3.40V – 3.60V (VRE)	2.7V – 2.9V	3.135 – 3.6V	
I/O Supply	3.135V – 3.60V (STD); 3.40V – 3.60V (VRE)	3.135V – 3.60V	3.135 – 3.6V	
I_{CC2} (1, 5)	Connected to I_{CC3}	5700mA (200 MHz) 4750mA (166 MHz)	Connected to I_{CC3}	Note (6)
I_{CC3} (2, 5)	4600mA (200 MHz) 2650mA (75 MHz)	650mA (200 MHz) 540mA (166 MHz)	4330mA	5000mA (200 MHz) (6) 4330mA(125–180 MHz)
I_{CC5} (3, 5)	Not Applicable	200mA	200mA	
Max. Power (5)	15.5W (200 MHz)	15.7 W (200 MHz)	15.0 W	17.0W (200 MHz) 15.0W (125–180 MHz)
No. of V_{CC2} Pins	None	25	None	28
No. of V_{CC3} Pins	53	28	60	32
No. of V_{CC5} Pins	None	2	2	
External Plane Type	Unified	Split	Unified	Unified or Split
Internal Plane Type	Unified	Split	Unified	Split
Package Type	296-pin PPGA or CPGA	296-pin PPGA or CPGA	320-pin CPGA	320-pin CPGA

NOTES:

1. I_{CC3} refers to V_{CC3} (I/O) supply current.
2. I_{CC2} refers to V_{CC2} (Core) supply current.
3. I_{CC5} refers to 5V supply current. This is used to power the fan/heatsink on the Pentium® OverDrive® processors.
4. Pentium OverDrive processors and future Pentium OverDrive processors with MMX™ technology do not require the bus frequency ratio to be changed when upgraded.
5. The number shown represents worst case or maximum current/power at highest available frequency.
6. When the future Pentium OverDrive processor with MMX technology is installed in split plane designs, 4600mA at 3.3V is drawn through V_{CC2} pins and 400 mA from V_{CC3} pins.
7. The 200 MHz future Pentium OverDrive processor with MMX technology will only be supported in Socket 7 designs.

- **BF1-0**: The bus fraction selection pins determine the bus to core frequency ratio. The BF pins are sampled by the processor at RESET, and will not be sampled by the processor again until another cold-boot (1ms) assertion of RESET. The signal on the BF pins is not an indication of the bus speed, only the ratio of the processor core with respect to the bus. The Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology do not require the BF pins to be changed when upgraded and will operate properly with the bus fraction ratio selected for the processor being replaced. Table 2 summarizes the operation of the BF pins on Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium processors with MMX technology.

- **CLK, PICCLK**: The clock inputs on the Pentium processor with MMX technology are not 5V tolerant. The clock inputs to the processor on the flexible motherboard are driven by an appropriate 3.3V clock driver. Driving the clock at 3.3 volts is also compatible with the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the Pentium OverDrive processor, and the future Pentium OverDrive processor with MMX technology.

2.3. Processor Identification

The CPUID instruction is used to provide information to the BIOS and other software about the vendor, family, model, and stepping of the processor. An input value of 1 loaded into the EAX register prior to executing the CPUID instruction will return the identification signature in the EAX register. Figure 2 shows the EAX bit assignment for the CPUID instruction. (For more details, refer to application note AP-485, *Intel Processor Identification with the CPUID Instruction*. See Appendix E.)

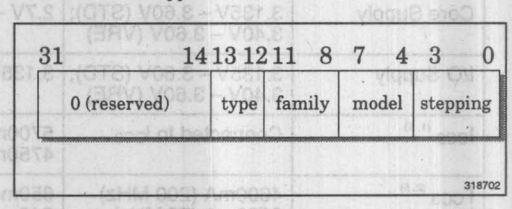


Figure 2. EAX Bit Assignments for CPUID

Table 3 provides the CPUID information for the different processors that are supported on the flexible motherboard.

Table 2. BF1-0 Core/Bus Ratio Selection Pins (1)

BF1 Value (5)	BF0 Value (5)	Pentium® Processor 75 / 90 / 100 / 120 / 133 / 150 / 166 200 Frequency Ratio	Pentium Processor with MMX™ Technology Frequency Ratio
0	0	2/5 (2)	2/5 (2)
0	1	1/3	1/3
1	0	1/2 (3)	1/2 (3) (Default)
1	1	2/3 (4) (Default)	Reserved

NOTES:

1. The Pentium processors with a maximum rated core frequency of less than 75 MHz have only one bus fraction ratio defined – (1:1).
2. The 2/5 ratio is defined on the Pentium® processor with MMX™ technology and Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200.
3. Defaults to 1/2 ratio if BF1 and BF0 are left unconnected on the Pentium processor with MMX technology. On the Pentium processor with MMX technology, the BF1 pin has an internal pull-up resistor, and the BF0 pin has an internal pull-down resistor.
4. Defaults to 2/3 ratio if BF1 and BF0 are left unconnected on Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200. On the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the BF1 and BF0 pins have internal pull-up resistors.
5. The value of external pull-down resistors used on the BF0/BF1 pins should be 500 ohms or less. The value of external pull-up resistors used on the BF0/BF1 pins should be 2.2 Kohms or less.

Table 3. CPUID Information

Type Bits(13:12)	Family Bits(11:8)	Model Bits(7:4)	Stepping Bits(3:0)	Description
00	0101	0010	xxxx	Pentium® processors (75, 90, 100, 120, 133 150, 166, 200)
00	0101	0100	xxxx	Pentium processor with MMX™ technology (166, 200)
00 (1)	0101	0010	xxxx	Pentium OverDrive® processor for Pentium processor (75, 90, 100)
01	0101	0100	xxxx	Future Pentium OverDrive processor with MMX technology for Pentium processor (75 90, 100, 120, 133, 150, 166, 200

NOTES:

1. The definition of the type field for the OverDrive® processor is 01. An errata on the Pentium® OverDrive processor will always return 00 as the type.

3.0. FLEXIBLE MOTHERBOARD IMPLEMENTATION

This chapter describes the implementation of a split plane flexible motherboard using Socket 7.

3.1. Voltage Supply Implementation Overview

In order to support the various members of the Pentium processor family with different voltage requirements, the flexible motherboard should include provisions for both 2.8V and 3.3V supply voltages for the processor.

The power supply pins on the Pentium processor with MMX technology are split into separate V_{CC2} and V_{CC3} pins. Socket 7 definition splits the 60 V_{CC} pins on Socket 5 into 28 V_{CC2} pins and 32 V_{CC3} pins. These pins are connected appropriately to the processor core voltage island and processor I/O voltage island. The Pentium processor with MMX technology uses 5.7A at 2.8V (200 MHz) for its core from the supply voltage solution. The 3.3V I/O voltage for the Pentium processor with MMX technology is supplied by the system (either through the 3.3V power supply or through a 3.3V voltage regulator on the motherboard).

The voltage provided to the core of the future Pentium OverDrive processor with MMX technology is supplied by a voltage regulator, internal to the OverDrive processor package, powered by 3.3V on the V_{CC2} pins. The I/O is powered directly from the 3.3V V_{CC3} pins. The voltage supply solution on the flexible motherboard supplies a minimum of 0.4A at 3.3V on V_{CC3} and 4.6A at 3.3V on V_{CC2} to support the 200 MHz future Pentium OverDrive processor with MMX technology. It is not required that both power planes be supplied by the same source. In addition, the Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology also use a +5V supply to power the fan/heatsink.

In a typical single processor system, the 3.3V power supply uses approximately 7A to power all the 3.3V components (i.e. processor, cache and chipset). In the 200 MHz Pentium processor with MMX technology, the 2.8V regulator draws up to approximately 5.7A at 2.8V for the processor core while the 3.3V power supply should require approximately 2A at 3.3V for the cache and chipset. Additional 3.3V devices such as 3.3V DRAM may require additional power. Actual power requirements should be calculated for the specific design.

3.2. The Distinct Power Planes

A typical desktop flexible motherboard contains a maximum of four different power planes. Any Pentium processor will directly plug into two of these planes (V_{CC2}, V_{CC3}) and may be indirectly connected to the 3.3V power supply ($3V_{POWER\ SUPPLY}$) through the $V_{I/O}$ (V_{CC3}) power plane. See Figure 3. For the most economically flexible motherboard design, it is recommended that the $V_{I/O}$ plane simply be connected to the motherboard's $3V_{POWER\ SUPPLY}$ by jumpers or 0Ω resistors. Therefore, excluding the main 5V power plane, the Pentium processor family flexible motherboard may have a minimum of two distinct

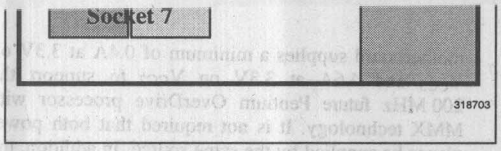


Figure 3. The Typical Power Planes in a Desktop Pentium® Processor Family Flexible Motherboard

The power plane distinctions are described below.

V_{CORE} — This power plane is connected to the V_{CC2} power pins on the Pentium processor family's Socket 7 connector (see Figure 3). When a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 is installed in the system, this plane will typically be connected to the $V_{I/O}$ plane through 0Ω resistors, jumpers, or the internal power plane of the Pentium processor. However, in the case of the Pentium processor with MMX technology, the V_{CC2} and V_{CC3} planes remain completely electrically separate. Also, the future Pentium OverDrive processor with MMX technology will not connect V_{CC2} and V_{CC3} through its internal power planes. Depending upon which processor is being supported, the V_{CC2} plane may require either a discrete 2.8V voltage regulator, or a configurable 2.8V/3.3V/VRE voltage regulator. The VCC2DET# signal can be used to select between 2.8V and 3.3V/VRE on the configurable V_{CORE} voltage regulator. The V_{CORE} power plane uses a voltage regulator that can supply at least 5.0A at 3.3V for a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and at least 5.7A at 2.8V for a Pentium processor with MMX technology.

Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 (a unified-plane processor) has its V_{CORE} + $V_{I/O}$ plane supplied with VRE voltage, the V_{CORE} + $V_{I/O}$ plane may need to be isolated from the 3.3V components and $3V_{POWER\ SUPPLY}$. See Figure 5. An auto-configurable flexible motherboard should make provisions for connecting/disconnecting the $V_{I/O}$ and $3V_{POWER\ SUPPLY}$ in order to accommodate processors running on VRE voltage or 3.3V voltage (see next section).

$3V_{POWER\ SUPPLY}$ — This power plane is the motherboard's 3.3V power plane (not to be confused with the motherboard's 5V power plane). This typically powers the 3.3V cache, chipset and DRAM components on the Pentium processor family flexible motherboard. In cost effective motherboards, the $3V_{POWER\ SUPPLY}$ is typically connected to the $V_{I/O}$ power plane; however, if the processor is a unified-plane processor, this plane will then be connected to both the $V_{I/O}$ and V_{CORE} power planes as well (see next section). In a split plane, dual voltage processor, like the Pentium processor with MMX technology, the $3V_{POWER\ SUPPLY}$ plane will be separated from the V_{CORE} power plane.

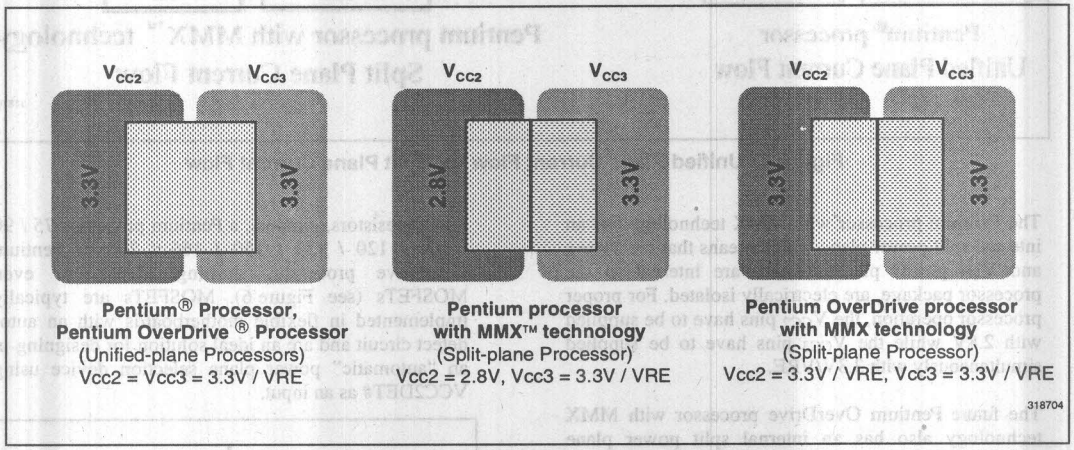
NOTE

The future Pentium OverDrive aprocessor with MMX technology will not internally connect V_{CORE} to $V_{I/O}$.

$5V_{POWER\ SUPPLY}$— This is the motherboard's 5V power plane. This plane will power the 5V components such as DRAM, keyboard controller, mouse, FLASH BIOS memory, TTL Logic, and some I/O bus components and connectors.

may be operated by applying 3.3V/VRE to both the V_{CC2} power pins and V_{CC3} power pins simultaneously, or by applying 3.3V/VRE power to either the V_{CC2} pins or the V_{CC3} pins separately. Since the internal power plane is unified, the power from the V_{CC2} pins will flow to the V_{CC3} pins and vice-versa.

with a future Pentium OverDrive processor with MMX technology, because of their internal split power plane design.



Pentium® Processor, Pentium OverDrive ® Processor
(Unified-plane Processors)
Vcc2 = Vcc3 = 3.3V / VRE

Pentium processor with MMX™ technology
(Split-plane Processor)
Vcc2 = 2.8V, Vcc3 = 3.3V / VRE

Pentium OverDrive processor with MMX technology
(Split-plane Processor)
Vcc2 = 3.3V / VRE, Vcc3 = 3.3V / VRE

Figure 4. Pentium® Processor Family Power Plane Characteristics

Table 4. The Three Types of Pentium® Processor Power Planes

Category	Processor
Unified Plane processors with Single Voltage Input (V_{CC} = 3.3V/VRE)	Pentium® processors 75 / 90 / 100 / 120 / 133 / 150 / 166 200 MHz, Pentium OverDrive® processors 125/150/166 MHz
Split-Plane processors with Dual Voltage Input (V_{CC2} = 2.8V & V_{CC3} = 3.3V/VRE)	Pentium processors with MMX™ technology (166, 200 MHz)
Split-Plane processors with Single Voltage Input (V_{CC} =3.3V/VRE)	Future Pentium OverDrive processors with MMX technology 125/150/166/180/200 MHz

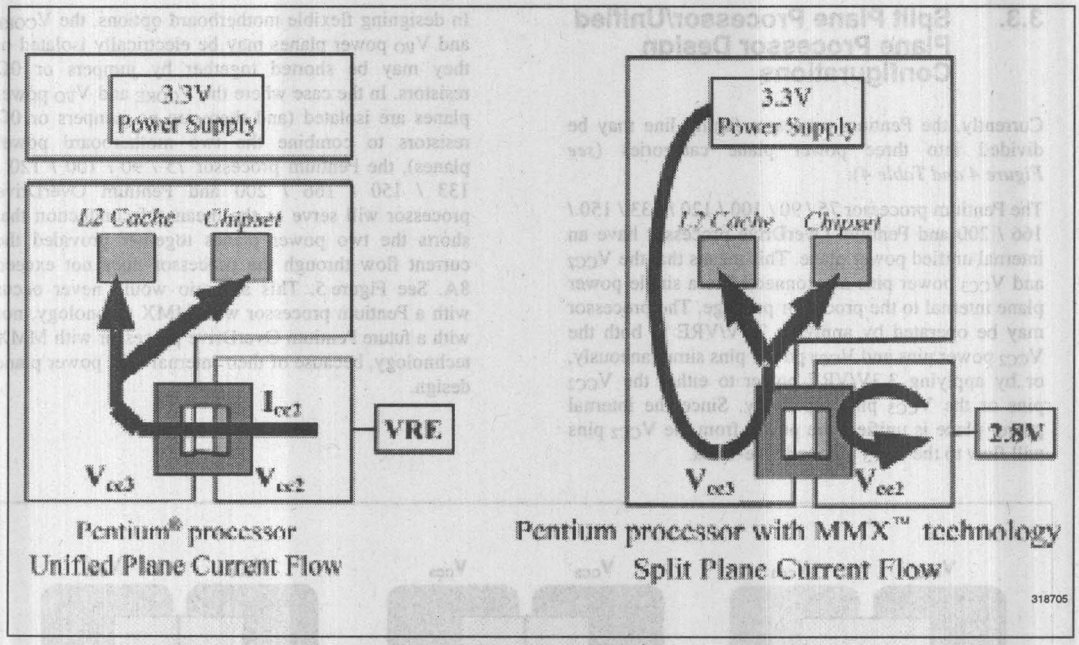


Figure 5. Unified Plane Current Flow vs. Split Plane Current Flow

The Pentium processor with MMX technology has an internal split power plane which means that the V_{CORE} and $V_{I/O}$ power planes, which are internal to the processor package, are electrically isolated. For proper processor operation, the V_{CC2} pins have to be supplied with 2.8V while the V_{CC3} pins have to be supplied simultaneously with 3.3V/VRE.

The future Pentium OverDrive processor with MMX technology also has an internal split power plane which means that the V_{CORE} and $V_{I/O}$ power planes, internal to the processor package, are also electrically isolated. In order to properly operate this OverDrive processor, the V_{CC2} pins and V_{CC3} pins must always be powered simultaneously with 3.3V/VRE.

NOTE

The two power planes do not have to be powered by the same voltage source.

3.4. Power Plane Connections and Voltage Regulator Shutdown

As a flexible motherboard option, the two V_{CORE} and $V_{I/O}$ power planes have the option of being connected via 0Ω resistors, jumpers, a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 or Pentium OverDrive processor, shorting blocks, or even MOSFETs (see Figure 6). MOSFETs are typically implemented in flexible motherboards with an auto-detect circuit and are an ideal solution for designing in an "automatic" power plane selection device using VCC2DET# as an input.

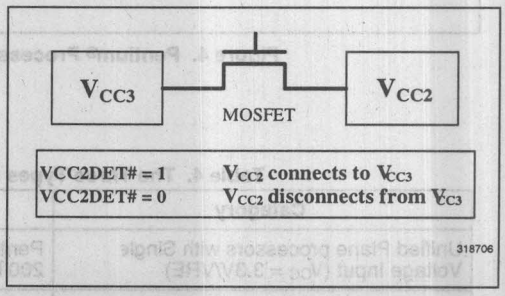


Figure 6. Use of MOSFETs to Connect/Disconnect Power Planes

If a unified-plane processor is plugged into a flexible motherboard with two voltage regulators, one of the voltage regulators may "shut down". The voltage

regulator attached to the V_{CC2} power pins will always have a much higher current rating than the voltage regulator attached to the V_{CC3} power pins because the V_{CC2} plane directly powers the processor core. When a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 or Pentium OverDrive processor is plugged into the system, the current will flow from the V_{CC2} plane to the V_{CC3} power plane and shut down the weaker voltage regulator (the weaker voltage regulator will detect the increased current and shut itself down). This is acceptable provided the 8A maximum specification for current flow across a unified plane processor is maintained (see Figure 7). However, when a split plane processor, like the Pentium processor with MMX technology or the future Pentium OverDrive processor with MMX technology, is inserted in the socket, the two regulators are electrically isolated and each continues to function. Also, the designer may design the motherboard such that the two voltage regulators current share; however, this is an implementation specific option and up to the designer's discretion.

3.5. Voltage Supply Implementation Options

There are several voltage supply implementation options to support all the different Pentium family processors on the flexible motherboard. The following options will be discussed in this section:

1. Using a 2.8V/3.3V auto-configurable voltage regulator.
2. Using an on-board 2.8V regulator as a build option.
3. Using the Voltage Regulator Module (VRM). Refer to Appendix A.

3.5.1. 2.8V/3.3V AUTO-CONFIGURABLE REGULATOR

An auto-configurable regulator circuit is an option for supply voltage implementation on the flexible motherboard. This approach allows all Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology, and future Pentium OverDrive processors with MMX technology to be easily supported without the need for any jumper/resistor configuration. Figure 8 shows two regulators that work together to form an auto-configurable voltage solution.

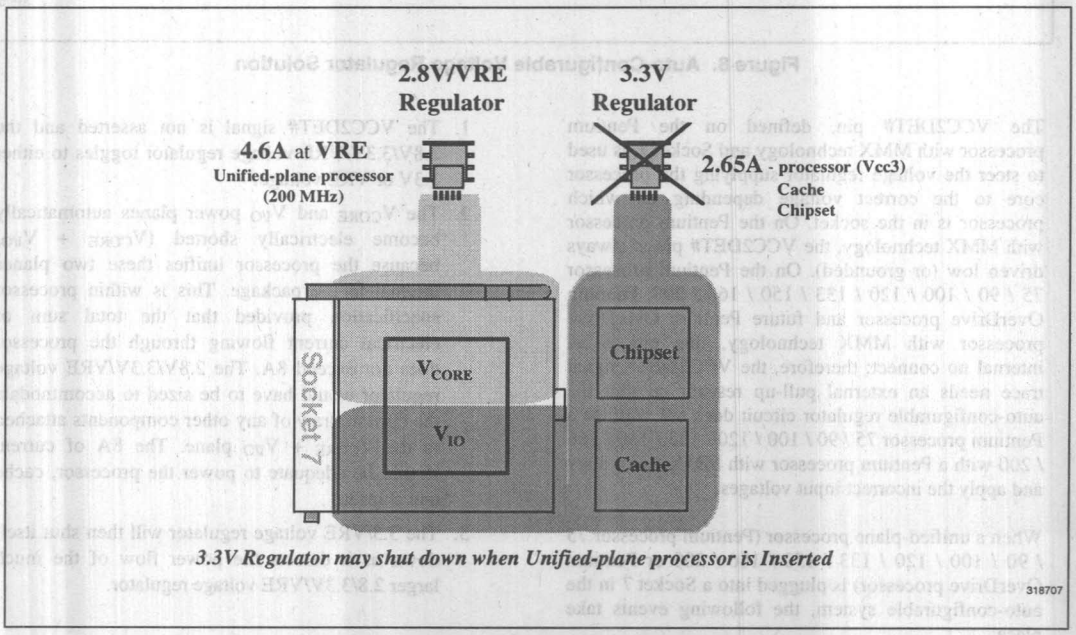


Figure 7. Regulator Shutdown Phenomenon

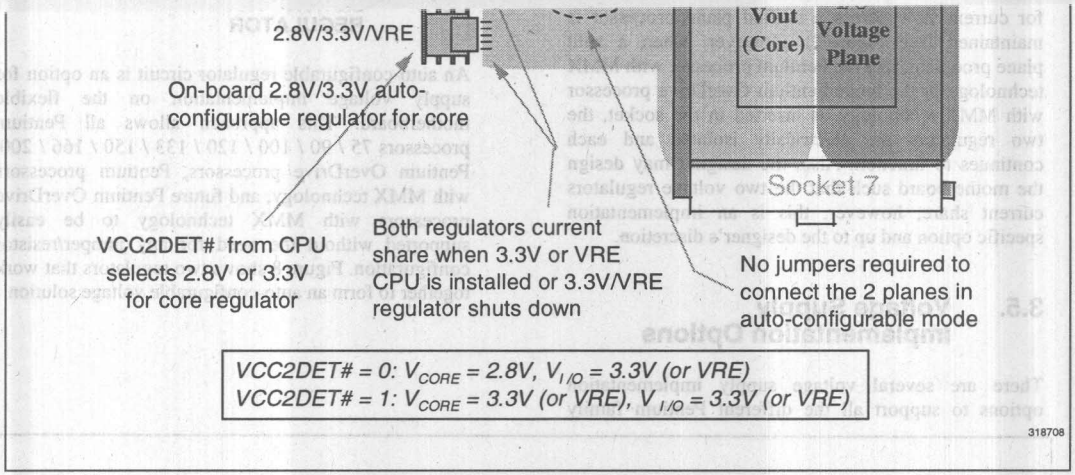


Figure 8. Auto-Configurable Voltage Regulator Solution

The VCC2DET# pin, defined on the Pentium processor with MMX technology and Socket 7, is used to steer the voltage regulator supplying the processor core to the correct voltage depending on which processor is in the socket. On the Pentium processor with MMX technology, the VCC2DET# pin is always driven low (or grounded). On the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology, this pin is an internal no connect; therefore, the VCC2DET# signal trace needs an external pull-up resistor so that the auto-configurable regulator circuit does not confuse a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 with a Pentium processor with MMX technology and apply the incorrect input voltages.

When a unified-plane processor (Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 or Pentium OverDrive processor) is plugged into a Socket 7 in the auto-configurable system, the following events take place:

1. The VCC2DET# signal is not asserted and the 2.8V/3.3V/VRE voltage regulator toggles to either 3.3V or VRE voltage.
2. The V_{CORE} and $V_{I/O}$ power planes automatically become electrically shorted (V_{CORE} + $V_{I/O}$) because the processor unifies these two planes internal to the package. This is within processor specification provided that the total sum of electrical current flowing through the processor does not exceed 8A. The 2.8V/3.3V/VRE voltage regulator would have to be sized to accommodate the current draw of any other components attached to the V_{CORE} + $V_{I/O}$ plane. The 8A of current should be adequate to power the processor, cache and chipset.
3. The 3.3/VRE voltage regulator will then shut itself down as it detects the power flow of the much larger 2.8/3.3V/VRE voltage regulator.

When a split-plane, dual voltage processor (Pentium processor with MMX technology) is plugged into a Socket 7 in the auto-configurable system, the following events take place:

1. The VCC2DET# signal is asserted and the 2.8V/3.3V/VRE voltage regulator toggles to 2.8V voltage.
2. The V_{CORE} and $V_{I/O}$ power planes remain electrically isolated because the processor splits these two planes internal to the package.
3. The 3.3V/VRE voltage regulator continues to function and supply the $V_{I/O}$ power plane which may include both the processor's V_{CC3} pins and any cache and chipset on the $V_{I/O}$ plane.

When a split-plane, single voltage processor (future Pentium OverDrive processor with MMX technology) is plugged into a Socket 7 in the auto-configurable system, the following events take place:

1. The VCC2DET# signal is not asserted and the 2.8V/3.3V/VRE voltage regulator toggles to either 3.3V or VRE voltage.
2. The V_{CORE} and $V_{I/O}$ power planes remain electrically isolated because the processor splits these two planes internal to the package.
3. The 3.3V/VRE voltage regulator continues to function and supply the $V_{I/O}$ power plane which may include both the processor's V_{CC3} pins and any cache and chipset on the $V_{I/O}$ plane.

An auto-configurable voltage regulator solution may also be designed-in as a manufacturing stuffing option. In this case, both regulators are designed-in but only one regulator is populated on the board. This regulator needs to provide enough current capability to drive both the core and the I/O voltage planes. With only one regulator in the system, 4–6 0Ω resistors or external jumpers are also needed to connect both the core and I/O planes at manufacturing time (for split-plane, single voltage processors). When the second regulator and associated circuitry is populated on the board, these jumpers are removed or left out to provide the full auto-configurable capability.

3.5.2. 2.8V REGULATOR AS A BUILD OPTION

In this implementation option, the flexible motherboard is configured at manufacturing build or assembly time for either the Pentium processor, 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 (unified-plane, single-voltage processor) or the Pentium processor with MMX technology (split-plane, dual voltage processor).

NOTE

All Pentium OverDrive processors and future Pentium OverDrive processors with MMX technology are intended as a consumer upgrade product for unified-plane, single-voltage processors.

As shown in Figure 9, a 2.8V voltage regulator is designed-in and populated when the board is configured to support the Pentium processor with MMX technology.

When the 2.8V voltage regulator is not installed on the board, a Motherboard build option of 4–6 jumpers or 0Ω resistors (i.e. , #1206, 1/8 watt, surface mount resistors) is recommended to connect the core and I/O voltage planes (in split-plane, single voltage processors and, optionally, unified-plane, single voltage processors as well) for an approximate current carrying capability of approximately 5–8 amps (dependent upon the quantity of components). However, a unified-plane processor will conduct current between the core and I/O voltage planes without a need for jumpers/resistors. Conversely, when the 2.8V voltage regulator is assembled on the motherboard, the jumper/resistor build option should not be added in order to isolate the two voltage planes.

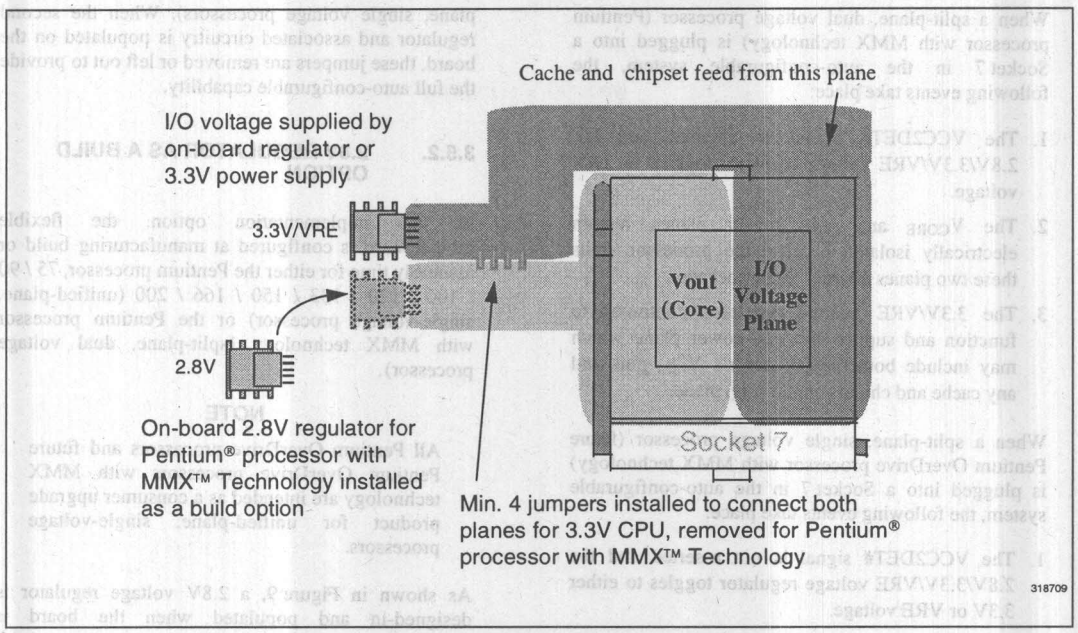


Figure 9. 2.8V Voltage Regulator Designed as a Build Option

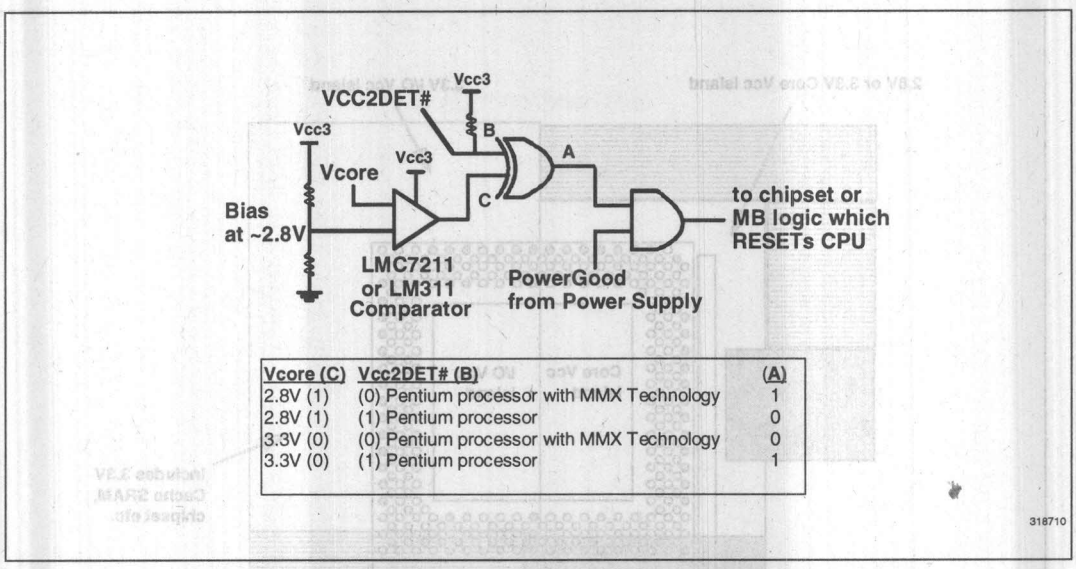
3.5.3. SAFEGUARDING THE PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY ON THE FLEXIBLE MOTHERBOARD

The Pentium processor with MMX technology core operates at 2.8V. A Socket 7 based flexible motherboard design that is not configured for 2.8V should implement some type of safeguarding mechanism to protect the Pentium processor with MMX technology from getting the wrong voltage. Operating the Pentium processor with MMX technology's core at 3.3V could potentially cause damage to the processor.

The VCC2DET# pin defined on the Pentium processor with MMX technology and Socket 7 may be used to implement some type of protection circuitry that can be used to either disable the voltage source or prevent the processor from booting if the wrong voltage is detected.

The example circuit shown in Figure 10 may be used to prevent RESET from being generated to the processor if the wrong core voltage is detected. This circuit uses a comparator to compare the core voltage to a reference voltage (~2.8V). If VCC2DET# is grounded (for the Pentium processor with MMX technology) and the core voltage is greater than the reference voltage, the output of the exclusive OR gate will be low which would signal the chipset to not assert RESET. Similarly if VCC2DET# is high (for 3.3V processor), and the core voltage is lower than the reference voltage, the chipset should not be allowed to assert RESET.

Another example of safeguard implementation is shown in Figure 11. The approach here is to reduce the output voltage of the core regulator (3.3V or VRE) if a low level on VCC2DET# pin is detected. This would be a simpler and cheaper implementation for designs that are using an adjustable voltage regulator, where the output voltage level can be adjusted using a resistor divider. As shown in Figure 9, the value of the resistor divider is altered appropriately (bottom resistor is shorted to ground) when VCC2DET# indicates a zero. This effectively can reduce the output voltage to an appropriate level for the Pentium processor with MMX technology.



Vcore (C)	Vcc2DET# (B)	(A)
2.8V (1)	(0) Pentium processor with MMX Technology	1
2.8V (1)	(1) Pentium processor	0
3.3V (0)	(0) Pentium processor with MMX Technology	0
3.3V (0)	(1) Pentium processor	1

Figure 10. External Safeguard Circuit to Prevent Processor from Booting

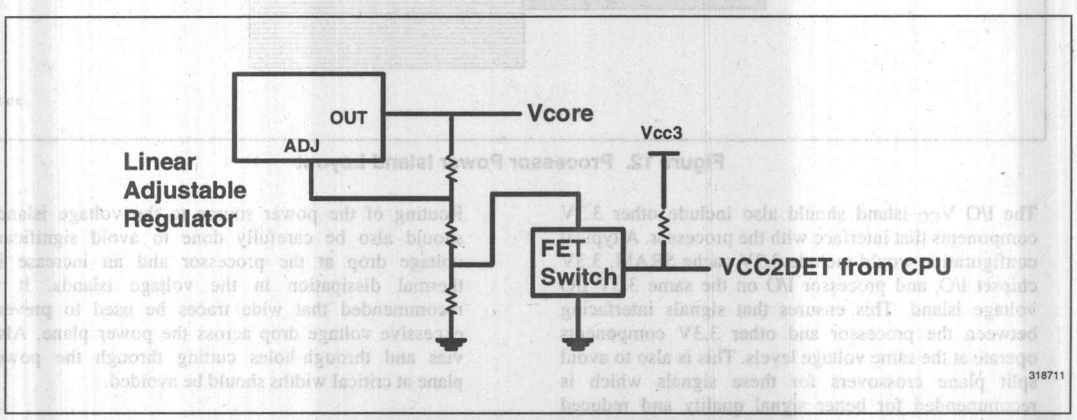


Figure 11. External Safeguard by Reducing the Output Voltage

3.6. Split Power Plane Layout

Implementing a power island on an existing power layer instead of assigning a separate power layer for core V_{CC} can be a more economical solution. The separate voltage island can be isolated from the other section of the power plane using an air gap. The size of the air gap is determined by analysis of the noise effects and board manufacturing capabilities (typically 10–20 mils).

Figure 12 shows a typical layout of the separate voltage islands in the processor area. It shows the core V_{CC} pins (V_{CC2}) clustered on one side of the processor to allow easy layout of the core voltage island. The remaining V_{CC} pins for the periphery (V_{CC3}) are located on the other side and are part of the I/O voltage island (refer to Socket 7 pinout, see Appendix B).

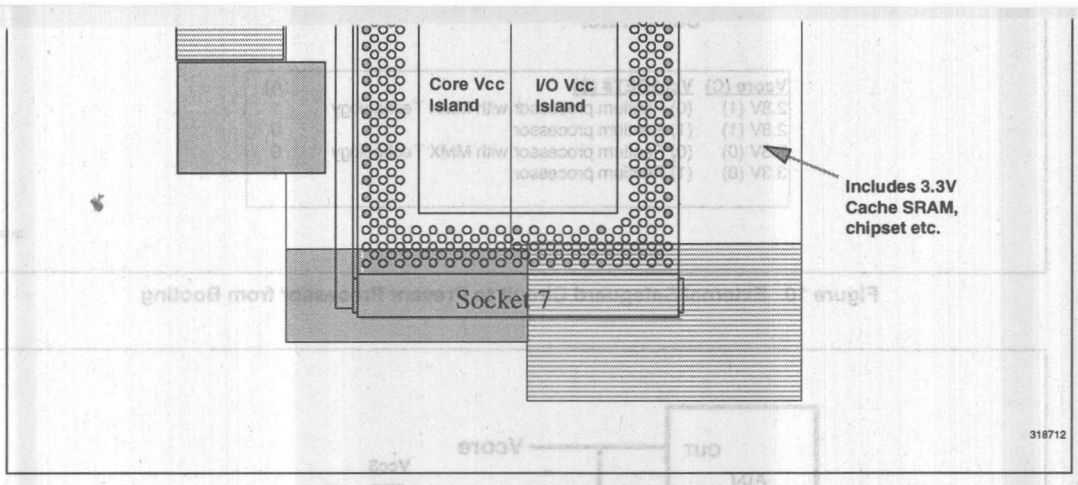


Figure 12. Processor Power Island Layout

The I/O V_{CC} island should also include other 3.3V components that interface with the processor. A typical configuration would include 3.3V cache SRAM, 3.3V chipset I/O, and processor I/O on the same 3.3V I/O voltage island. This ensures that signals interfacing between the processor and other 3.3V components operate at the same voltage levels. This is also to avoid split plane crossovers for these signals which is recommended for better signal quality and reduced EMI/RFI effects.

When using jumpers or 0Ω resistors to connect the two power planes (in the case of single voltage processors), the number of jumpers should be chosen so as to provide enough current carrying capability. Insufficient number of jumpers will result in excessive voltage drop and other reliability problems. For the flexible motherboard, a minimum of four (six recommended) zero-ohm, #1206, 1/8 watt, surface mount resistors should be used.

Routing of the power source to the voltage islands should also be carefully done to avoid significant voltage drop at the processor and an increase in thermal dissipation in the voltage islands. It is recommended that wide traces be used to prevent excessive voltage drop across the power plane. Also vias and through-holes cutting through the power plane at critical widths should be avoided.

3.7. Decoupling

The small size of the processor core voltage island, its isolation from the motherboard power plane, and support of varied voltage requirements make proper decoupling of the island power plane voltage and ground plane essential. Appropriate decoupling capacitors are implemented on the voltage island near the processor to ensure that the processor voltage stays within specified limits during normal and transient conditions. There are two types of decoupling that need to be considered: bulk decoupling and high frequency decoupling.

The Auto-HALT Power Down feature is always enabled even when other power management features are not implemented.

All of these examples may cause abrupt changes in the power consumed by the processor.

As the voltage supply (regulator) cannot respond to a sudden load change instantaneously, bulk storage capacitors with low ESR (Effective Series Resistance) are used to maintain the regulated supply voltage during the interval that falls between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

3.7.2. HIGH FREQUENCY DECOUPLING

High frequency decoupling may be required to provide a short, low impedance path to high frequency components such as high current spikes in order to

3.7.3. DECOUPLING RECOMMENDATIONS

Table 5 shows the processor decoupling recommendations for the flexible motherboard for both the processor core and I/O voltage islands. This is based on simulation and testing of the voltage transients from the processor and the effects of motherboard decoupling.

Spice modeling (modeling worst case current transients including the processor package inductance, capacitance, routing, decoupling, voltage regulator output inductance, etc.) should be used to estimate the amount of decoupling capacitance for the processor voltage island.

It is highly recommended that before committing to any change from the decoupling capacitor recommendation, the solution be simulated for the variety of variables in components, temperature and lifetime degradation.

Table 5. Decoupling Recommendations for Processor Core and I/O Voltage Islands

	Quantity	Value	ESR	ESL	Type
Processor Core Voltage Island	4	100 µF	25 mOhms (1)	0.45 nH (3)	Tantalum
	25	1 µF	0.6 mOhms (2)	0.084 nH (4)	X7R dielectric, ceramic
Processor I/O Voltage Island (5)	12	0.1 µF			603 Type

NOTES:

1. ESR per capacitor should be less than 100 mOhms.
2. ESR per capacitor should be less than 15 mOhms.
3. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.7 nH.
4. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.1 nH.
5. This does not include decoupling for components other than the processor in the 3.3V I/O voltage island.

For bulk decoupling, tantalum capacitors are recommended over electrolytic capacitors. In general, electrolytic capacitors degrade at a much faster rate, are not as accurate, and are not as stable over temperature as tantalum capacitors.

For high speed decoupling in the processor core voltage island, low inductance, 1µF capacitors of X7R dielectric are recommended. These capacitors not only decouple the processor core for high frequency noise but also control the voltage during very fast transients (less than 100 ns.) Figure 13 shows that ceramic capacitors of X7R (or X7S) dielectric exhibit relatively stable capacitor characteristics over temperature compared to capacitors of Z5U or Y5V type dielectric. For example, at a typical operating temperature of 45°C, the Y5V dielectric can lose 45% of the initial rated capacitance.

Measurement techniques to ensure that motherboard designs are within V_{CC} noise and transients specification are discussed in the following application notes (see Appendix E for order information).

- Voltage Guidelines for Pentium® Processors with MMX™ Technology Processors
- *Implementation Guidelines for Pentium® Processors with VRE Specifications*

3.7.4. PLACEMENT OF DECOUPLING CAPACITORS

Figure 14 shows an example of how the recommended processor decoupling capacitors (Table 5) should be placed inside the respective voltage islands on the flexible motherboard. The bulk capacitors should be placed near the processor inside the voltage island to ensure that the supply voltage stays within specified limits during changes in the supply current during operation. The 1 µF, X7R capacitors should be evenly distributed inside the processor core voltage island inside and around the processor footprint. Figure 12 also shows the twelve 0.1 µF capacitors evenly placed around the processor, close to the processor V_{CC3} pins inside the processor I/O voltage island.

In this example, all the capacitors were placed on one side of the board. If components are assembled on both sides of the board then these capacitors can be distributed between the top and bottom sides. If done this way, vias connecting the capacitor pads to the power and ground layer can be shared between the capacitors on the top and bottom sides. This can help reduce the total overall capacitor inductance.

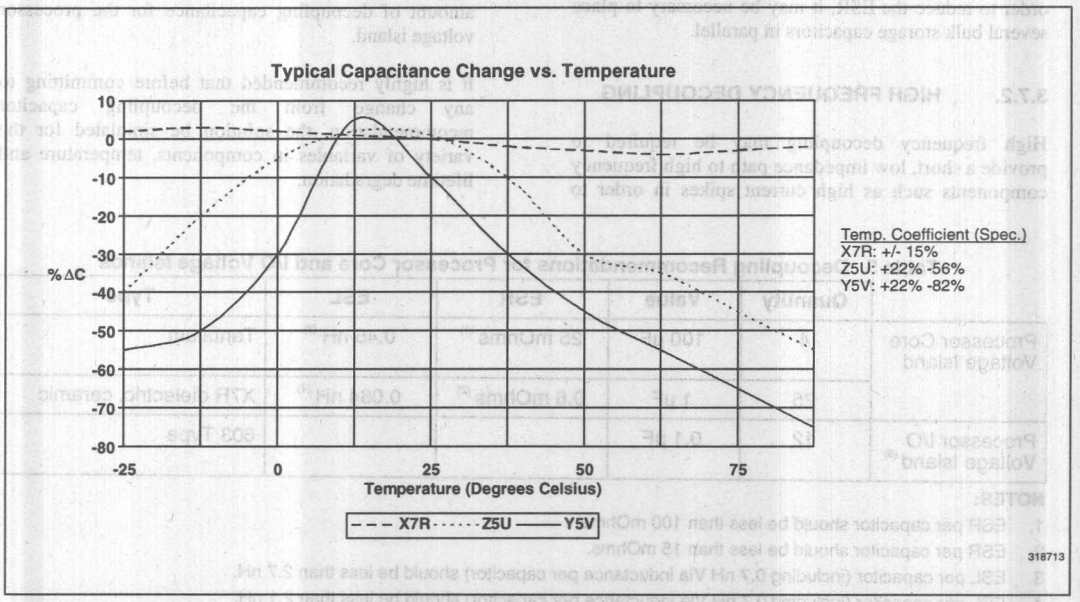


Figure 13. Typical Capacitor Characteristics

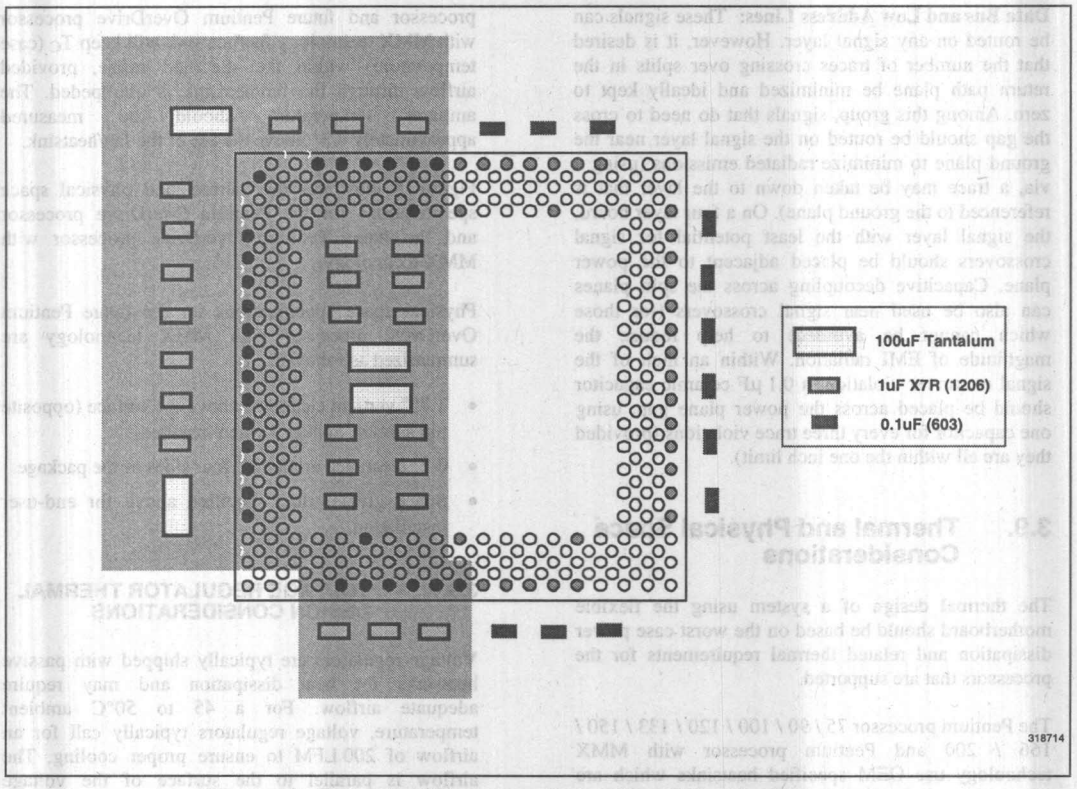


Figure 14. Example of Processor Decoupling Capacitor Placement

The traces connecting the vias to the capacitor pads should be kept as short as possible. In cases where it is difficult to reduce the length of the circuit board trace, the trace should be made wider so as to reduce the trace inductance.

3.8. Signal Routing Guidelines

As the power plane on the flexible motherboard is split into separate voltage islands, signal routing should be done in such a way so as to minimize crossovers between voltage islands for high speed signals. Signal routing between the voltage islands and the system power plane should be limited to only those signals that absolutely need to cross the gap between the island and the power plane. This is to avoid possible signal degradation from impedance discontinuity effects. Significant levels of EMI could be generated by electromagnetic radiation from high speed traces (such as clocks, strobes, data lines, and low address lines) when their return path is interrupted. On a multi-layer board this return path is on the power or ground plane that is adjacent to the signal layer directly under the signal trace. If this trace is routed over a break in the return path, the return current has to find another longer path in order to maintain current continuity. The increased area generated by the signal trace and the length of this extended return path can lead to increased radiation levels from this signal trace.

The following guidelines should be followed when routing high speed signals on the flexible motherboard:

Clocks and Strobes: These signals should not be routed over breaks in the reference plane return path. Use of vias to connect between signal planes should be minimized, and the signal planes should be within 8 mils of the reference plane. Clock signals should be routed on the layer that is adjacent to the ground layer.

Data Bus and Low Address Lines: These signals can be routed on any signal layer. However, it is desired that the number of traces crossing over splits in the return path plane be minimized and ideally kept to zero. Among this group, signals that do need to cross the gap should be routed on the signal layer near the ground plane to minimize radiated emissions (using a via, a trace may be taken down to the layer that is referenced to the ground plane). On a four layer board, the signal layer with the least potential for signal crossovers should be placed adjacent to the power plane. Capacitive decoupling across the split planes can also be used near signal crossovers (for those which cannot be avoided) to help reduce the magnitude of EMI radiation. Within an inch of the signal crossover violation, a 0.1 µF ceramic capacitor should be placed across the power plane gap, using one capacitor for every three trace violations (provided they are all within the one inch limit).

3.9. Thermal and Physical Space Considerations

The thermal design of a system using the flexible motherboard should be based on the worst case power dissipation and related thermal requirements for the processors that are supported.

The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium processor with MMX technology use OEM specified heatsinks which are dependent upon the entire system cooling solution. The maximum case temperature for these processors should not exceed 70°C to ensure proper operation. Heatsinks also may need a certain airflow in order to maintain their specified temperature. For detailed information refer to the respective datasheet for these processors (see Appendix E). In addition, detailed discussion of thermal design issues for the Pentium processor is covered in *Pentium® Processor Thermal Design Guidelines* (see Appendix E).

The Pentium OverDrive processors and future Pentium OverDrive processors with MMX technology are shipped with integrated fan/heatsink cooling solutions. Although these fan/heatsinks remove the heat from the package, the system should be able to dissipate the added heat to the system. From Table 1, the future Pentium OverDrive processor with MMX technology dissipates the most power at 200 MHz. The system provides sufficient airflow to dissipate this power from the system and prevent the temperature of the air entering the fan/heatsink from exceeding 45°C. When the T_A (max) ≤ 45°C specification is met (T_A = ambient temperature), the Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology fan/heatsink will keep T_C (case temperature) within the specified range, provided airflow through the fan/heatsink is unimpeded. The ambient temperature should be measured approximately 0.3" above the top of the fan/heatsink.

Figure 15 illustrates the thermal and physical space specifications for the Pentium OverDrive processor and the future Pentium OverDrive processor with MMX technology.

Physical space specifications for the future Pentium OverDrive processor with MMX technology are summarized as follows:

- 1.75" vertical clearance above the surface (opposite pin side) of Socket 7 when installed.
- 0.2" clearance around all four sides of the package.
- Space greater than specified above for end-user installation.

3.9.1. VOLTAGE REGULATOR THERMAL DESIGN CONSIDERATIONS

Voltage regulators are typically shipped with passive heatsinks for heat dissipation and may require adequate airflow. For a 45 to 50°C ambient temperature, voltage regulators typically call for an airflow of 200 LFM to ensure proper cooling. The airflow is parallel to the surface of the voltage regulator to ensure that the heatsink receives adequate airflow. Refer to your voltage regulator datasheet for actual specifications.

3.9.2. DESKTOP SYSTEM THERMAL DESIGN CONSIDERATIONS

To avoid localized heating at the processor, a clear air path and adequate venting is provided to prevent hot spots from occurring. A typical solution to this thermal problem is to add an auxiliary fan to the front vents of the chassis, directing airflow across the processor. While this solution would appear to be fairly simple, the addition of a second fan can actually cause the problem to intensify. Unless the front vents are of sufficient size, and placement of the fan is carefully considered, the auxiliary fan can actually cause the air heated by the processor and other components to be re-circulated within the system rather than expelled out the back of the chassis. This heated air can easily raise the temperature around the processor beyond the temperature specifications for the components in the system.

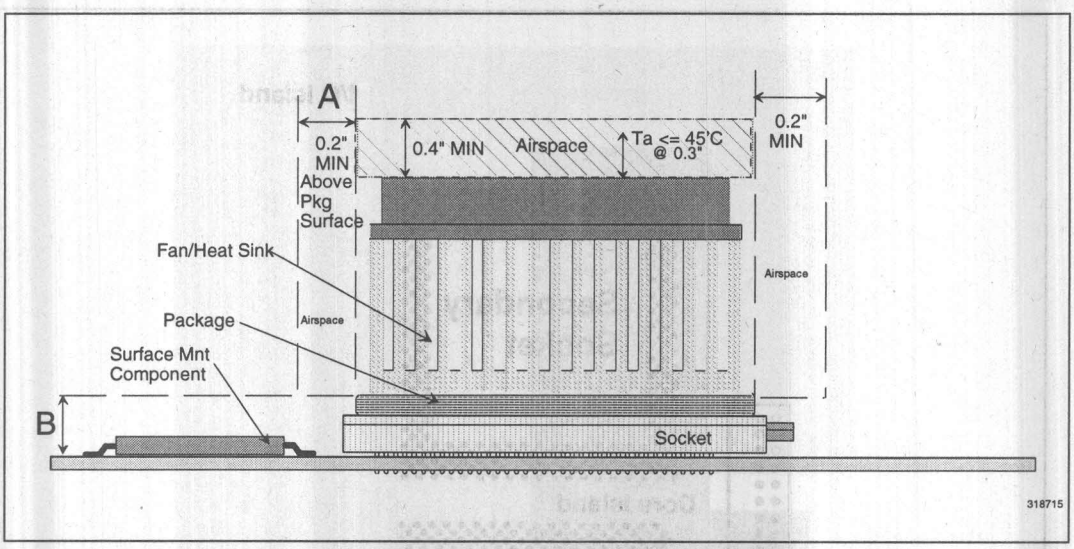


Figure 15. Thermal and Physical Space Requirements for the Pentium® OverDrive® Processor with MMX™ Technology

When adding an auxiliary fan to the system, the size of the chassis vents deserves special consideration. The fan is most effective when all of the air pushed through the fan blades comes from outside the chassis. If the vents are too small or inadequate for the fan velocity, gaps between the fan and chassis will cause air from inside the system to be drawn through the fan, causing re-circulation of heated air. The position of the fan is also critical. The highest air flow is from the blades and not from the center of the fan. Care should be taken not to block the blades with frame supports.

For details on Baby AT style chassis design suggestions, refer to the application note, *Pentium® Processor Chassis Design Suggestions* available on CD-ROM (See Appendix E).

3.10. BIOS/Software Considerations

As the flexible motherboard can accommodate a variety of processors, the BIOS is designed such that it can support all the different processors on the flexible motherboard. The BIOS code should use the CPUID instruction to identify the processor's CPUID signature (see Section 2.3.).

Other considerations for BIOS/software on the flexible motherboard include the following:

- Processor test code should be independent of model specific registers (MSR). Various processors have different caches, test registers, and core architecture; e.g. the Pentium processor with MMX™ technology's cache size and associativity is different from the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 resulting in differences in cache test registers.
- Since processors of various core frequencies are supported on the flexible motherboard, BIOS code should not contain any software timing loops and should be independent of the prefetch algorithm.

3.11. Dual Processor Design Considerations

The Pentium processor family flexible motherboard may also be designed as one planar board to support uni-processor (UP) and dual-processor (DP) modes. This provides the flexibility of using the same motherboard populated with either one socket (for UP system) or two sockets (for DP system.) Figure 16 shows the layout for a split plane flexible motherboard designed with two sockets.

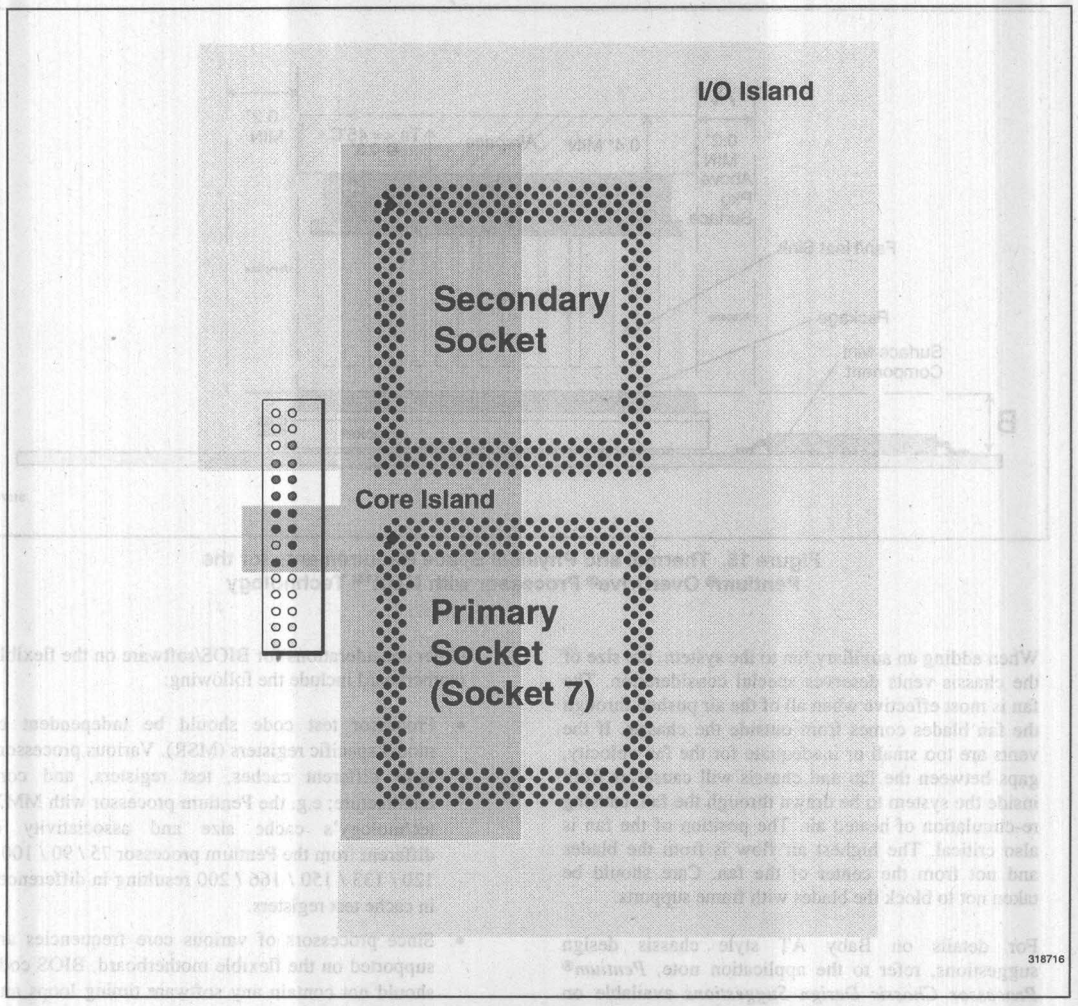


Figure 16. Layout of a DP Flexible Motherboard

The following needs to be considered when designing a split plane flexible motherboard with two sockets:

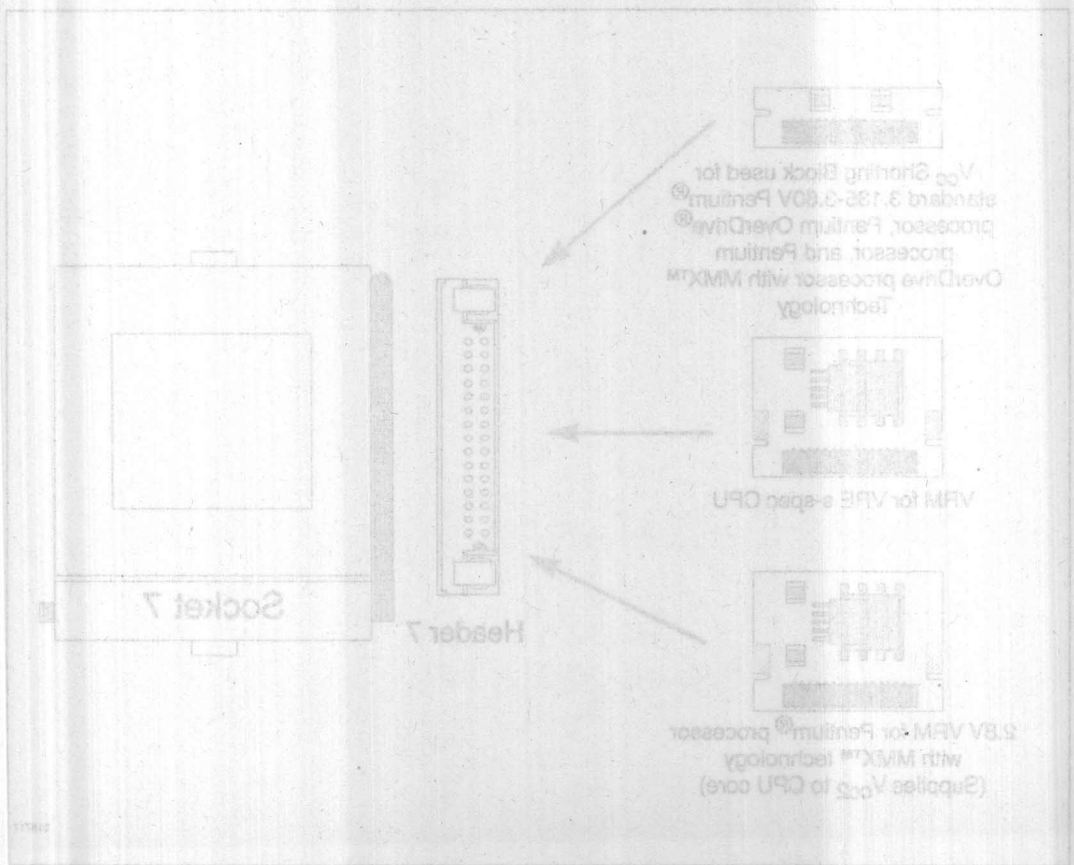
- The power islands should be laid out such that the processor cores share one common island and the I/O share another island. This minimizes the number of islands resulting in better signal quality and reduced EMI effects.
- Socket 7 should only be used at the primary socket location. The secondary socket footprint should not be designed with the Socket 7 footprint.

NOTE

Pentium OverDrive processors and future Pentium OverDrive processor with MMX technology do not support dual processor operation. The 296-pin LIF or ZIF socket should be used at the secondary socket location.

- The primary socket location should always be populated. The nets should be balanced for worst case timing when the primary processor is driving the bus.

- A single on-board voltage regulator (or VRM) should be used to support one or two processor cores. The on-board voltage regulator is located close to the processor such that the resistance and inductance is minimized.
- The recommended decoupling capacitors (Section 3.3.) should be used for each processor location to ensure that the voltage for each processor stays within specified limits during normal and transient conditions.
- The on-board voltage regulator (or VRM) needs to provide sufficient current in DP mode to support two processors unified on a single motherboard power plane and other 3.3V I/O current requirements in the I/O voltage island. For a 200 MHz, split-plane, dual-voltage input, DP Pentium processor with the MMX technology system, this amounts to approximately 11.4A at 2.8V and approximately 3–4A at 3.3V of typical current requirement. This assumes 5.7A at 2.8V for each of the processors, 1A for each of the dedicated 512K cache, and approximately 1.0A for the chipset. Actual current requirements will vary based on the devices used. In particular, current requirements should be carefully analyzed if implementing 3.3V DRAM powered from the I/O voltage island.



APPENDIX A

A1.0. VOLTAGE REGULATOR MODULE

The Voltage Regulator Module (VRM) offers flexibility in that it allows processors with different voltage and current requirements to be easily supported on the flexible motherboard. The VRM is a voltage converter with a pinout capable of converting a system power supply voltage to the voltage necessary for the processor core. The only difference between the VRM and a voltage regulator on the motherboard is the pinout and ease in changing the processor supply voltage after assembly. By following a common pinout specification, a variety of VRMs may be developed by the OEM and third party vendors to support the Pentium processor family.

Figure 17 shows how the Voltage Regulator Module allows processors with different voltage and current requirements to be supported on the flexible motherboard using interchangeable VRMs.

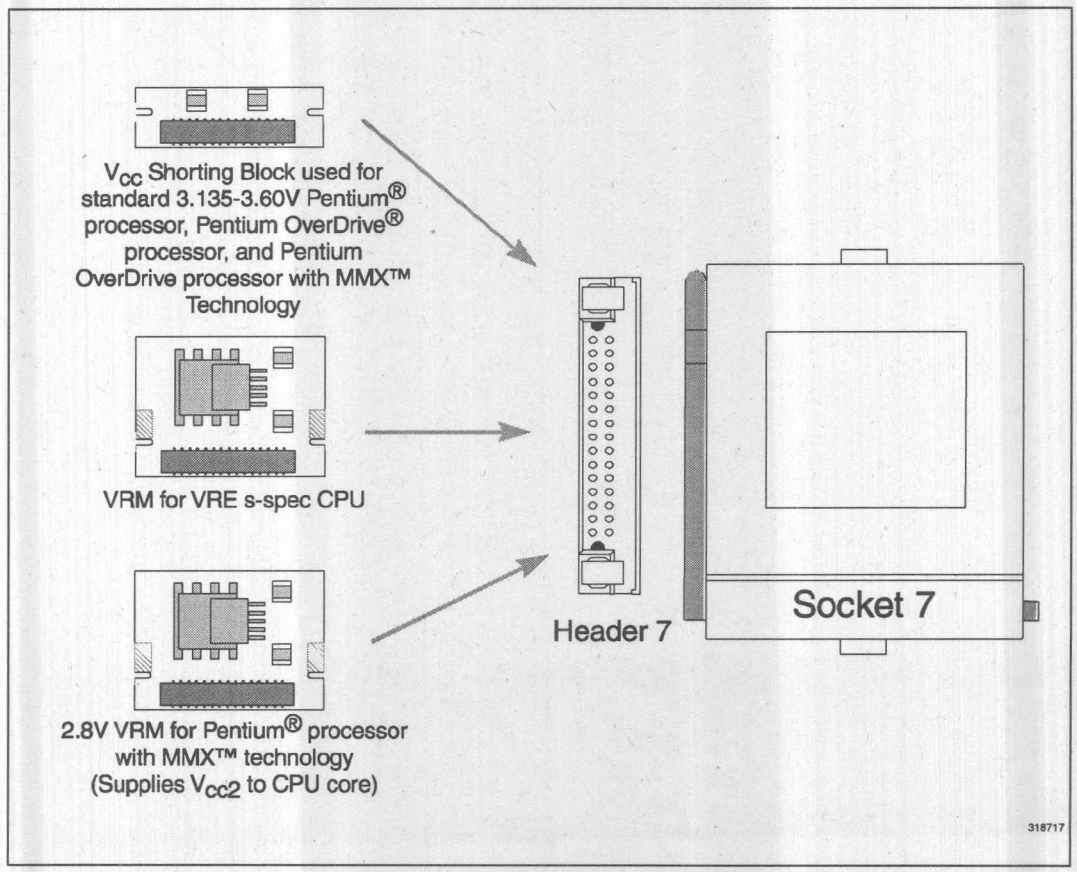


Figure 17. Voltage Regulator Modules

When the processor socket is populated with either the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the Pentium OverDrive processor, the Pentium processor with MMX technology or the future Pentium OverDrive processor with MMX technology, an OEM shorting block (pass-through module) can be installed in the VRM socket which allows 3.3V from the power supply (or on-board 3.3V regulator) to pass through to the processor core and I/O voltage islands.

When the processor socket is populated with a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, a Pentium OverDrive processor, or a future Pentium OverDrive processor with MMX technology running on VRE voltage, a VRM designed for the specific operating voltage is used to supply the proper voltage to the core and I/O voltage islands.

NOTE

The VRM in this case needs to supply sufficient current to support higher frequency upgrade processors (Pentium OverDrive processor or future Pentium OverDrive processor with MMX technology) when installed.

When the processor socket is populated with the Pentium processor with MMX technology, a 2.8V VRM is installed in the VRM socket to supply 2.8V to the processor core's V_{CC2} pins. The 3.3V supplied to the processor I/O is not provided by the VRM in this case. The VRM only supplies 2.8V to the core V_{CC2} pins. The Pentium processor with MMX technology VRM, however, will have provisions to allow 3.3V from the power supply to pass through to the processor I/O voltage island.

Table 6 summarizes the *typical* processor voltage supply configuration with the VRM.

A1.1. Header 7

The VRM header (Header 7) is a 30-pin shrouded header with retaining clips. The retaining clips in the header hold the VRM in place when installed properly. The pins are set as 2 x 15 matrix. The power pins are capable of carrying up to 2A each.

The definition of Header 7 connections include: eight input voltage pins (four pins for +3.3V input, four pins for +5V input); ten output voltage pins (seven V_{CORE} pins that supply voltage to the processor core and three $V_{I/O}$ pins that connect to the voltage island supplying the processor V_{CC3} pins); three control signal pins (Disable input, Power Good output, Sense input); seven V_{SS} pins (Ground reference); one +12V pin (+12V or NC); and one RES pin (reserved for future use). Refer to the end of Appendix A for the VRM pinout and quick pin reference.

The 5V input pins on Header 7 are intended for regulation to 3.3V or 2.8V or any other voltage necessary for the processor. The 3.3V inputs can also be used for regulation (e.g. 2.8V) or as a source to connect to the processor 3.3V I/O plane through the $V_{I/O}$ pins. The +12V reference is used on some of the VRM's targeting VRE specifications. It is recommended to route +12V to this pin.

Table 6. Typical Processor Voltage Supply Configuration with VRM

	Core V_{CC}	I/O V_{CC}
Pentium® processor STD voltage (3.135V – 3.60V)	Shorting Block	Same as Core V_{CC} (1)
VRE (3.40V – 3.60V)	3.40V to 3.60V VRM (2)	Same as Core V_{CC}
Pentium processor with MMX™ technology	2.8V VRM	3.3V Power Supply or on-board 3.3V regulator
Pentium OverDrive® processor and future Pentium OverDrive processor with MMX technology	Shorting Block	Same as Core V_{CC}

NOTES:

1. Core and I/O voltages are supplied by the 3.3V power supply or an on-board 3.3V voltage regulator through the VRM header.
2. 3.40V to 3.60V VRM supplies voltage to the processor core, I/O and other 3.3V components on the motherboard that interface with the processor. The VRM is able to supply enough current (7A typical) to the processor, 3.3V cache and chipset in the processor I/O voltage island.

The primary output of the VRM is through the V_{CORE} pins. These pins supply the voltage necessary for the processor core. The $V_{I/O}$ output pins are connected to the processor power plane supplying the processor V_{CC3} pins. These $V_{I/O}$ pins are connected to the V_{CORE} pins on VRMs that need to power both the processor core and I/O from a single source (e.g. VRE VRMs.)

The control signals DISABLE and PWRGOOD on the VRM header are optional control signals provided for system use. It is up to the discretion of the OEM to decide whether to implement circuitry to use these features. The SENSE input, however, allows voltage regulators on the modules to adjust their output voltage to correct for a voltage drop through the connectors and power plane. SENSE should be routed to a point in the center of the processor core voltage island. The sense line can make contact to the power plane through a via supporting one of the decoupling capacitors.

If the flexible motherboard is designed with a VRM header, the +3.3V inputs on the VRM header are connected directly to the $V_{I/O}$ pins through the module (Pentium processor with MMX technology VRM) to supply the processor I/O voltage island. In the case where a VRE VRM is used, the module connects the V_{CORE} output pins to the $V_{I/O}$ pins to allow both islands to obtain the same voltage. The best solution for connecting the output of the 3.3V or VRE supply to both the voltage planes, when a unified plane processor is used, is through the VRM header. A shorting block in the VRM header to connect the 3.3V supply inputs on the VRM to the V_{CORE} and $V_{I/O}$ outputs will provide the best electrical performance.

A1.2. Shorting Block or Pass-Through Module

The shorting block or Pass-Through Module is nothing more than a connector which shorts the 3.3V input pins to the V_{CORE} and $V_{I/O}$ pins on the VRM header. This is used with the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the Pentium OverDrive processor, and the future Pentium OverDrive processor with MMX technology. The shorting block allows voltage from the 3.3V power supply or on-board 3.3V voltage regulator to pass through to the processor core and I/O voltage islands.

A1.3. VRM for Processors Running at VRE

The Voltage Regulator Module concept allows VRE (3.40V to 3.60V) processors to be easily supported on the flexible motherboard. A VRM designed for the VRE voltage range is used in Header 7 to supply the VRE processors. The VRM in this case supplies voltage to the processor core, I/O and other 3.3V components on the motherboard that interface with the processor. The VRM provides adequate current for all these components.

A1.4. VRM for Pentium® Processor with MMX™ Technology

The VRM for the Pentium processor with MMX technology supplies 5.7A at 2.8V (200 MHz) for the processor core. The VRM will regulate down to 2.8V from either 5V or 3.3V. The 3.3V supplied to the processor I/O will come from the 3.3V system power supply or on-board 3.3V regulator. The Pentium processor with MMX technology VRM will have the +3.3V inputs shunted to the $V_{I/O}$ outputs to allow 3.3V inputs to the VRM header to pass through to the 3.3V processor I/O voltage island.

NOTE

The Voltage Regulator Module for 2.8V processors will not generate the 3.3 volts for the processor I/O supply. This is necessary due to space constraints of the module and the potential power limitations for 3.3V components. The modules for 2.8V processors can connect the $V_{I/O}$ pins to the 3.3V input for ease of implementation. The system provides adequate current for the 3.3V components on the $V_{I/O}$ plane.

A1.5. VRM Header Placement

The VRM header should be located close to the processor socket. This is to prevent an excessive voltage drop across the power plane and allow the header to be easily located. It is recommended that the VRM header be located no further than 1 inch from the processor socket.

NOTE

The VRM specifications allow for a maximum of 7 mOhms resistance and a maximum of 3.4 nH inductance from VRM to processor V_{CC2} pins.

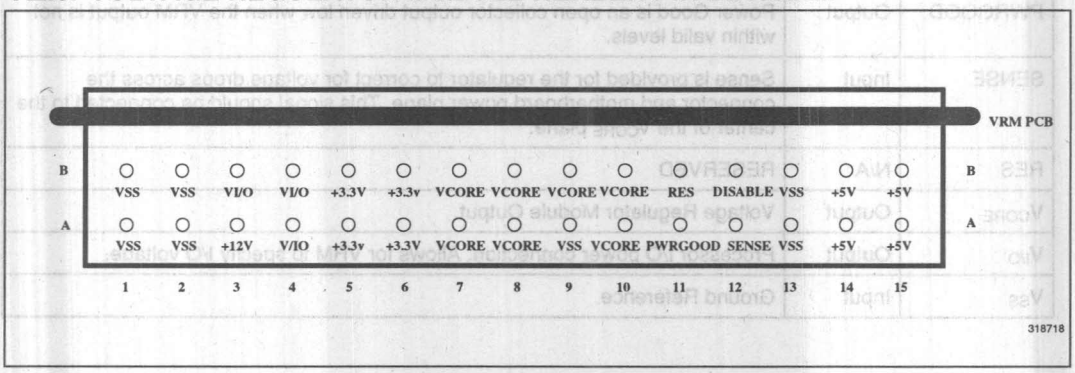
The VRM header should be placed such that it provides easy routing of the core and I/O voltage islands from processor to VRM. The header may be located on the handle side of Socket 7 or any of the two sides that are closest to the handle side. Placing the header on the side that is opposite to the handle side is not recommended as it increases the distance from VRM to the processor, thereby increasing the voltage drop across the power

plane. It also makes routing to the core island more difficult. If the VRM header is placed on the handle side of Socket 7, it should be located no closer than 0.5 inch to the ZIF handle. This clearance allows easy access to the socket handle.

Location of the VRM header with respect to the processor socket should also take into consideration the following:

- The distance from motherboard surface to VRM component overhang should be kept at a minimum vertical distance of 0.55".
- Ease of routing the 3.3V voltage island from the 3.3V power supply to the +3.3V inputs on the VRM header.
- The VRM does not impede the installation of full size add-in cards in the I/O slots.
- The VRM is located such that it receives adequate airflow to ensure proper cooling. The airflow is parallel to the surface of the VRM to ensure that the heatsink on the VRM receives adequate airflow.
- Use of logic analyzer probes — The VRM header is placed such that is does not impede the installation of probes into the processor socket.

A2.0. VOLTAGE REGULATOR MODULE HEADER PIN DIAGRAM

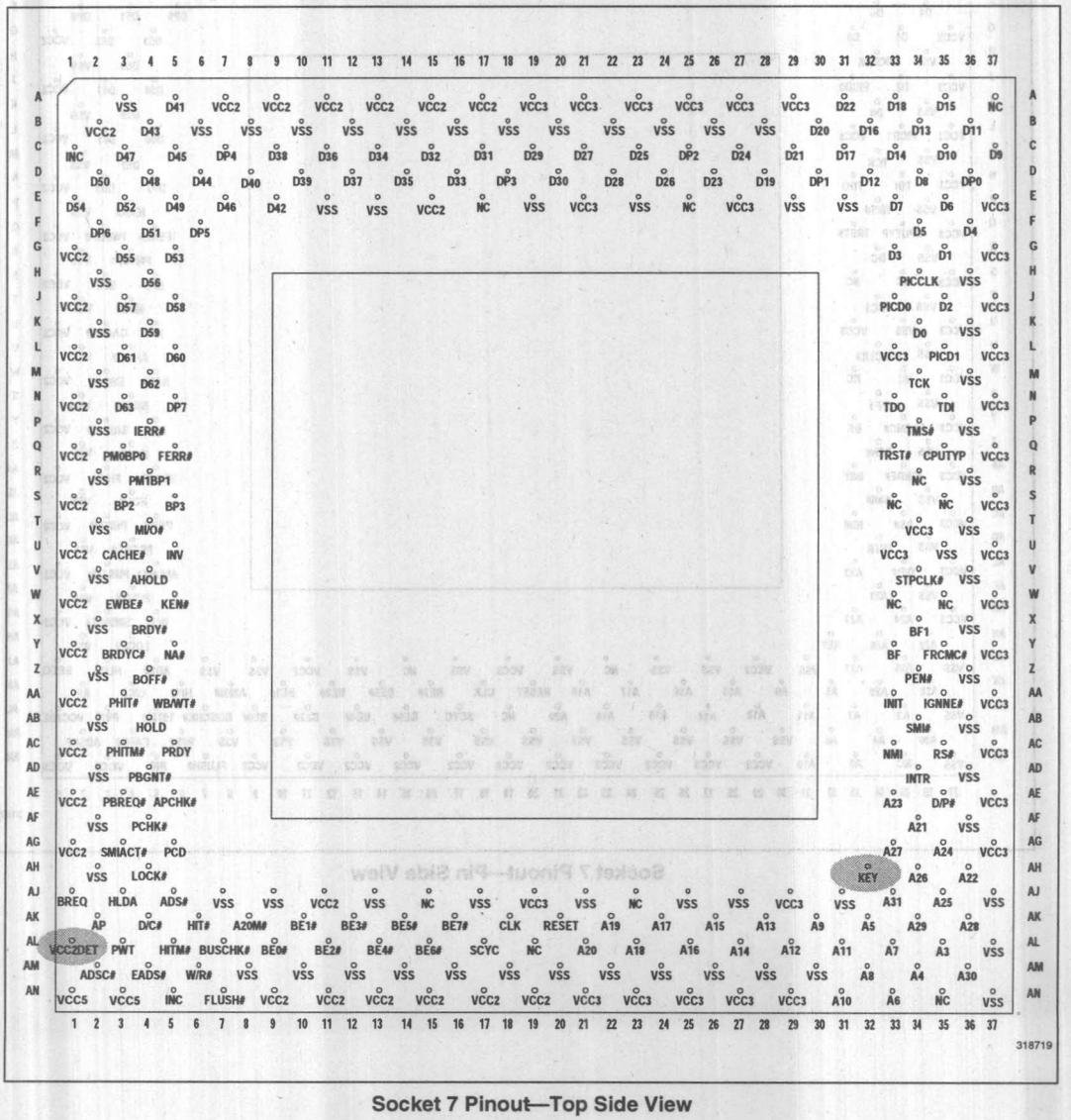


VRM Pinout Top Side View

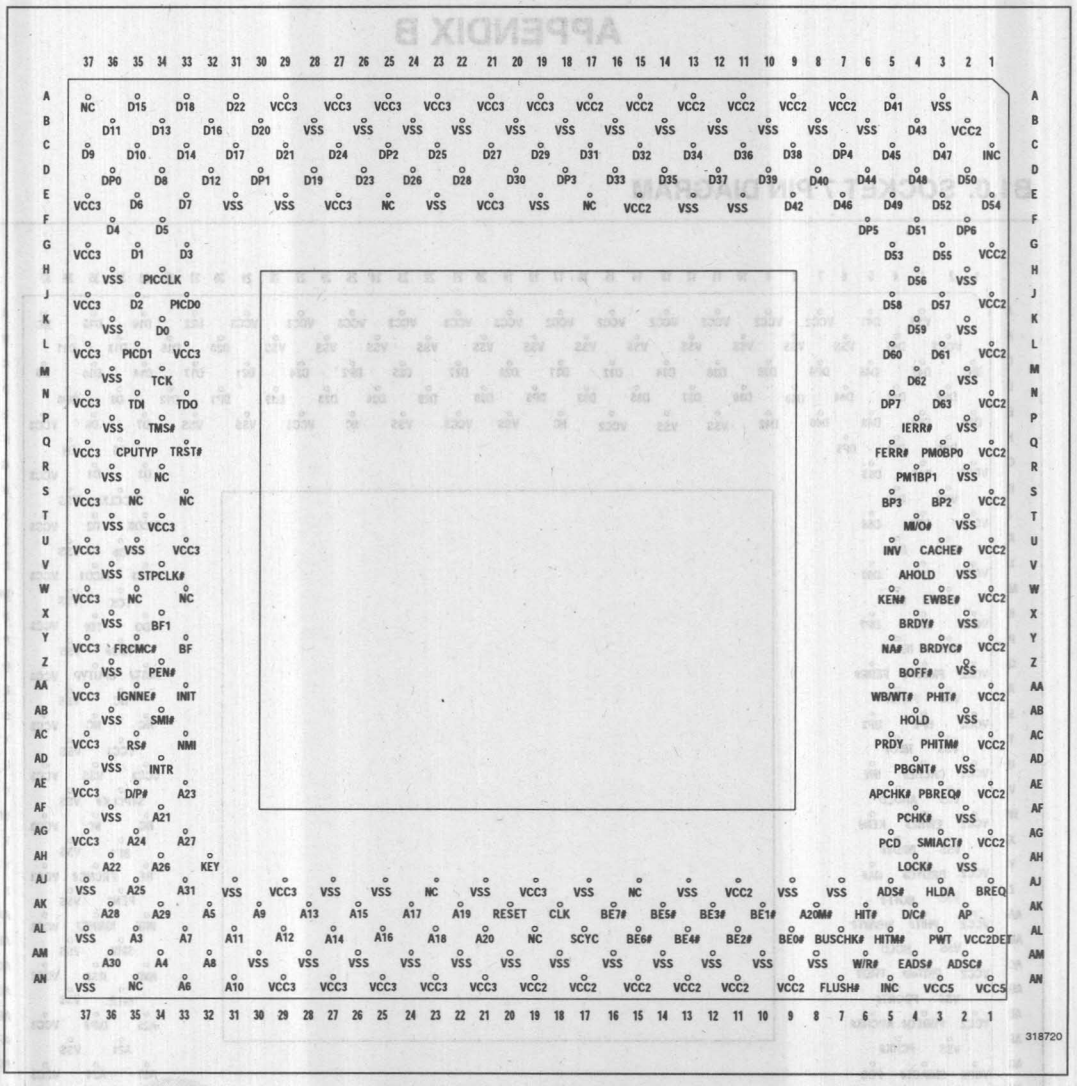
DISABLE	Input	When driven high, this input will disable the Voltage Regulator Module output and the output of the module will float.
PWRGOOD	Output	Power Good is an open collector output driven low when the VRM output is not within valid levels.
SENSE	Input	Sense is provided for the regulator to correct for voltage drops across the connector and motherboard power plane. This signal should be connected to the center of the V_{CORE} plane.
RES	N/A	RESERVED
V_{CORE}	Output	Voltage Regulator Module Output.
$V_{I/O}$	Output	Processor I/O power connection. Allows for VRM to specify I/O voltage.
V_{SS}	Input	Ground Reference.

APPENDIX B

B1.0. SOCKET 7 PIN DIAGRAM



Socket 7 Pinout—Top Side View



Socket 7 Pinout—Pin Side View

B2.0. SOCKET 7 QUICK PIN REFERENCE

Socket 7 has the same pin definition as Socket 5 with the exception of the following pins.

Symbol	Type	Name and Function
CLK, PICCLK	(I)	Unlike some Pentium® processors, the **Clock and Programmable Interrupt Controller Clock** inputs to Socket 7 are **not** 5V tolerant. These inputs are driven by an appropriate 3.3V clock driver.
KEY	NA	The KEY pin is strictly a mechanical keying device for future Pentium OverDrive® processors. The hole in the socket permits installation of the higher speed Pentium OverDrive processors. The corresponding pin on the Pentium OverDrive processors is an Internal No Connect and has no electrical purpose. This pin is not populated on 320-pin packages.
VCC2DET#	(O)	**V_{CC2} Detect** is defined for the Pentium processor with MMX™ technology which uses a supply of 2.8 volts on the V_{CC2} pins. The Pentium processor with MMX technology with a core voltage of 2.8 volts, will always drive V_{CC2DET} low. This pin may be used to select the proper core voltage from a voltage regulator or system supply. This pin is not driven high on 3.3 volt Pentium processors or Pentium OverDrive processors. The VCC2DET# system trace has a pull-up for proper use
V_{CC2}	(I)	Socket 7 has 28 power supply pins defined for the core voltage on processors with separate power inputs. For processors with a single power supply requirement, these pins can be considered the same as V_{CC3} pins and should be driven with the same power source.
V_{CC3}	(I)	Socket 7 has 32 power supply pins defined for the I/O voltage on processors with separate power inputs. For processors with a single supply requirement, these pins are used in conjunction with the V_{CC2} pins to power the device.

APPENDIX C

C1.0. LINEAR AND SWITCHING REGULATOR SOLUTIONS

Appendix C contains a list of Linear/Switching Voltage Regulator solutions. These lists may not be all inclusive or accurate of all vendor solutions, but they are intended as a voltage regulator reference lists for known 2.8V/3.3V/VRE regulator solutions. Please contact your vendor for their latest product specifications.

2.8V/3.3V/VRE Linear Regulator Solutions

		Electrical						Availability	
Vendor	Part Number	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Power (Max) (W)	Remote Sense	Package	Sample	Product
Cherry	CS5206	5	2.8	6	17	No	TO-220/ D^2Pak	Now	Now
		5	3.3/ VRE	6	20				
	CS5207A	5	2.8	7	20	Yes	TO-220	Q4'96	Q4'96
		5	3.3/ VRE	7	23				
Linear Tech	LT1575 (+ ext FET)	3.3	2.8	10	5	Yes	8-pin SOIC	Now	Now
		5	2.8	10	22				
		5	3.3/VRE	10	27				
	LT1577 (Dual)	5	2.8	10	22	Yes	16-pin SOIC	Now	Now
		5	3.3/VRE	10	27				
	LT1580	5	2.8	7	15.4	Yes	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	LT1584	5	2.8	7	15.4	No	TO-220/ TO-263	Now	Now
		5	3.3/VRE	7	11.9				
	LT1585A	5	3.3	5	8.5	No	TO-220/ TO-263	Now	Now
Linfinity	LX8384	5	3.3/VRE	5	8.5	No	TO-220/ TO-263	Now	Now
	LX8585	5	3.3/VRE	4.6	7.82	No	TO-220/ TO-263	Now	Now
	LX8586	5	2.8	6	13.2	No	TO-220/ TO-247	Now	Now
		5	3.3/VRE	6	10.2				

2.8V/3.3V/VRE Linear Regulator Solutions (Contd)

Vendor	Part Number	Electrical				Remote Sense	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Power (Max) (W)			Sample	Product
National	LM2951	5	2.8	7	15.4	No	SO-8	Now	Now
		5	3.3/VRE	7	11.9				
	LM3411	5	3.3/VRE	7	11.9	No	SO-8/ 5-pin SOT 23	Now	Now
Raytheon	RC5102 (Dual)	5	2.8	7	15.4	Yes	8-pin SOIC	Now	Now
		5	3.3/VRE	7	11.9				
Semtech	EZ1083/A	5	2.8	7.5	16.5	No	TO-220 or TO-247	Now	Now
		5	3.3/VRE	7.5	12.75				
	EZ1082	5	2.8	10	22.0	No	TO-220 or TO-247	Now	Now
		5	3.3/VRE	10	17				
	EZ1584A	5	2.8	7	15.4	No	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1900	5	2.8	7	15.4	No	8-pin SOIC	Now	Now
	(Dual)	5	3.3/VRE	7	11.9				
	EZ1580	5	2.8	7	15.4	Yes	5-pin TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1585D	5	2.8	6	13.2	No	TO-220	Now	Now
		5	3.3/VRE	6	10.2				
Unisem	US1080	5	2.8	8	17.6	No	TO-220/ TO-263	Q1'97	Q1'97
		5	3.3/VRE	8	13.6				

2.8V/3.3V/VRE Switching Regulator Solutions

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
Cherry	CS5120	5	2.8	5.7	92%	2	14-pin PDIP	Now	Now
		5	3.3/VRE	5.7	92%		14-pin SOIC		
Harris	HIP5010	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5011	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5010	5	2.8	6	89%	2	7-pin TO-220 or	Now	Now
		5	3.3/VRE	6	92%		7-pin D^2Pak		
	HIP5016	5	2.8	6	89%	2	7-pin TO-220 or	Now	Now
		5	3.3/VRE	6	92%		7-pin D^2Pak		
Linear Tech	LTC1266	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
	LTC1430	5	2.8	15	93%	2	16-pin SOIC or	Now	Now
		5	3.3	15	95%		8-pin SOIC		
	LTC1435	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
Linfinity	LX1660/1	5	2.8	12	85%	2	SO-16	Q4'96	Q4'96
		5	3.3/VRE	12	85%				
Maxim	MAX797	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				
	MAX798	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				

2.8V/3.3V/VRE Switching Regulator Solutions (Cond)

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
National	LM3578 & LM3411	5	3.3/VRE	10	88%	1	SO-8 or 5-pin SOT23	Now	Now
Raytheon	RC5036 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5031	5	2.8	10	87%	1	14-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5035 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
Siliconix	Si9140	5	2.8	6	90%	2	16-pin SOIC	Now	Now
		5	3.3	6	90.5%				
	Si9145	5	2.8	6	82%	1	16-pin SOIC or	Now	Now
		5	3.3/VRE	6	83%		16-pin TSSOP		
Unitrode	UC3886	5	2.8	10	85%	1	16-pin SOIC or	Now	Now
		5	3.3/VRE	10	85%		16-pin DIP		
	UCC3881	5	2.8	10	85%	1	16-pin SOIC or	Now	Q1'97
		5	3.3/VRE	10	85%		16-pin DIP		
	UCC3880	5	2.8	10	85%	1	20-pin SOIC or	Now	Now
		5	3.3/VRE	10	85%		20-pin DIP		
	UC3874	5	2.8	10	90%	2	18-pin SOIC or	Now	Now
		5	3.3/VRE	10	90%		18-pin DIP		
Unisem	US2050	5	2.8	10	85%	1	7-pin TO-220	Q1'97	
		5	3.3/VRE	10	85%		or TO-263		

APPENDIX D

D1.0. REGULATOR VENDOR SOLUTIONS CONTACT LIST

On-board Regulators

Vendor	North America	Europe	Asia	Japan
Cherry	Dennis Gatano Tel: (401) 886-3305 Fax: (401) 885-5786			
Harris	Dean Henderson Tel: (919) 405-3603 Fax: (919) 405-3651	Robert Lahaye Tel: (33) 1 346 54046 Fax: (33) 1 394-64054	Jason Lin Tel: (886) 2 716 9310 Fax: (886) 2 715 3029	Masaru Agano Tel: (81) 3 3265 7571 Fax: (81) 3 3265 7575
Linear Tech	Bob Scott Tel: (408) 432-1900 Fax: (408) 434-0507	Fred Killinger Tel: (49) 89 9642550 Fax: (49) 89 963147	Dave Quarrels Tel: (65) 753 2692 Fax: (65) 754 4112	
Linfinity	Andrew Stewart Tel: (714) 898-8121 Fax: (714) 893-2570			
Maxim	David Timm Tel: (408) 737-7600 Fax: (408) 737-7194	David Watson Tel: (44) 17 3430 3388 Fax: (44) 17 3430 5511	Steve Huang Tel: (886) 2558 6801 Fax: (886) 2555 6348	Tadi Kodairo Tel: (81) 3 3232 6141 Fax: (81) 3 3232 6149
National	Venkatesh Shan Tel: (408) 721-3753 Fax: (408) 721-8763	Werner Obermaier Tel: (49) 81 4135 1331 Fax: (49) 81 4135 1220	Vincent Lin Tel: (852) 2737 1616 Fax: (852) 2736 9931	Mark Kachmerak Tel: (81) 43 299 2373
Raytheon	David McIntyre Tel: (415) 9667734 Fax: (415) 966-7742	David Frye Tel: (44) 17 0566 5555 Fax: (44) 17 0566 3355	Mike Wisnia Tel: (81) 3 3406 5998 Fax: (81) 3 3406 5998	
Semtech	Gene Krzwinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Siliconix	Erik Ogren Tel: 408-970-5543 Fax: 408-567-8910	Sean Montgomery Tel: (44) 344 485757 Fax: (44) 344 427371	Serge Jaunay Tel: (852) 2378 9715 Fax: (852) 2375 5733	Tony Grizelj Tel: (81) 3 5562 3321 Fax: (81) 3 5562 3316
Unitrode	John O'Connor Tel: (603) 429-8504 Fax: (603) 429-8963	David Wells Tel: (44) 181 318 1431 Fax: (44) 181 318 2549	Wilkie Wong Tel: 8522-722-1101 Fax: 8522-369-7596	
Unisem	Reza Amirani Tel: (714) 453-1008 Fax: (714) 453-8748			

Voltage Regulator Modules

Vendor	North America	Europe	APAC	Japan
Ambit	Leonard Kao Tel: (886) 35-7849575 Fax: (886) 35-782924			
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 1753-67-6800 Fax: (44) 1753-67-6801	Joe Navin Tel: (81) 44-813-8507 Fax: (81) 44-813-8500	
C-MAC	Dave Holmes Tel: (407) 881-2321 Fax: (407) 881-2342			
Corsair	John Beckley Tel: (408) 559-1777 Fax: (408) 559-4294			
Semtech	Gene Krzywinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Raytheon	David McIntyre Tel: (415) 966-7734 Fax: (415) 966-7742	David Frye Tel: 44 17 0566 5555 Fax: 44 17 0566 3355	Mike Wisnia Tel: 81 3 3406 5998 Fax: 81 3 3406 5998	
VXI	Joseph Chang Tel: (503) 652-7300 Fax: (503) 786-5011			

Socket 7

Vendor	North America	Europe	APAC	Japan
Amp	Bob Branden Tel: (910) 855-2247 Fax: (910) 855-2224	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Appros	Hiroshi Narita Tel: (81) 45-941-4080			
Augat	David M. Barnum Tel: (508) 699-9890 Fax: (508) 695-8111	Arif Shahab Tel: (44) 952-670-281 Fax: (44) 952-670-342	Atsushi Sasaki Tel: (81) 44-853-5400 Fax: (81) 44-853-1113	
Foxconn	Julia Jang Tel: (408) 749-1228 Fax: (408) 749-1266		Wesley Lin or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Yamaichi	Ann Sheperd Tel: (408) 456-0797 Fax: (408) 456-0779	Mr. Matsuda Tel: (49) 89-451021-43 Fax: (49) 89-451021-10	Alan Liu Tel: (886) 02-546-0507 Fax: (886) 02-546-0509	Mr. Shiwaku Tel: (81) 3-3778-6161 Fax: (81) 3-3778-6181
Berg/ McKenie	Fred Baldwin Tel: (510) 651-2700 Fax: (510) 651-1020			

Decoupling Capacitors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1µF, X7S	Dennis Lienemann Tel: (803) 946-0616	Steve Chan (Singapore) Tel: (65) 258-2833 Fax: (65) 258-8221
	TPSD107K010R0100	100µF, Tantalum	Fax: (803) 946-6678	K.J. Kim (Korea) Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
Johanson Dielectrics	160R18W105K4	1µF, X7R	Dave Lopez Tel: (818) 364-9800 Fax: (818) 364-6100 NCTR (California only) Tel: (510) 624-8900 Fax: (510) 624-8905	Bill Yu (Taiwan) Nanco Electronics Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Sales Dept (Hong Kong) Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100µF, Tantalum	Richey-Cypress Elect. Tel: (408) 654-9100 Fax: (408) 566-0160	Warren Marshall Tel: (800) 421-7258 Fax: (714) 713-0129
Murata Electronics	GRM40X7R105J016	1µF, X7R	Sales Department Tel: (770) 436-1300 Fax: (770) 436-3030	Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721 Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (847) 803-6100 Fax: (847) 803-6296	Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090 Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108

Shorting Blocks

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Wesley Lin or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Molex	Micheal Gits Tel: (408) 946-4700 Fax: (408) 946-5386	(Molex) Tel: (49) 89-413092-0 Fax: (49) 89-401527	(Molex) Tel: (65) 268-6868 Fax: (65) 265-6044	(Molex) Tel: (81) 427-21-5539 Fax: (81) 427-21-5562

Resistors

Vendor	Size	Type	Accuracy/ Value	Contact
Thin Film Technology	1208	thin	0.1%, 100-250KΩ 0.5%, 10-250KΩ	(507) 625-8445 Region Sales Mgrs
	0805	thin	0.1%, 100-100KΩ 0.5%, 10-1MΩ	Patrick Lyons x14 W. of Mississippi (except TX & S. Cal)
	0803	thin	0.1%, 100-33KΩ 0.5%, 10-330KΩ	Mark Porisch x12 Southern US, E. of Mississippi (inc. TX)
	0402	thin	0.5%, 10-100KΩ	Tim Goertzen x13 Northern U.S., E. of Mississippi & Canada Mike Smith (310) 768-8923 Southern California
Dale Electronics	0603	thin	0.5%, 10-100KΩ	Gary Bruns (402) 371-0080
		thick	1%,2%, 10-1MΩ	
	805	thin	0.1%, 100-100KΩ	
Koa Spear	805	thin	0.1%, 100-100KΩ	T. Yogi (814) 362-5536
		thick	0.5-5%, 10-1MΩ	
Beckman Industrial	0805	thin	0.1%, 10K-100KΩ	Cathy Whittaker (214) 392-7616
		thick	1-5%, 10-1MW	
	0603	thick	1-5%, 10-1MW	

3.3V Clock Driver Suppliers

Supplier	Contact	Phone	Fax
ICS	Raju Shah	408-925-9493	408-925-9460
ICW	Angel Atondo	408-922-0202 ext 1131	408-922-0833
National Semiconductor	John Bergen	408-721-2990	408-732-6017
Cypress Semiconductor	John Wunner	206-821-9202 ext 325	206-820-8959
Texas Instruments	David Hoover	903-868-5694	903-868-5962
IDT	Mark Hermsen	408-492-8366	408-492-8362
AMCC	Mark Denzin	619-535-6526	619-450-9885
Motorola	Geraldine Stih	602-952-3046	602-952-3682
Triquint Semiconductor	George Sanders	503-644-3535	503-644-3198
IMI	Elie Ayache	408-263-6300	408-263-6571

APPENDIX E

E1.0. LIST OF RELATED TOOLS & COLLATERAL

E1.1. Public Documentation

These documents may be ordered from the Intel Literature Center by calling 800-548-4725 in the U.S. In other geographies please contact your local sales office.

Document Title	Order Number
Pentium® Processor Family Developer's Manual (3 Volume Set)	241563
- Volume 1: Pentium Processors (Databook)	241428
- Volume 2: 82496/82497/82498 Cache Controller and 82491/82492/82493 Cache SRAM (Databook	241429
- Volume 3: Architecture and Programming Manua	241430
Pentium® Processor Datasheet (75 MHz, 90 MHz, 100 MHz, 120 MHz, 133 MHz, 150 MHz, 166 MHz and 200 MHz)	241997
Pentium® Processor Specification Update	242480
Pentium® Processor Family Product Briefs	241561
Pentium® Processor Performance Brief	241557
Pentium® Processor Technical Overview	241610
AP-479: Pentium® Processor Clock Design	241574
AP-480: Pentium® Processor Thermal Design Guidelines	241575
AP-485: Intel Processor Identification with the CPUID Instruction	241618
AP-577: An Introduction to PPGA Packaging	243103
AP-522: Implementation Guidelines for 3.3V Pentiun® Processors with VRE Specifications	242687
AP-578: Software and Hardware Considerations in Handling FPU Exceptions	242415
Pentium® Processor 3.3V Clock Driver Specifications	Contact your local Intel Sales Office or Distributor
Pentium® Processor 3.3V ASIC Interface Specification	Contact your local Intel Sales Office or Distributor
Pentium® Processor 3.3V Pipeline BSRAM Specification	Contact your local Intel Sales Office or Distributor

E1.2. Collateral Available Under Non-Disclosure Agreement

These documents may be obtained by contacting your local Intel sales office or distributor.

Product Information

Document Title	Notes ID/PDDC Document Number
Pentium® Processor Specification Update	FMKIHU
200 MHz P54CS-cC0 Stepping Information, Rev. 1.0	EW3Q1T
P55C BIOS Compatibility	CW1QGR
P55C External Design Specification (EDS), Rev. 3.1	SC-1294
P55C Platform Architecture Analysis, Rev. 3.0	SC-1263

System Design Documentation

Document Title	Notes ID/PDDC Document Number
Pentium® Processor Flexible Motherboard (FMB) Desigr Guidelines, Rev 2.0	RG4Y1L
P55C/FMB Design Review Checklist, Rev 3.0	MCLOOO
Socket 7 Specification, Rev. 3.0	FM-0632
Socket 7 Design Review Checklist, Rev. 2.0	PC89O9
Pentium® Processor Input Strapping Recommendations Rev. 2.0	MCQ3OW
P55C Voltage Regulator Module Overview and Targe Spec., Rev 4.0	FBKP54
Voltage Guidelines for Pentium® Processors with MMX™ Technology	KW1TFD

System Design Tools

Split-plane Platform Test Kit	Contact your local Intel Sales Office or Distributor

E2.0. REFERENCES

Clyde F. Coombs, Jr., *Printed Circuits Handbook*, McGraw Hill Publishing Co., New York, 1988

intel®

AP-577

APPLICATION NOTE

An Introduction to Plastic Pin Grid Array (PPGA) Packaging

June 1997

Order Number: 243103-004

AP-577

APPLICATION
NOTE

An Introduction to Plastic Pin Grid Array (PPGA) Packaging

June 1997

Order Number 243703-004

1.0. INTRODUCTION

As Intel microprocessors become faster, more complex and more powerful, the demand on high-performance packaging technology increases. For instance, higher clock rates imply faster internal signals, which may cause more switching noise. Thus packaging technology needs to tackle power supply decoupling issues. For each new generation of microprocessors, a greater number of transistors are packed onto each chip, generating more heat. The package thermal resistance becomes critical. Furthermore the shrinking die size causes higher power density, which tests the effectiveness of the package to dissipate the heat. The improvements in microprocessor speed and functionality drive the package design improvements in electrical, thermal and mechanical performance.

Over the years, Intel has introduced a variety of innovative package designs, such as surface mount, small outline, very thin package, and multilayer molded plastic quad flatpacks (PQFP). Keeping form, fit and function in mind, Intel continues to research and develop advanced packaging technology. The Pentium® microprocessor family has been available in either ceramic pin grid array (CPGA) package or tape carrier package (TCP) format to date. However as the core frequency of microprocessors steps up. Power dissipation will be increasing accordingly.

In 1993, Intel engineers began the development of plastic pin grid array (PPGA) packages to alleviate potential performance-limiting package problems. Compared to the existing CPGA package technology, the PPGA package has a better power distribution and improved thermal and electrical performance. Intel also ensures that the processors in PPGA and CPGA packages meet the same product specifications in Input/Output (I/O) timings, mechanical fit and quality and reliability.

Table 1 summarizes the key differences between the PPGA package and the CPGA package. The following sections will detail the physical structure, electrical modeling and performance of PPGA.

Table 1. Differences Between CPGA and PPGA Packages

Attribute	CPGA	PPGA
Physical		
Appearance	Tile, flat ceramic top	Circuit board, exposed pins
Package Body Material	Ceramic body, Al bond wires	BT laminate, Ni/Cu slug, encap, Au bondwires
Body Thickness	2.8 mm	3.0 mm (with heat slug)
Weight	29 gms	18 gms
Package Trace Metal	Tungsten	Copper
External Heat Slug	No	Yes
External Capacitors	No	Yes
Performance		
Thermal (θ_{jc}) with Heat Sink	1.25° C/W	0.50° C/W
Power Distribution	Good	Better
Package Trace Propagation Delay	Good	Better
Others		
Thermal Grease Used for Heat Sink Attachment	Electrically conductive or non-conductive	Electrically non-conductive
Thermal grease tranfer foil if used	flat, curved or cupped	flat only
Foil size if used	determined by the system manufacturers	equal or smaller than the heatslug
Board Mount	Socket or thru-hole insertion	Socket only
Shipping Tray	Blue color ,see Figure 6	Brown color, pocket size reduced
Caution: For PPGA packages, electrically conductive surfaces should not touch any part of the processo except the heatslug. For instance, an electrically conductive heat sink should not contact the exposed pins, th external capacitors or the exposed metal on the sides of the package		

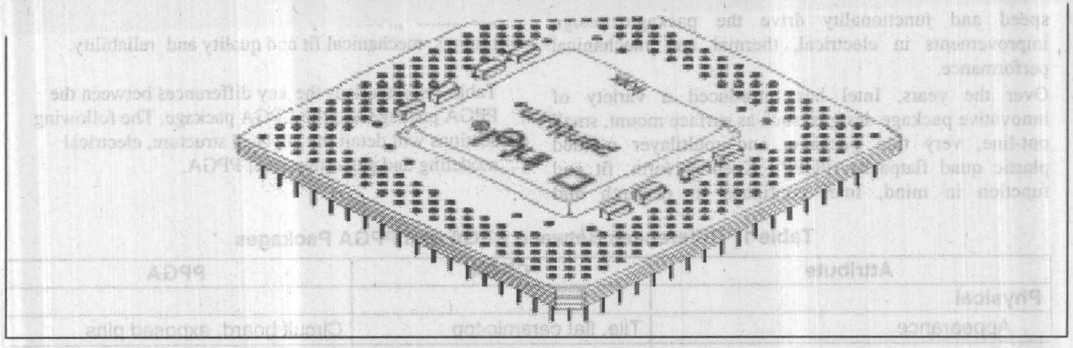


Figure 1. Top View of a PPGA Package

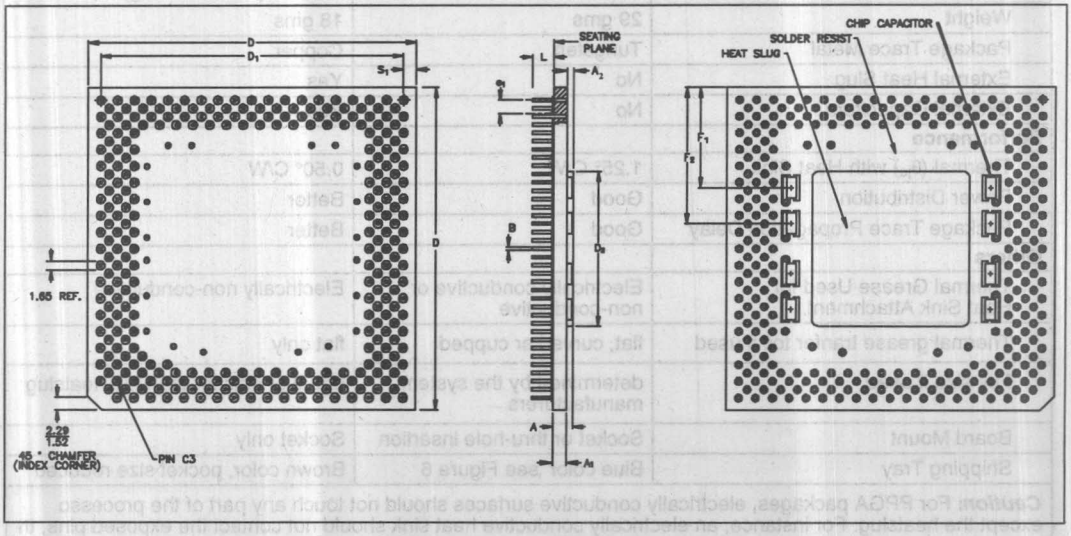


Figure 2. Plastic Pin Grid Array (PPGA) Package Dimensions

Table 2. Physical Dimensions of a 296-Pin Staggered PPGA Package

Family: Plastic Pin Grid Array Package				
Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	2.72	3.33	0.107	0.131
A1	1.83	2.23	0.072	0.088
A2	1.00		0.039	
B	0.40	0.51	0.016	0.020
D	49.43	49.63	1.946	1.954
D1	45.59	45.85	1.795	1.805
D2	23.44	23.95	0.923	0.943
e1	2.29	2.79	0.090	0.110
F1	17.56		0.692	
F2	23.04		0.907	
L	3.05	3.30	0.120	0.130
N	296		296	
S1	1.52	2.54	0.060	0.100

2.2. Physical Structure of a PPGA Package

The PPGA package body is a pinned laminated printed circuit board (PCB) structure. Figure 3 illustrates the cross section schematic[1]. The dielectric material, which is chosen for its high temperature stability and industry history, is a glass-reinforced high glass transition temperature (Tg) Bismaleimide Triazine (BT) with a Tg ranging from 170° C to 190° C. Conductors are copper traces. For bondability, the copper (Cu) bond fingers are plated with gold (Au) over nickel (Ni). The heat slug is Ni plated copper, which gives high thermal dissipation. The Kovar pins are plated with Au over Ni.

[1] The cross section is a schematic only. It does not depict the exact stackup model of the PPGA production units.

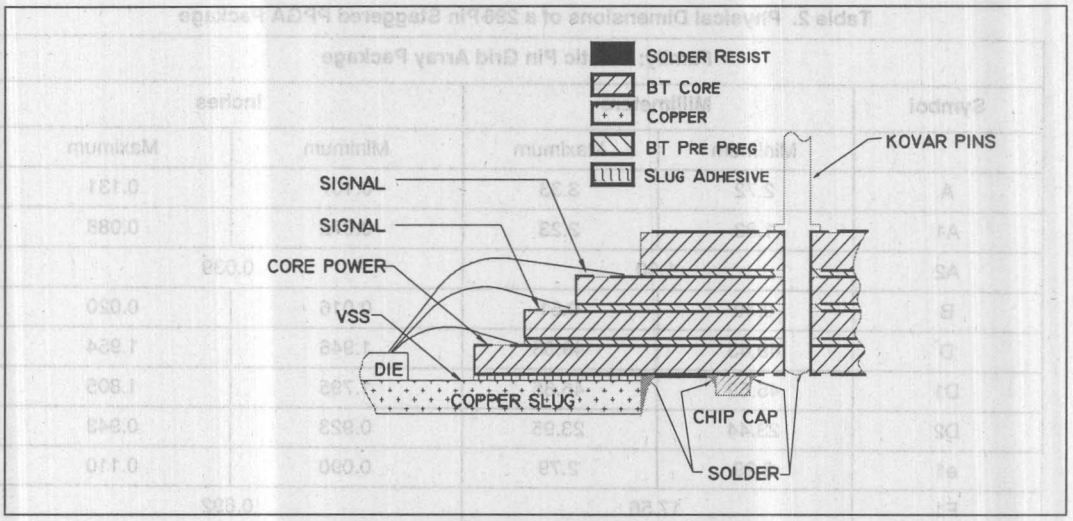


Figure 3. A PPGA Schematic Cross Section

In manufacturing the PPGA piece part, standard Printed Circuit Board (PCB) processing and equipment are used. Figure 4 lists the basic manufacturing and lamination process.

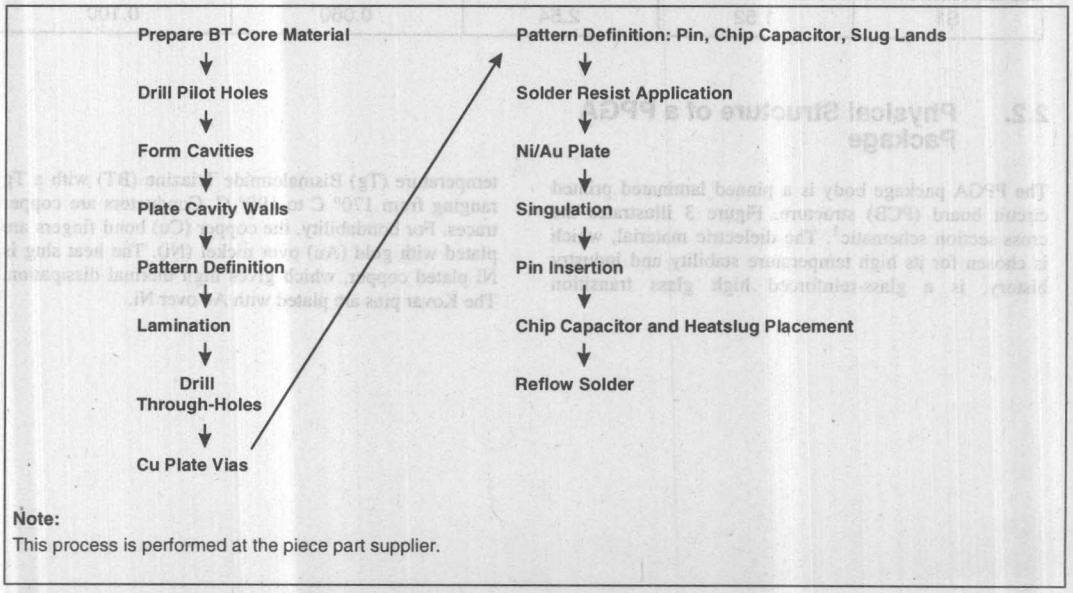


Figure 4. Piece Part Substrate Manufacturing and Lamination Process

Intel's PPGA component assembly process is very similar to CPGA in both equipment and process steps. This is summarized in Figure 5.

2.3. PPGA Package Shipping Media

PPGA shipping trays meet the JEDEC standards. All external dimensions of the PPGA tray are the same as the CPGA tray. For easy identification, the PPGA tray has a brown color while the CPGA tray is blue. In addition, to reduce package free-play, the PPGA tray has slightly smaller pocket dimensions. Refer to Figure 6 for the dimensions of the PPGA shipping tray.

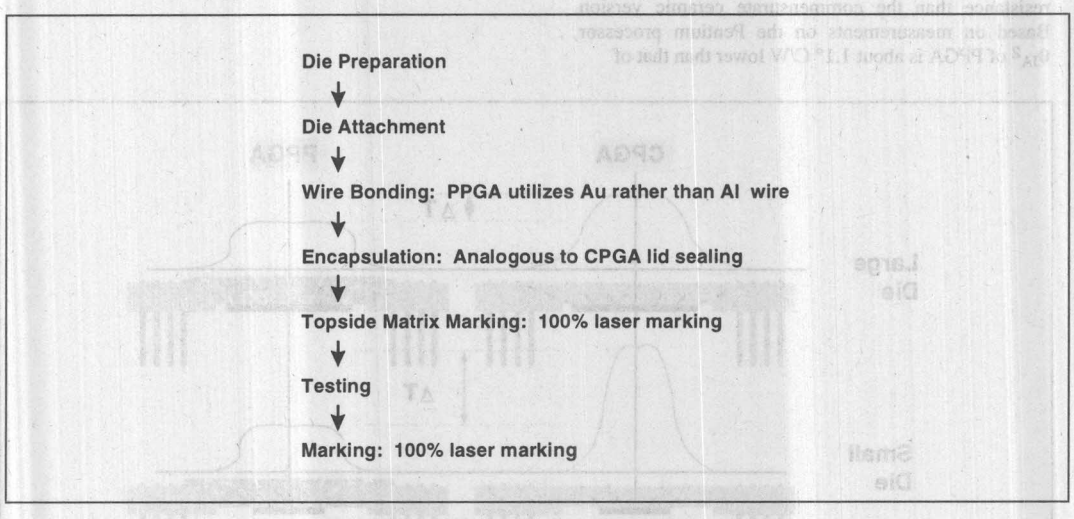


Figure 5. Intel PPGA Assembly Process

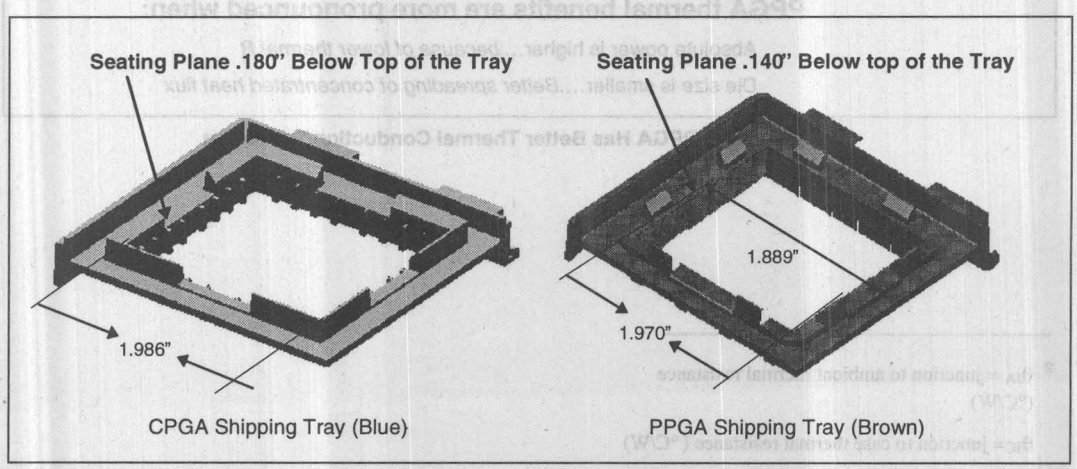


Figure 6. CPGA and PPGA Shipping Trays

3.0. PPGA PERFORMANCE CHARACTERISTICS

3.1. Thermal Characteristics

To improve the thermal performance, the PPGA package utilizes a heat slug with a high thermal conductivity. The die is attached directly to the nickel plated copper heat slug, resulting in a lower thermal resistance than the commensurate ceramic version. Based on measurements on the Pentium processor, θ_{JA}[2] of PPGA is about 1.1° C/W lower than that of CPGA. Appendix A details the thermal resistance values for the Pentium processor in ceramic pin grid array and plastic pin grid array packages. The benefit in thermal improvement for the PPGA package is more pronounced when the absolute power is higher and when the die size is smaller. In other words, the PPGA technology will be a preferable choice for the future generations of high power processors and systems. Figure 7 illustrates the thermal conduction and heat flux spreading of both CPGA and PPGA.

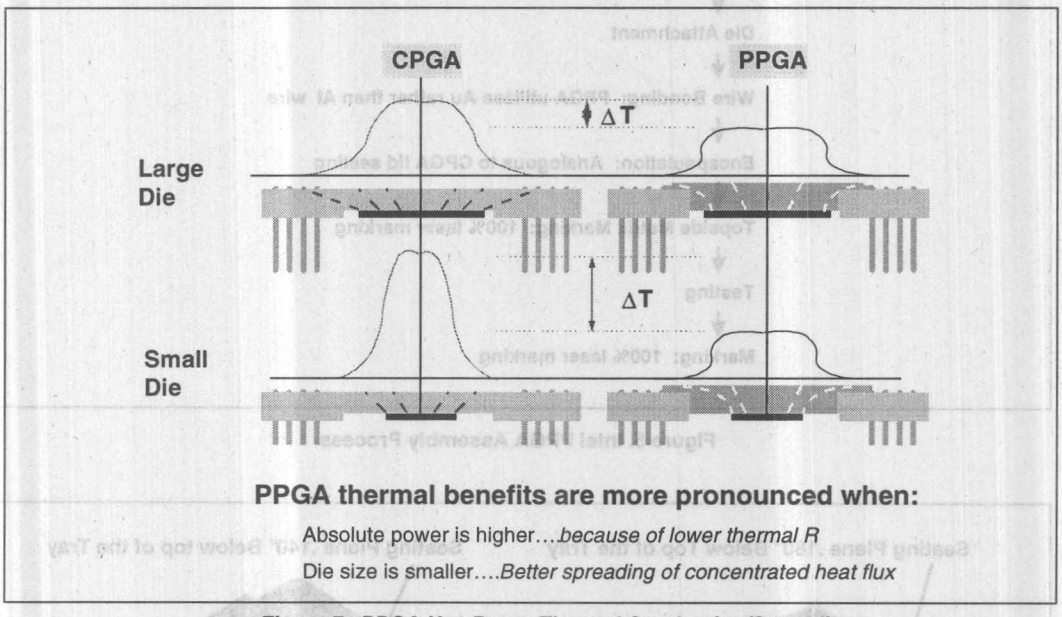


Figure 7. PPGA Has Better Thermal Conduction/Spreading

[2] θ_{JA} = junction to ambient thermal resistance (°C/W)

θ_{JC}= junction to case thermal resistance (°C/W)

θ_{CA} = case to ambient thermal resistance (°C/W)

3.2. Electrical Characteristics

3.2.1. I/O BUFFER

The package I/O model for Pentium processors in PPGA packages is shown in Figure 8 as a first order buffer model. R_O and C_O values are independent of the package and remain unchanged. Lp is the package inductance that includes bond wire inductance, trace inductance, pin inductance and socket inductance. C_P is the package capacitance consisting primarily of trace capacitance and socket capacitance. The parameter values are compiled in Table 3 and the buffer types for signals can be found in Table 4. The PPGA package input buffer model is the same as CPGA.

In this model, an effective inductance is used for the bond wire. Both self and mutual inductance are taken into account. The pin and its socket are considered as a single entity and a typical inductance value of 4.5 nH is used. A typical value of 1.0 pF is used for the socket capacitance.

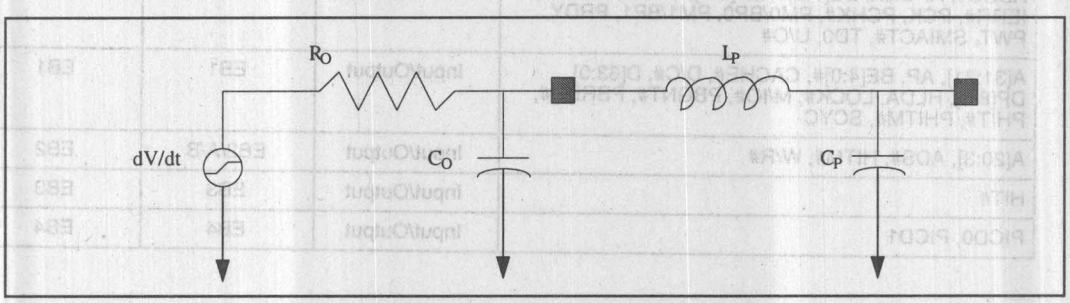


Figure 8. First Order I/O Buffer Model for PPGA

Table 3. Parameter Values for PPGA I/O Model (Pentium® Processor)

Buffer Type	Cp (pF)[1]		Lp (nH)[1]	
	min	max	min	max
ER0	3.41	3.41	9.64	9.64
ER1	3.25	5.98	9.3	11.94
ED1	3.37	5.0	9.09	14.99
EB1	3.2	5.48	9.18	15.98
EB2	3.36	5.06	9.54	14.7
EB2A	3.36	5.06	9.54	14.7
EB2B	3.36	5.06	9.54	14.7
EB3	4.72	4.72	13.24	13.24
EB4	3.7	4.03	10.57	10.7

Note:
[1] The values provided included typical socket capacitance and socket inductance.

ADSC#, APCHK, BE[7:5]#, BP[3:2], BREQ, FERR#, IERR#, PCK, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TD0, U/O#	Output	ED1	
A[31:21], AP, BE[4:0]#, CACHE#, D/C#, D[63:0] DP[8:0], HLDA, LOCK#, M/IO#, PBGNT#, PBREQ#, PHIT#, PHITM#, SCYC	Input/Output	EB1	EB1
A[20:3], ADS#, HITM#, W/R#	Input/Output	EB2/A/B	EB2
HIT#	Input/Output	EB3	EB3
PICD0, PICD1	Input/Output	EB4	EB4

3.2.2. SIGNAL QUALITY

Intel has performed noise measurements on the Pentium processors in both CPGA and PPGA packages. The results show that at the component level, the PPGA packages are comparable with the CPGA packages. In addition, the results indicate that all PPGA parts have a higher mean-core-power supply level than CPGA parts.

3.2.3. EMI

The Federal Communications Commission (FCC) has set limits on the maximum radiation from electrical systems. In turn, each component in a system should not exceed the typical level that is allocated to it. Electromagnetic Interference (EMI) levels from Intel's Pentium processors in ceramic pin grid array (CPGA) and PPGA packages have been measured with and without heat sinks attached. Measurements were performed up to a core clock frequency of 280 MHz. EMI levels are well below critical levels at all clock speeds tested. There is no significant EMI performance difference between CPGA and PPGA.

3.3. Mechanical Characteristics

3.3.1. MECHANICAL FIT

Note

Intel suggests that, when performing insertion and extraction, the maximum force should not exceed 100 lbs. For better manufacturing control, Intel also suggests that the force be placed on the pin matrix area uniformly, rather than on the heat slug. The insertion and extraction tooling should take into account the clearance for the external capacitors and the heat slug.

In order to ensure that PPGA packages are mechanically interchangeable with CPGA packages, Intel did extensive studies on mechanical fit, including insertion/extraction force, peak compressive force, clip force and heat sink attachment.

For the maximum insertion force measurement, the 296L PPGA packages were inserted at a rate of 1.27 mm/min (0.050 in/min). To understand the worst case scenario, the insertion force was applied uniformly on the entire heat slug surface of the package. A steel

plate was glued to the package using a room temperature cure adhesive. A stud was then attached to the plate to perform the extraction tests.

PPGA package insertion/extraction forces were measured with low insertion force (LIF) and zero insertion force (ZIF) sockets from different vendors. The socket insertion process involves applying an increasing amount of pressure on a package as it is inserted into the position in the socket. The applied load overcomes the frictional resistance applied to the package pins by the contact receptacles in the socket. If the socket receptacle structure is simple, the applied force increases smoothly as the package is inserted and the load-displacement curve is usually linear. When the package is completely inserted and any additional force will cause the package/socket assembly to bend together, the load-displacement curve will show a change in slope. The insertion force in this case is defined as the point where the load-displacement curve shows a final distinct change in slope.

To reduce the insertion force, some socket vendors stagger the placement of the pins in the socket body in the "Z" direction. The load-displacement curve in this case is no longer a simple linear curve. From the package integrity perspective, the maximum force seen by the package before complete insertion is critical. The maximum force, indicated by the point of final change in slope of the load-displacement curve is defined as insertion force. Table 5 summarizes the average measured insertion and extraction force with different sockets.

Components can be inserted into all socket types tested and still meet the suggested maximum loading of 100 lbs. Separate studies of package integrity have demonstrated that the PPGA package can sustain this level of applied normal compressive force plus margin.

The peak compressive force was uniformly distributed over the package heat slug while the PPGA unit rested on a PCB which contained a matrix of through-hole vias allowing for pin insertion. The rate at which the force was applied was 0.76 mm/minute (30 mils/minute). After the force was applied, each package was examined and no apparent physical changes were observed. Then each package was tested electrically and each package passed all electrical test parameters. Finally each package was inspected using Through Scan Acoustic Microscopy (TSAM) imaging. The result exhibited no significant changes and the cross section results confirmed that there was no delamination or internal package cracking .

3.3.2. HEAT SINK ATTACHMENT

3.3.2.1. Thermal Interface Material

CAUTION

Components on top (and exposed metal on the sides) of the PPGA packages can be shorted by any electrically conductive materials including heat sinks, thermal grease(if electrically conductive) and thermal grease foil carriers (if electrically conductive)

To ensure that PPGA packages are mechanically compatible with CPGA, Intel has performed a comprehensive evaluation of the effective method of heat sink attachment. Intel suggests that the interface material used for heat sink attachment should have the thermal conductivity greater than 0.8 W/mK, and should be electrically insulating. The volume resistivity of the material should be greater than 1×10^6 Ohm-cm. Intel has demonstrated that Thermalcote I* Conductacoat* with a flat aluminum foil carrier is an effective interface material for the Pentium® processor heat sink. Shaped or curved conductive foil carriers are not recommended with the PPGA package.

Table 5. PPGA Insertion/Extraction Force Measurement

Socket[1]	Average Insertion Force (lb.)	Average Extraction Force (lb.)
Preci-Con LIF	44.69	57.43
Mill-Max LIF	38.09	49.65
Robinson Nugent LIF	78.35	73.51
AMP LIF	65.06	69.91
Andon LIF	54.26	58.58
Yamaichi ZIFs	n/a	80.94[2]

Notes:

1 These data do not constitute a recommendation for any specific supplier or part number.

2 This is measured when the socket is in the "closed" position.

3.3.2.2. Clip Design and Attach

A minimum clip force of 5 lbs is recommended. Clips retain the heat sink assembly in the socket by exerting a force on the heat sink and the socket. The clip force, in turn, aids in forcing the grease to fill the many microscopic peaks and valleys on the heat sink and package surface, thereby reducing the interface thermal resistance. Since the quantity of grease squeezed out is different depending on the clip, the corresponding bond line thickness of the grease will affect thermal performance.

3.3.2.3. Thermal Test Results

296-pin PPGA packages were used as test vehicles. The assemblies of packages with a Thermalloy heat sink (0.87" tall) and a steel spring clip were tested inside a wind tunnel at a power setup of 10 W and an air flow rate of 300 LFM.

Test samples were subjected to the following stress test conditions: (1) 50 cycles of Temperature Cycle (T/C) from - 40 to 70° C; (2) 60 hours of aging at 150° C; (3) 120 hours of 92 percent humidity at 55° C. Junction to ambient thermal resistance (θ_{JA}) was measured before and after each stress. The failure criteria was defined as an increase of more than 1° C at 10 W in the junction temperature when measured after stressing. The results showed that there is no significant degradation of thermal performance for Thermalcote I Conductacoat after reliability stressing.

The effect of foil sizes, clip force and voiding on Thermalcote I Conductacoat* thermal performance was also explored. If there is an insufficient amout of grease on the Al foil, voiding will exist in the bond line. This results in higher θ_{ja} values. While up to 30% grease voiding can be tolerated without any impact on PPGA thermal performance, zero voiding is strongly recommended for any heat sink attachment methods.

A larger foil size will cover a larger area with grease, but a smaller foil size is preferred for handling. For instance, thermal resistance θ_{ja} measured with a 1.0" x 1.0" foil is 0.1 C/W to 0.2 C/W lower than θ_{ja} measured with a smaller foil (0.7" x 0.7"). In addition, if the foil dimensions exceed that of the heatslug, the risk of shorting the external capacitors will greatly increase. Note that the aluminum foil is a carrier specific for Thermalcote I Conductacoat* grease to aid volume manufacturing. OEMs should decide whether to use flat aluminum foils based on their particular heat sink attachment methods and assembly lines.

Clip force determines the thermal grease bond line thickness and directly impacts thermal performance. To determine the effect of clip force on thermal performance, θ_{JA} and θ_{CS}[3] values for the heat sink assemblies were measured at different clip forces. The actual clip forces of these modified clips were individually measured by using a Material Testing System (MTS) before the thermal resistance measurement. All clip forces were also verified by using MTS after the thermal resistance measurement. Figures 9 shows θ_{JA} and θ_{CS} values versus clip force, respectively. The result indicates that as long as clip

3 θ_{CS}= case to heatsink thermal resistance (°C/W)

force is higher than 5 lbs (corresponding to ~ 5 psi), there is no significant effect of clip force on PPGA thermal performance.

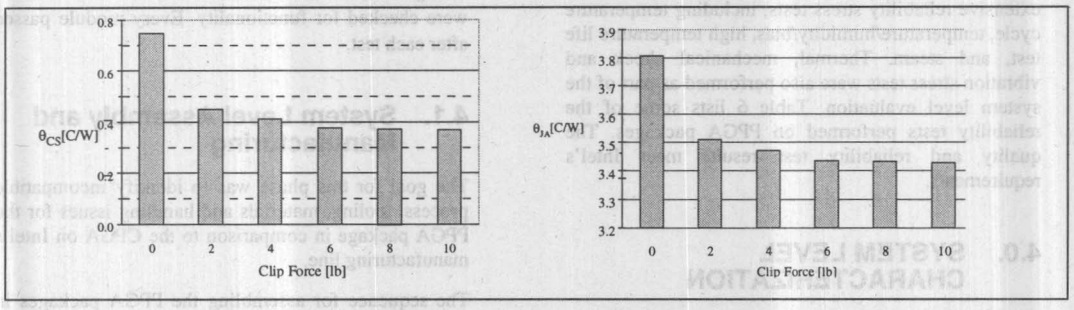


Figure 9. Comparison of θ_{CS} and θ_{JA} for Different Clip Forces

The new PPGA package may affect some existing heat sink designs. In one design, shown in Figure 10, the heat sink has a lip designed for CPGA Pentium processors to prevent movement of the heat sink relative to the package, socket and clip during mechanical shock tests. However, the new PPGA package has a heat slug, external capacitors, and exposed pins on the top side of the package. On the PPGA package, if the heat sink slips out of its secured position, the lip may touch the exposed pins. Therefore, the lip needs to be extended to a proper length to lock the heat sink in a secured position. Intel's evaluations indicate that a 50 mil lip is not adequate and that a 70 mil lip is needed to ensure reliable performance. Our tests also show that the 70 mil lip works well with CPGA packages. In addition, the side of the package has exposed metal that is electrically conductive. If the heat sink is electrically conductive, and the lip touches the side of the package, electrical shorting may occur, causing damage to the processor.

There may be other instances where heat sink designs need minor modifications to fit both the new PPGA package and the existing CPGA package. Customers need to work with their heat sink suppliers to ensure that their heat sink designs can accommodate both the PPGA and CPGA packages.

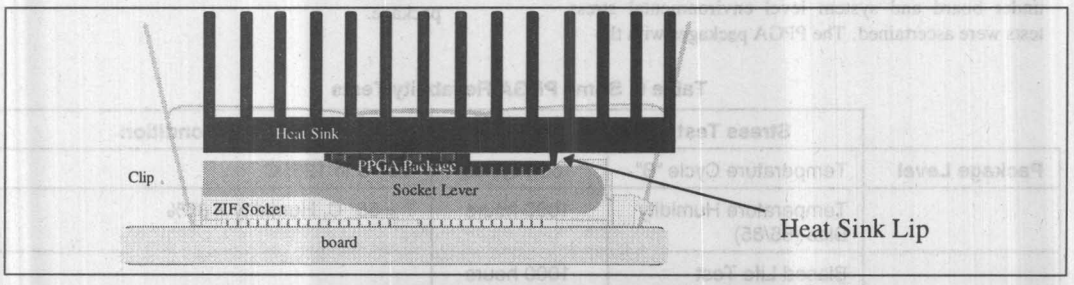


Figure 10. A Heat Sink Design With a Lip

3.4. Quality and Reliability

To ensure that the PPGA package continues to meet performance requirements over time, Intel performed extensive reliability stress tests, including temperature cycle, temperature/humidity/bias, high temperature life test, and steam. Thermal, mechanical shock and vibration stress tests were also performed as part of the system level evaluation. Table 6 lists some of the reliability tests performed on PPGA packages. The quality and reliability test results meet Intel's requirements.

4.0. SYSTEM LEVEL CHARACTERIZATION

The Plastic Pin Grid Array (PPGA) package was evaluated as a drop-in replacement for the Ceramic PGA package for present and future Intel board designs.

First, the impact of the PPGA package on board assembly was studied by assembling PPGA packages into sockets soldered on boards. These packages were split equally between LIF and ZIF sockets and the process steps included the application of thermal grease, and attachment of heat sinks and clips. No major issues were discovered during this evaluation. This indicates that introduction of the PPGA will cause no adverse impact on the manufacturing process flow for assembling boards.

Second, the PPGA package integrity and reliability under board and system level environmental stress tests were ascertained. The PPGA packages with the Pentium processors, assembled on a server CPU module, were subjected to thermal shock, vibration, mechanical shock, humidity, and temperature and voltage limits tests. After each test, the CPU modules were checked for functionality. Every module passed after each test.

4.1. System Level Assembly and Manufacturing

The goal for this phase was to identify incompatible process, tooling, materials and handling issues for the PPGA package in comparison to the CPGA on Intel's manufacturing line.

The sequence for assembling the PPGA packages in sockets soldered onto boards was:

- Visual inspection under 10X magnification
- Sockets were wave soldered on each dummy test board. Half of the sockets were ZIF sockets and the other half were 296-pin LIF sockets.
- Multiple boards were assembled with the sockets
- After wave soldering, the boards were delivered to the heat sink assembly area.
- PPGA components were inserted into the ZIF and LIF sockets per standard procedure. A lubricant is typically also sprayed on the socket to aid in this insertion process. ZIF socket insertions are done manually.
- Next, a grease foil was placed on top of the package.

Table 6. Some PPGA Reliability Tests

	Stress Test	Duration	Stress Condition
Package Level	Temperature Cycle "B"	1000 cycles	-55° C to 125° C
	Temperature Humidity Bias (85/85)	1000 hours	T = 85° C, Humidity = 85%
	Biased Life Test	1000 hours	
	Steam Stress	168 hours	T = 121° C, Pressure = 2 Atm
System Level	Thermal Shock		T = -40° C to +70° C
	Mechanical Shock		50 grams and averages 3 shakes per axis
	Vibration		Random frequencies between 20 Hz to 2000 Hz

- The heat sink was placed on the package, the heat sink clip was hooked on to the socket.
- After the assembly process was completed, the heat sink assemblies were disassembled, the PPGA packages were removed from the sockets and inspected under 10X magnification for damage.

The test results did not show any damage to any of the PPGA packages. The use of PPGA packages required no manufacturing process change.

Note:

Insertion tooling may need to be modified for the clearance due to the external capacitors on top of the package. No problem has been observed in the evaluation process related to foil misalignment on the heat slug causing shorts between the adjacent capacitors. Use manufacturing controls when stacking up the processor, thermal interface and the heat sink to avoid foil misplacement on the PPGA package heat slug.

4.2. Quality and Reliability

PPGA Packages with Pentium processor devices were the test vehicles for this evaluation. These PPGA packages were inserted into LIF sockets on typical server product type boards. These boards have one Pentium processor with an expandable cache. Table 7 details the environmental tests to which the boards were subjected.

After each of the stress tests described above, a functional test was performed to verify that the boards under test were functional. All the boards tested passed after every environmental stress test exposure and they were functional at the end of the entire test sequence. The PPGA packages passed the typical Intel board and system level environmental stress exposure tests.

Table 7. Environment Stress Exposure Evaluation

Thermal Shock Test (Non-operating)	-40° C to 70° C for 50 hours, at a rate of 15°C to 30° C /minute
Vibration Test	10 minutes per axis for all 3 axes. 5 Hz to 20 Hz at a rate of 0.01 g^2/Hz to 0.02 g^2/Hz 20 Hz to 200 Hz at a rate of 0.02 g^2/Hz
Mechanical Shock	Trapezoidal 50G, 11 msec at a velocity change of 170 inches/sec
Temperature/Voltage Corner Tests	0° C, +4.75 V, +11.4 V 0° C, +5.25 V, +12.6 V 55° C, +4.74 V, +11.4 V 55° C, +5.25 V, +12.6 V
Humidity Test	95% humidity at a temperature range from 21° C to 65° C for 240 hours

5.0. PERFORMANCE COMPARISON BETWEEN PPGA AND CPGA

5.1. Package Level Comparison

The PPGA package provides increased availability of high frequency microprocessors, and provides better system thermal margin. Moreover, as the die size continues to shrink, the concentrated heat flux becomes critical. Hence effective heat spreading will significantly improve the processor performance.

Figure 11 details the package trace for CPGA and PPGA. Because of the different metallization, the trace metal of the CPGA package being tungsten and that of the PPGA being copper, the resistance is lower in PPGA package, yielding lower IR drop. Therefore a higher core voltage is achieved when PPGA is used. Intel guarantees that the product I/O timing specifications will not change from one package type to another.

5.2. System Level Comparison

A 120 MHz Pentium processor in a CPGA package was compared to a 120 MHz Pentium processor in a PPGA package for its thermal effectiveness in a typical server chassis. The conditions under which these two packages were tested were identical. The heat sink and thermal interface compound used was also the same. The case temperatures of the packages were measured and recorded for comparison. The results show a 5° C to 6° C difference between the margin of the two packages, with the device in the PPGA package running cooler than that in the CPGA package. It can be concluded that the device in a PPGA package can be installed in any system that currently has the same device in a CPGA package.

6.0. CONCLUSION

The new PPGA package outperforms the CPGA package electrically and thermally. In addition to providing increased availability of high-performance microprocessors, it is compatible with CPGA board manufacturing processes and is board-level reliability compliant. The interchangeability ensures that the thermal design solutions for PPGA package are compatible with the existing CPGA thermal designs.

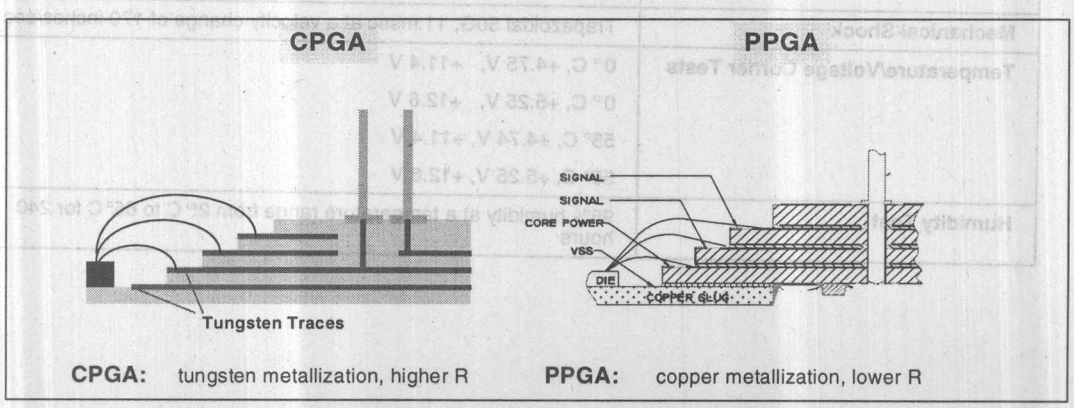


Figure 11. PPGA Has Lower Trace Resistance

APPENDIX A. THERMAL RESISTANCE VALUES FOR PENTIUM® PROCESSOR CB1 IN CPGA (WITHOUT HEAT SPREADER) AND IN PPGA

Table A-1: θ_{CA}[°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)

	θ_{CA}[°C/W] vs Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25"	9.4	8.3	6.9	4.7	3.9	3.3
0.35"	9.1	7.8	6.3	4.3	3.6	3.1
0.45"	8.7	7.3	5.6	3.9	3.2	2.8
0.55"	8.4	6.8	5.0	3.5	2.9	2.6
0.65"	8.0	6.3	4.6	3.3	2.7	2.4
0.80"	7.3	5.6	4.2	2.9	2.5	2.3
1.00"	6.6	4.9	3.9	2.9	2.4	2.1
1.20"	6.2	4.6	3.6	2.7	2.3	2.1
1.40"	5.7	4.2	3.3	2.5	2.2	2.0
1.50"	5.5	4.1	3.1	2.4	2.2	2.0
None	14.5	13.8	12.6	10.5	8.6	7.5

Note:
θ_{CA} is case to ambient thermal resistance. θ_{CA} values shown in this table are typical values. The actual $q\theta_{CA}$ values depends on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

Table A-2: θ_{JC}[°C/W] for a CPGA Package With and Without a Heat Sink

	No Heat Sink	With Heat Sink
Average θ_{JC}	1.7	1.25

Table A-3: θ_{JA}[°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)

	θ_{JA} °C/W] verses Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25"	10.6	9.5	8.1	5.9	5.1	4.5
0.35"	10.3	9.0	7.5	5.5	4.8	4.3
0.45"	9.9	8.5	6.8	5.1	4.4	4.0
0.55"	9.6	8.0	6.2	4.7	4.1	3.8
0.65"	9.2	7.5	5.8	4.5	3.9	3.6
0.80"	8.5	6.8	5.4	4.1	3.7	3.5
1.00"	7.8	6.1	5.1	4.1	3.6	3.3
1.20"	7.4	5.8	4.8	3.9	3.5	3.3
1.40"	6.9	5.4	4.5	3.7	3.4	3.2
1.50"	6.7	5.3	4.3	3.6	3.4	3.2
None	16.2	15.5	14.3	12.2	10.3	9.2

Table A-4: θ_{CA}[°C/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)

	θ_{CA}[°C/W] verses Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25"	9.0	7.9	6.5	4.3	3.5	2.9
0.35"	8.7	7.4	5.9	3.9	3.2	2.7
0.45"	8.3	6.9	5.2	3.5	2.8	2.4
0.55"	8.0	6.4	4.6	3.1	2.5	2.2
0.65"	7.6	5.9	4.2	2.9	2.3	2.0
0.80"	6.9	5.2	3.8	2.5	2.1	1.9
1.00"	6.2	4.5	3.5	2.5	2.0	1.7
1.20"	5.8	4.2	3.2	2.3	1.9	1.7
1.40"	5.3	3.8	2.9	2.1	1.8	1.6
1.50"	5.1	3.7	2.7	2.0	1.8	1.6
None	13.0	12.3	11.4	8.0	6.6	5.7

Note:

θ_{CA} is case to ambient thermal resistance. θ_{CA} values shown in this table are typical values. The actual θ_{CA} values depends on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

Table A-5: θ_{JC}[°C/W] for a PPGA Package With and Without a Heat Sink

	No Heat Sink	With Heat Sink
Average θ_{JC}	1.3	0.50

Table A-6: θ_{JA}[°C/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)

	θ_{JA}[°C/W] verses Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25"	9.5	8.4	7.0	4.8	4.0	3.4
0.35"	9.2	7.9	6.4	4.4	3.7	3.2
0.45"	8.8	7.4	5.7	4.0	3.3	2.9
0.55"	8.5	6.9	5.1	3.6	3.0	2.7
0.65"	8.1	6.4	4.7	3.4	2.8	2.5
0.80"	7.4	5.7	4.3	3.0	2.6	2.4
1.00"	6.7	5.0	4.0	3.0	2.5	2.2
1.20"	6.3	4.7	3.7	2.8	2.4	2.2
1.40"	5.8	4.3	3.4	2.6	2.3	2.1
1.50"	5.6	4.2	3.2	2.5	2.3	2.1
None	14.3	13.6	12.7	9.3	7.9	7.0

APPENDIX B. FREQUENTLY ASKED QUESTIONS

1. Does Intel have any plans to cover the exposed circuitry on the slug side of the PPGA package?

Intel has no plans to pursue protective coatings on top of the current organic package. Exposed circuitry is not new to the component or PC board industries. World-class manufacturing techniques will ensure that shorting/damage does not occur.

2. What are the concerns in attaching a heat sink clip to the package rather than the socket?

Repeated installation/removal of the clip can cause damage to the package edge as it is PC board material rather than ceramic. Additionally, our tests indicate that if the combined mass of package and heat sink is greater than ~135 grams, the assembly can vibrate out of certain type 5 or 7 ZIF sockets during shock and vibration testing. If heat sink attach to the package is going to be used, the customer should evaluate the assembly fully for these types of issues. The majority of Intel data was taken attaching the heat sink clip to the socket.

3. Does Intel plan to add either product or S-spec marking to the heat slug?

Intel has no current plans to change the marking on the PPGA. The product speed code is marked on the heat slug.

4. Is Intel considering changing the color of the PPGA shipping tray to make it more distinguishable from the CPGA tray to distinguish product/speed?

The production version of the PPGA shipping tray is brown in color to distinguish it from the CPGA tray (blue). No other changes were made to the original PPGA tray. Production units will be shipped in the brown tray.

5. Is Intel considering an 85° C T_{CASE} rating for this package?

PPGA thermal efficiency is a factor in enabling Intel to offer higher performance processors. We have no plans to increase T_{CASE} at the expense of performance.

6. In view of the PPGA package's superior thermal and electrical properties, will the same product in CPGA be interchangeable with PPGA?

Intel guarantees that all Pentium processors in the PPGA package meet the same AC/DC specifications as those in the CPGA package.

7. Will protective shipping bags be used to prevent foreign material accumulation during shipping or storage?

The PPGA package will be shipped in the same manner as the CPGA package. The shipping box itself offers protection from foreign material.

8. What is the maximum heat sink clip force that can be applied?

100 lbs is the maximum force. Experiments have shown that 5 lbs is sufficient to achieve optimum thermal transfer between the package slug and heats sink when thermal grease is used. Due to the slight package thickness increase when compared to the CPGA package, clip force will increase by approximately 5 percent when applying CPGA clips to the PPGA package. Before applying a CPGA heat sink, be sure to verify that it has proper clearance and will fit the PPGA package.

9. Is Intel planning to provide a video or other training on how to handle this package in a manufacturing environment?

We have no plans to offer any specialized training.

10. What is the total capacitance of the CPGA package and how does it compare to PPGA total capacitance?

The CPGA package capacitance is 14 nfds. The goal in design was to match effective series inductance between the packages rather than capacitance. Due to the capacitor layout, termination differences, and relative locations in relation to the die, the CPGA package requires considerably less total capacitance than the PPGA package's 120 nfds.

11. What are the flammability ratings for the encap and BT material used in the package?

The PPGA package passes the " Needle Flame Test" per IES 695-2-2. The samples do not support flaming time nor do they have any flaming particles. The Oxygen Index Test has been conducted. 24 percent oxygen is the minimum concentration that will support flaming. Copies of the UL reports are available.

(insertion pressure will be applied to the slug rather than the pin matrix area)?

We expect no issues if force is applied uniformly and parallel to the plane of the package to ensure no heat sink tilt occurs and total force is kept below 100 lbs.

14. Can Intel supply its thermal modeling data or thermal test chips so customers can run their own simulations?

We can supply modeling data as to the effect of airflow LFM on heat sink size. This should be requested from your Field Applications Engineer (FAE).

15. Will Intel provide data on additional thermal interface materials?

Intel evaluated TC-208 and chose not to use it as it did not meet our manufacturing process dry out requirements. Our application note, *An Introduction to Plastic Pin Grid Array (PPGA) Packaging*, (Order Number 243103-001) references Thermalcote I. Other materials may have similar performance but we have no plans to provide data on any other materials.

18. Does Intel have any plans to cover the sides of the PPGA package, which has exposed metal and is electrically conductive?

Intel has no plans to pursue protective coatings on the side of the current organic package. World class manufacturing techniques will ensure that shorting/damage does not occur. Please refer to this application note for recommendation of implementation.

APPENDIX C. HEAT SINK/FANSINK AND SOCKET SUPPLIERS

Heat Sink/ Fansink Suppliers	Address of Suppliers	Contact	Phone	Fax
Aavid	One Kool Path P.O.Box 400 Laconia, NH 03247	Gary Kuzmin	(603) 528-3400	(603) 528-1478
Des Tech	No.463, Kang Ning St Hsi Chih Chen, Taipei 22121, Taiwar	Jason Hsu	886-6-695-0462	886-2-695-0462
Evox Rifa	300 Tri-State Internationa Suite 375 Lincolnshire, IL 60069	Andrews Bellavia	(847) 948-9511	(847) 948-9320
Global Win Technology	IF, No. 366, Tanan Rd. Shih Lin, Taipei, Taiwar	Andy Lin	886-2-891-7388	886-2-881-7219
IERC	135 W. Magnolia Blvd. Burbank, CA 91502	Guy Addis	(818) 842-7277	(818) 848-8872
Johnson Matthey	15128 East Euclid Ave. Spokane, WA 99216	Brent Bollong	(509) 922-8702	N/A
Megaland Inc.	4962 El Camino Real Suite #109 Los Altos, CA 94022	Wayne Clement	(415) 967-2800	(415) 967-2878
Sanyo-Denki (Keymarc)	1-15 Kita Ohtsuka Toshima, Tokyo 170, Japan	James Sia	(310) 787-6825	813-3-917-4521
Thermalloy	2021 W. Valley View Lane Dallas, TX 75234	Larry Tucker	(214) 243-4321	(214) 241-4656
Chip Coolers*, Inc.	333 Strawberry Field Rd. Warwick, RI 02886	William B. Rife	(800) 227-0254	(401) 732-6119
EG&G Wakefield Engineering	60 Audubon Rd. Wakefield, MA 01880	David Saums	(617) 245-5900	(617) 246-0874

Socket Suppliers	Address of Suppliers	Contact	Phone	Fax
AMP	19200 Stevens Creek Blvd. Cupertino, CA 95014	Berny Kulwin	(408) 725-4984	(408) 725-4997
Andon	4 Court Drive Lincoln, RI 02865	John Tate	(410) 333-0388	(410) 333-0287
Bergquist	5300 Edina Industrial Blvd. Edina, MN 55435	Kevin Hanson	(612) 835-9096 x172	(612) 835-4156
Burndy	51 Richards Ave., P.O.Box5200, Norwalk, CT 06856	Ed Hrvatin	(203) 852-8553	(203) 852-8556
Loranger	3000 Scott Blvd. Santa Clara, CA 95050	Whitney Sharp	(408) 727-4234	(408) 727-5842
Mill Max	190 Pine Hollow Rd. Oyster Bay, NY 11771	Roger Sutcliffe	(516) 922-6000 x209	(516) 922-0023

Socket Suppliers	Address of Suppliers	Contact	Phone	Fax
AMP	18200 Stevens Creek Blvd. Cupertino, CA 95014	Barry Kulwin	(408) 725-4884	(408) 725-4897
Andon	4 Court Drive Lincoln, RI 02865	John Tate	(410) 393-0888	(410) 393-0287
Bergquist	8300 Edina Industrial Blvd. Edina, MN 55435	Kevin Hanson	(612) 835-9098 X172	(612) 835-4156
Burndy	51 Richards Ave. P.O.Box8200 Norwalk, CT 06856	Ed Hrvatin	(203) 852-8553	(203) 852-8556
Lotsinger	3000 Scott Blvd. Santa Clara, CA 95050	Whitney Sharp	(408) 727-1234	(408) 727-5382
Mill Max	190 Pins Hollow Rd. Oyster Bay, NY 11771	Roger Sutcliffe	(516) 922-6000 X209	(516) 922-6023

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AP-522

APPLICATION NOTE

Implementation Guidelines for 3.3V Pentium® Processors with VRE Specifications

for Desktop and Server Designs

June 1997

Order Number: 242687-003

intel

AP-522

APPLICATION
NOTE

Implementation Guidelines for 3.3V Pentium® Processors with VRE Specifications

for Desktop and Server Designs

June 1997

Order Number: 243827-003

1.0. INTRODUCTION

In addition to standard 3.3V Pentium® processors, Intel is offering 3.3V Pentium processors with VRE specifications to enable quicker time-to-market cycles, and higher-performance desktop and server systems. **This document will explain the voltage specifications, recommend solutions for supplying consistent power, and suggest validation techniques to ensure robust 3.3V Pentium processor-based desktop or server systems.** VRE (Voltage Regulated Extension) components have stricter supply voltage specifications than standard components, and as such VRE-based designs bring additional challenges to power regulation. Although this document focuses on VRE designs, the system design and voltage measurement concepts also apply to designs for standard components.

This document contains five key sections:

Chapter 2.0 discusses the standard and VRE specifications. The VRE and standard voltage ranges have been adjusted for the C2-step and all subsequent processors. These changes are reflected in the chapter (and the entire document). Chapter 2.0 also gives an overview of some important system design and voltage measurement considerations associated with VRE components. The consequences of specification violations are also discussed.

Chapter 3.0 deals with the power supply and regulation. It contains power implementation recommendations to ensure a robust system design. In addition, this chapter contains detailed low cost bulk and high speed decoupling recommendations for Socket 5, Socket 7, and standard 3.3V designs.

Chapter 4.0 explains the proper measurement techniques to verify that systems meet their respective voltage specifications. These measurement techniques apply to all Pentium processors. Measurement results from the *Pentium® Processor Flexible Motherboard Reference Design* are shown in this chapter.

Appendices A and B provide information about tools to assist in both simulating decoupling solutions, and in taking voltage measurements. Specifically, information is provided about obtaining SPICE* source files and simulation results. This section also contains information on how to obtain and use the recommended "stress" code for voltage noise measurement.

Finally, Appendix C provides a list of third party vendors. These vendors include suppliers of regulators, resistors, capacitors, and sockets.

2.0. SPECIFICATIONS

2.1. The VRE Specification

The only difference between the VRE, and standard 3.3V specifications are the voltage supply requirements. Since the VRE specification has a stricter V_{CC} requirement than the standard voltage specification, VRE-based systems are very sensitive to voltage supply noise and transients. **Any overshoot or undershoot beyond the voltage range (at a measurement bandwidth of 20MHz) is not permitted.** Any transient excursion beyond the specified voltage range may result in unstable system behavior. Note that socket type and measuring techniques are also specified and should be followed to ensure consistent and accurate measurements.

Complete S-Specs, and availability of the Pentium processor family may be found in the latest Pentium processor stepping information or *Pentium® Processor Specification Update* (Order Number 242480).

The complete specifications shown above must be met to ensure a robust VRE-based platform. All measurements must be made and guaranteed at the back of the motherboard at the CPU socket pins. The voltage specifications assume an oscilloscope measurement bandwidth of 20MHz. Socket 5 or Socket 7 (or an equivalent socket of less than 5nH) should be used to ensure upgradability to future Pentium OverDrive® processors and to ensure accurate transient measurements.

Note that standard voltage range encompasses the VRE range, hence standard parts will operate in VRE systems.

2.1.1. The VRE Supply Voltage Range

VRE components allow less transient tolerance than standard components. To compensate for the smaller transient tolerance, VRE-based platforms must use accurate voltage regulators and adequate local decoupling capacitors. During worst-case transient conditions (transition into and out of Stop Grant Mode or Halt Power Down Mode), current supplied to the processor can change by several amperes in tens of nanoseconds (Appendix B provides information about obtaining simulation models for accurately determining

2.2. Typical Application Behavior

Poorly designed desktop and server systems will violate VRE specifications during normal operation. An unusual application instruction mix can cause large current spikes from clock cycle to clock cycle. Figure 2 shows the rapid fluctuations of system power during execution of a BAPCo93* benchmark trace (BAPCo93 is a system benchmark used for measuring system performance). These quick transitions in current occur in a shorter time frame than that in which the power supply unit or voltage regulator may be able to respond.

Worst-case transients occur during power management. Figure 3 shows an oscilloscope trace of a system leaving the low-power Stop Grant State (via a deassertion of STPCLK#). The supply voltage "droops" due to ESL and ESR effects (see section 3.4), and because the voltage regulator cannot respond quickly enough to the large, instantaneous change in current. Droops and surges also occur in systems with proper decoupling, but to a lesser extent. The system also has high frequency noise due to high operation speed of the internal core.

2.3. Voltage Specification Violations

Overshooting the voltage specification can cause certain signals to violate their Minimum Valid Delay timing specifications. This timing violation will in turn lead to a failure in the system. Excessive and sustained overshooting can also cause hot electron related effects which can compromise the reliability of the part.

Undershooting causes a reduction in the performance of the component, and may also lead to timing related failures. The processor will not function properly at its correct clock frequency. The effects of undershooting are aggravated by improper cooling mechanisms.

Extensive die probing experiments show that high frequency overshooting and undershooting of the voltage specification are filtered by the processor's package parasitics, and are accounted for during the testing of the processor. As a result, the recommended oscilloscope measurement bandwidth has been adjusted to 20MHz (see section 4.2 for details).

Table 1. Comparison of Standard Specifications to VRE Specifications

Specifications	Standard	VRE
V_{CC}	**3.135V[1] to 3.6V** No overshoot or undershoot allowed	**3.4V[2] to 3.6V** No overshoot or undershoot allowed
Timings	Standard and MD	MD only
Thermals	Same Maximum I_{CC} and Maximum Power Dissipation	
Socket	Pentium OverDrive® Processor Upgrade Socket 5 or Socket 7	
Measurement	Transients must be measured and guaranteed at the back of the motherboard at the CPU socket pins. The measurement should be taken with a bandwidth of at least 20MHz (see section 4.2)	

[1]Applies to the C2 stepping, and all subsequent Pentium processors.

[2]Applies to the C2 stepping, and all subsequent Pentium processors with the VRE specification.

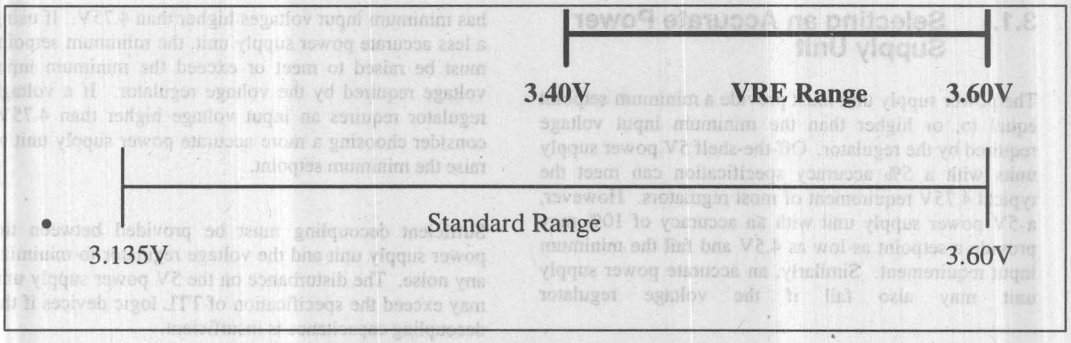


Figure 1. A Comparison of Standard and VRE Specifications

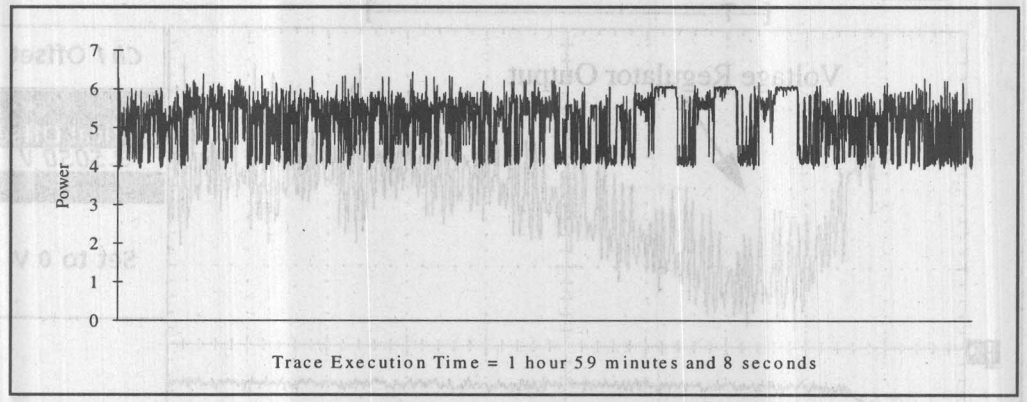


Figure 2. Rapid Fluctuations of System Power While During Active Operation (BAPCo93)

3.0. THE POWER SUPPLY

Until traditional power supply units with 3.3V DC outputs are widely available, supplying power to the 3.3V Pentium processor requires a 5V-to-3.3V voltage regulator. In addition, robust local decoupling must be provided to accommodate the transition to and from low-power modes. It is important to select the components to be as accurate as possible. A platform based on an inaccurate power supply unit must be compensated with a more accurate regulator and extra local decoupling. Similarly, a platform based on an inaccurate regulator requires accurate supporting components and additional decoupling capacitors. As shown next, selecting accurate components will maximize the voltage transient allowed.

VRE Specifications =	Σ Voltage Regulator Accuracy	
		+ Support Component Accuracy
		+ Thermal Drift and Aging Effects
		+ **Measured Voltage Transient**

The VRE specification allows a total voltage budget of 200mV. It is important to understand the voltage budget must include any deviation in the voltage regulator, the inaccuracy of its supporting components, and other non-ideal behavior of real components. When designing for a VRE-based platform, these DC factors must be subtracted from the total VRE budget. The remaining allowance should be targeted when measuring the voltage transient. It is hence important to select accurate voltage regulators and precise support components to allow maximum voltage transients.

3.1. Selecting an Accurate Power Supply Unit

The power supply unit must provide a minimum setpoint equal to, or higher than the minimum input voltage required by the regulator. Off-the-shelf 5V power supply units with a 5% accuracy specification can meet the typical 4.75V requirement of most regulators. However, a 5V power supply unit with an accuracy of 10% may provide a setpoint as low as 4.5V and fail the minimum input requirement. Similarly, an accurate power supply unit may also fail if the voltage regulator has minimum input voltages higher than 4.75V. If using a less accurate power supply unit, the minimum setpoint must be raised to meet or exceed the minimum input voltage required by the voltage regulator. If a voltage regulator requires an input voltage higher than 4.75V, consider choosing a more accurate power supply unit to raise the minimum setpoint.

Sufficient decoupling must be provided between the power supply unit and the voltage regulator to minimize any noise. The disturbance on the 5V power supply unit may exceed the specification of TTL logic devices if the decoupling capacitance is insufficient.

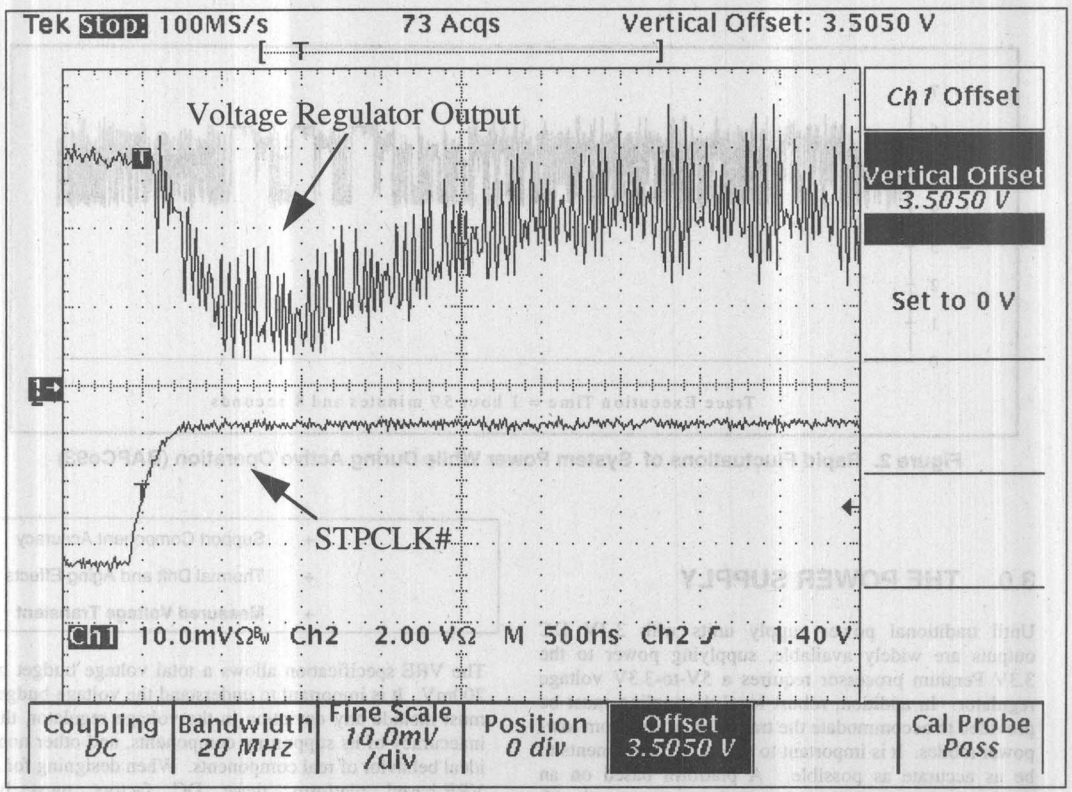


Figure 3. Voltage "Droop" when Exiting Stop Grant State

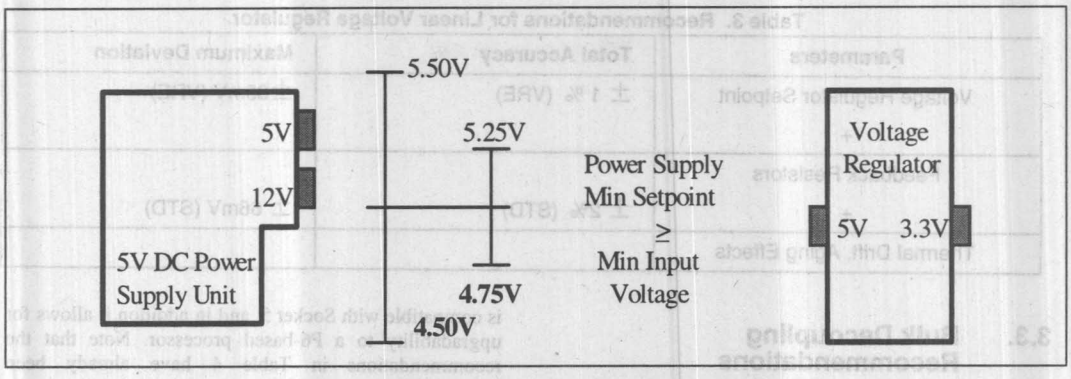


Figure 4. Setpoint Requirement of Power Supply

3.2. Selecting an Accurate Voltage Regulator

There are two types of voltage regulators: switching and linear. Switching regulators provide power by pulsing the voltages and currents to the load, thus resulting in lower heat dissipation and higher efficiency. Switching regulators are however generally more expensive and require more supporting components than linear regulators. Linear regulators essentially are voltage dividers and provide power by "dividing down" the 5V inputs to 3.3V outputs. Linear regulators dissipate more power, but are less expensive and typically require only two additional (feedback) resistors. Unless the system has strict thermal requirements, linear regulators generally are suited for high-volume designs. Both types of regulators can meet the VRE voltage range if they have accurate outputs and precise supporting components. Table 2 below compares the two types of voltage regulators:

An inaccurate regulator leaves little room for transient tolerance. For example, VRE specifications allow a voltage regulator solution to deviate only two percent (3.4V to 3.6V) from the desired regulator setpoint of 3.5V. Static specifications such as line regulation, temperature drift, and the initial setpoint must be held to 1% if any transient is to be permitted at all. Table 3 recommends the voltage regulator module accuracy required to ensure a robust VRE-based platform.

There are direct tradeoffs between the accuracy of the regulator and the amount of local decoupling. Using an inaccurate regulator requires more accurate dividing resistors and more decoupling. Conversely, using high-ESR, quick-aging capacitors necessitates accurate regulators. The next section recommends the bulk and high-speed decoupling required to ensure a robust VRE-based platform. The recommendations were based on extensive simulations and empirical measurements.

Table 2. Comparison of Voltage Regulators

Characteristics (Typical)	Linear Regulator	Switching Regulator
Maximum Efficiency	67%	95%
Maximum Power Dissipation	33%	5%
Supporting Components	2 to 6 (feedback resistors)	5 to 12 (feedback resistors, MOSFET switches, inductor, diode, caps)
Approximate Total Cost	Moderate	Moderately High

Table 3. Recommendations for Linear Voltage Regulator

Parameters	Total Accuracy	Maximum Deviation
Voltage Regulator Setpoint +	± 1 % (VRE)	±35mV (VRE)
Feedback Resistors +	± 2% (STD)	± 66mV (STD)
Thermal Drift, Aging Effects		

3.3. Bulk Decoupling Recommendations

The Pentium processor can be shut down and restarted very quickly with either the STPCLK# signal, or the HALT instruction. Switching the supply current on and off in very short time may cause serious power supply surges and droops in systems with inadequate bulk decoupling. Adequate bulk decoupling capacitors, located between the power and ground planes, near the processor, are necessary to filter these surges and droops. Adequate bulk capacitance is necessary to provide a current reservoir until the regulator can respond to the new load. It is important to use tantalum capacitors to minimize any aging effect. Electrolytic capacitors age faster, are inaccurate and are not stable over a wider temperature range. Capacitors with long leads add inductance and increase transients. Figure 5 shows the bulk decoupling required and a layout example to ensure the effectiveness of bulk decoupling.

Table 4 shows the decoupling recommendations for Socket 5, Socket 7 and standard 3.3V designs. Socket 7 is compatible with Socket 5, and in addition it allows for upgradability to a P6-based processor. Note that the recommendations in Table 4 have already been optimized for cost efficiency.

3.4. High Speed Decoupling Recommendations

Due to its high speed core activity, the Pentium processor generates high frequency noise components and higher current spikes in the power supply. High frequency capacitors between the power and ground planes and near the processor, are required to filter these high frequency noise components. Since the inductive effects of circuit board traces and component leads become more critical at higher frequencies, it is critical to place high frequency capacitors as near as possible to the processor, using short traces to minimize inductance. Surface mount capacitors should be placed inside and around the socket cavity as shown in Figure 6.

The reccomendations shown in Table 4 and Table 5

Table 4. Bulk Decoupling Recommendations for 3.3V Platforms

Design	Qty	Value	Type	Maximum ESR	Maximum ESL
Socket 5	4	100 µF	Tantalum	25 mΩ (100 mΩ/cap)	0.68 nH (2.7 nH/cap)
Socket 7	4	100 µF	Tantalum	25 mΩ (100 mΩ/cap)	0.68 nH (2.7 nH/cap)
Standard (low cost, non -VRE)	4	100 µF	Tantalum	25 mΩ (100 mΩ/cap)	0.68 nH (2.7 nH/cap)

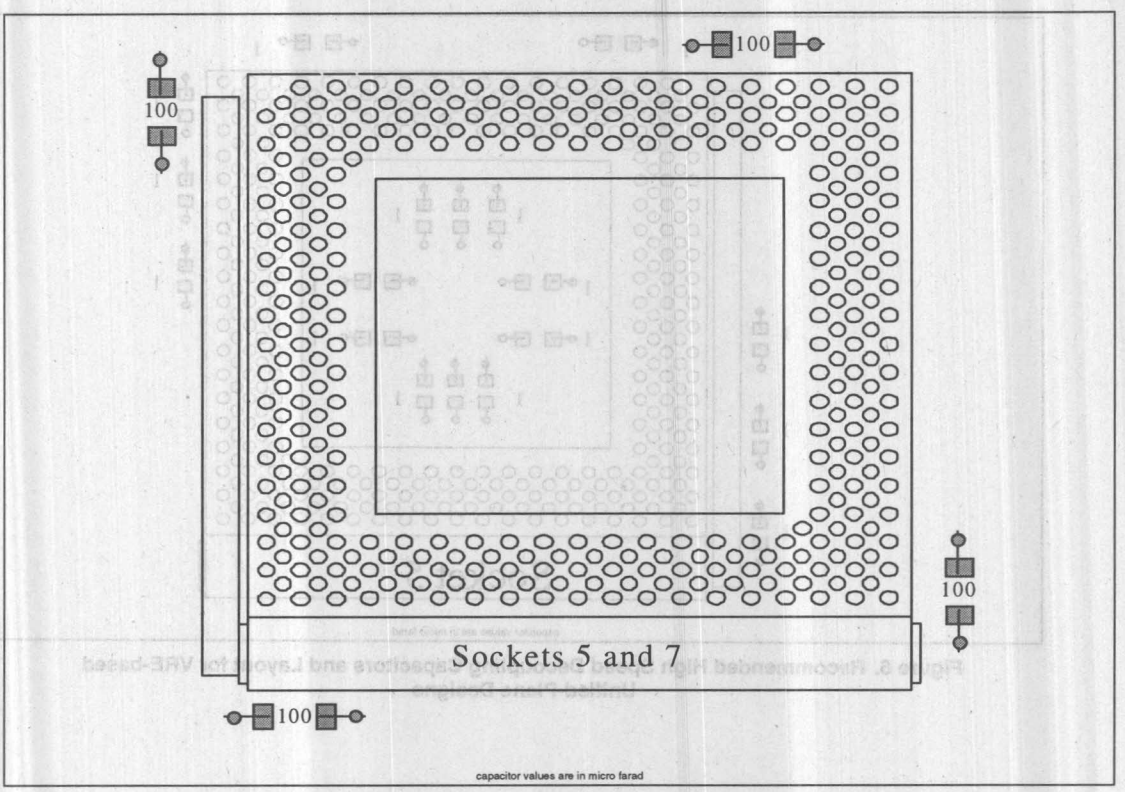


Figure 5. Recommended Bulk Decoupling Capacitor Values and Layout for VRE-based Design

Table 5. High Speed Decoupling Recommendations for 3.3V Platforms

Socket	Qty	Value	Type	Maximum ESR	Maximum ESL
Socket 5	18	1 µF	**X7R/X7S ceramic caps**	**0.83 mΩ** (15 mΩ/cap)	**0.117 nH** (2.1 nH/cap)
Socket 7	25	1 µF	**X7R/X7S ceramic caps**	**0.6 mΩ** (15 mΩ/cap)	**0.084 nH** (2.1 nH/cap)
Standard (Low Cost)	12	1 µF	**X7R/X7S ceramic caps**	**1.25mΩ** (15 mΩ/cap)	**0.175 nH** (2.1 nH/cap)

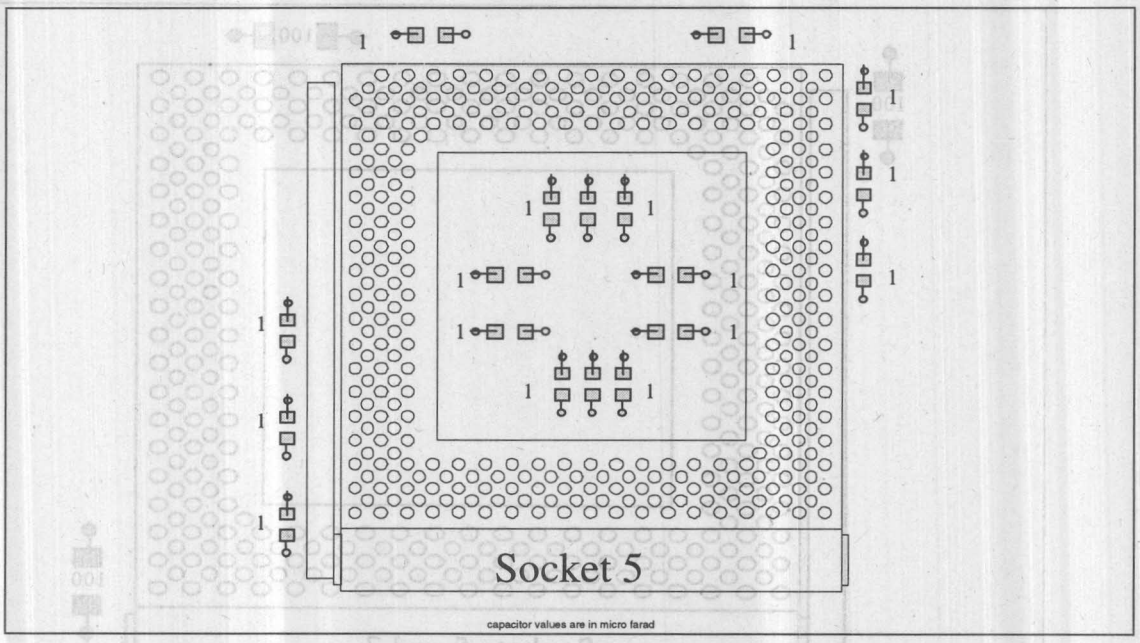


Figure 6. Recommended High Speed Decoupling Capacitors and Layout for VRE-based Unified-Plane Designs

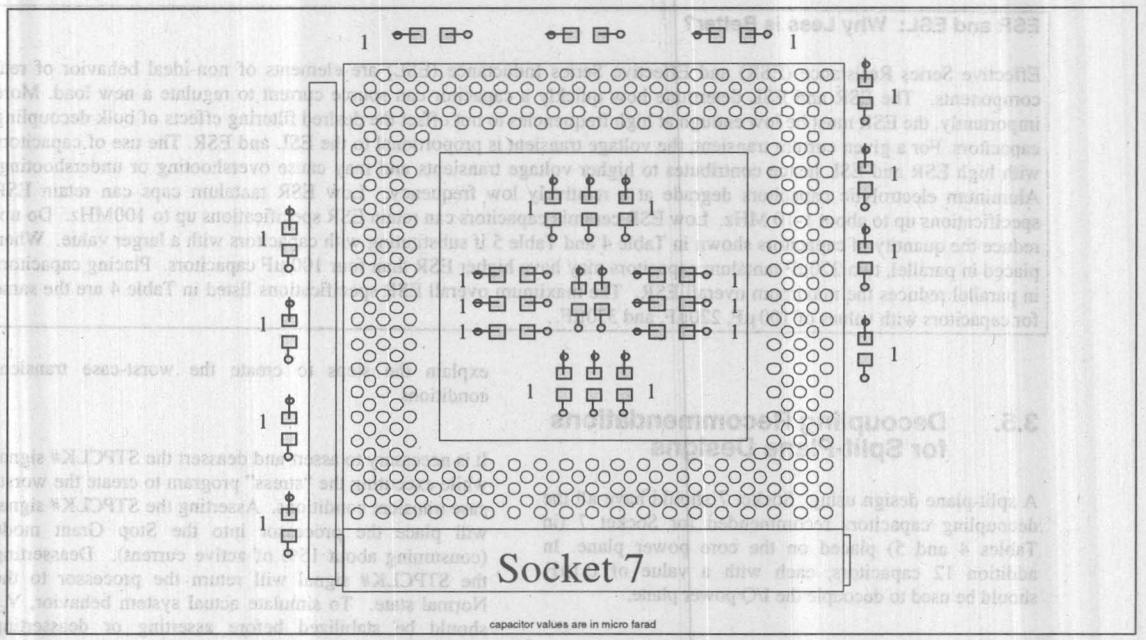


Figure 7. Recommended High Speed Decoupling Capacitors and Layout for VRE-based Unified-Plane Designs

were based on extensive simulations and experiments. They provide a robust, low cost solution to accommodate various Pentium processors and Pentium Overdrive processors. During system design cycles, questions may arise about reducing cost by reducing the amount of decoupling, substituting with different capacitor dielectrics, and using less accurate resistors. Before committing to any deviations from the recommendations, it is highly recommended that the solution be simulated and certified for the variety in components, temperatures, and lifetime degradations. **The use of fewer, and / or lower quality decoupling than indicated in this section is discouraged, even if voltage measurements indicate that the margin exists at 20MHz[1].**

Endnotes

1 The product test environment assumes a certain minimum amount of decoupling.

ESR and ESL: Why Less is Better?

Effective Series Resistance (ESR) and Effective Series Inductance (ESL) are elements of non-ideal behavior of real components. The ESR and ESL determine how quickly a capacitor can source current to regulate a new load. More importantly, the ESR must be low enough at high frequencies to not offset the desired filtering effects of bulk decoupling capacitors. For a given current transient, the voltage transient is proportional to the ESL and ESR. The use of capacitors with high ESR and ESL hence contributes to higher voltage transients and may cause overshooting or undershooting. Aluminum electrolytic capacitors degrade at a relatively low frequency. Low ESR tantalum caps can retain ESR specifications up to about 1-10 MHz. Low ESR ceramic capacitors can retain ESR specifications up to 100MHz. Do not reduce the quantity of capacitors shown in Table 4 and Table 5 if substituting with capacitors with a larger value. When placed in parallel, two 220µF tantalum capacitors may have higher ESR than four 100 µF capacitors. Placing capacitors in parallel reduces the maximum overall ESR. The maximum overall ESR specifications listed in Table 4 are the same for capacitors with values of 100 µF, 220µF, and 330µF.

3.5. Decoupling Recommendations for Split-Plane Designs

A split-plane design using Socket 7 should have all the decoupling capacitors recommended for Socket 7 (in Tables 4 and 5) placed on the core power plane. In addition 12 capacitors, each with a value of 0.1µF, should be used to decouple the I/O power plane.

4.0. TAKING VOLTAGE MEASUREMENTS

4.1. Creating Worst-Case Transient Excursion

The recommendations for regulators and local decoupling can be validated by creating worst-case supply transient conditions and measuring accurately. Worst-case transients may be generated by executing the "stress" program on a Pentium processor test sample (refer to Appendix A for directions on obtaining test samples and the "stress" program). The table below explain the steps to create the worst-case transient conditions

It is necessary to assert and deassert the STPCLK# signal while executing the "stress" program to create the worst-case transient conditions. Asserting the STPCLK# signal will place the processor into the Stop Grant mode (consuming about 15% of active current). Deasserting the STPCLK# signal will return the processor to the Normal state. To simulate actual system behavior, V_{cc} should be stabilized before asserting or deasserting STPCLK# as shown below. Asserting and deasserting STPCLK# too rapidly may generate unrealistic voltage transients. There are no minimum time specifications required to stabilize V_{cc} since the estimated time is highly dependent on the system (length of current instruction, outstanding write cycles, response time of voltage regulator, and accuracy and quantity of decoupling). However, based on experiments from the Pentium Processor Flexible Motherboard Reference Design, STPCLK# should be asserted and deasserted at a rate of 10-100KHz. As part of their power saving features, certain BIOS are able to assert/deassert STPCLK# during execution of a batch file (such as described in Table 6).

Table 6. Directions to Generate Worst-Case Transient

Step One	A	Install Pentium® processor
Step Two	B	Insert diskette containing the "stress" program
Step Three	C	Copy "STR4Y.EXE" to the C drive
Step Four	D	Create a batch file with an infinite loop that executes"STRY4.EXE" once in every loop. See Appendix A.
Step Five	E	Run the batch file created in step four.
Step Six	F	Measure V_{cc} and set oscilloscope as shown in Table 8 to obtain the voltage transient. The voltage transient must not overshoot 3.6V, or dip lower than 3.4V for VRE systems.
Step Seven	G	Assert and deassert STPCLK# while the "stress" program is executing.

Table 7. Measurement Technique Summary

Measurement Bandwidth[1]	≥ 20 MHz
Probe Bandwidth	≥ 250 MHz
Board Location	At the back of the board, at Socket pins
Pin Locations	12 Pins (listed above)

[1] Signals should be attenuated by no more than 3dB at 20MHz, and 6dB at 40MHz.

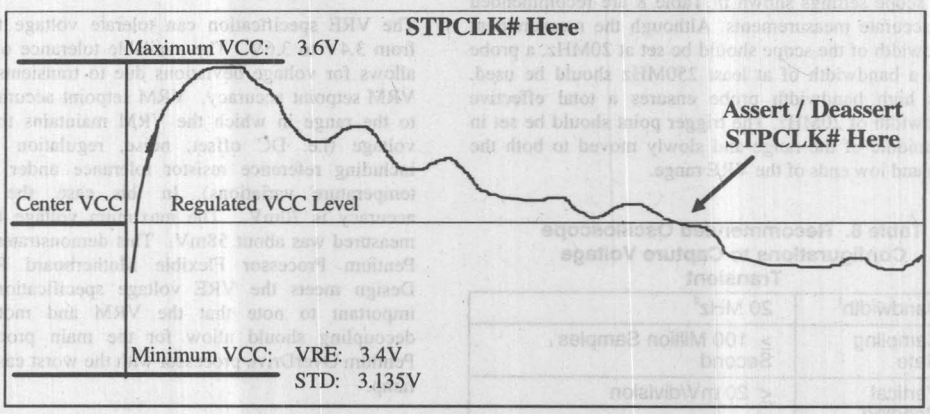


Figure 8. Method for Generating Worst-Case Transient via STPCLK#

4.2. Measurement Technique

All transient measurements must be taken at the back of the motherboard at the socket pins on an iPSL-certified Socket 5, Socket 7, or an equivalent socket of 5nH or less. Measuring transients on an unspecified socket or at a different location will result in inaccurate readings. For accurate readings, all probe connections must be clean. Shorten the ground lead of the probe to minimize any extra inductance. A specially-made probe as shown in Figure 9A will ensure accurate readings by connecting the probe tip directly to the V_{ss} signal and connecting four standoffs to the V_{ss} plane. Figure 9B proposes an alternate solution by providing a short loop of wire around the ground shield of the probe. Figure 9C is not a good example of how to perform measurements. The ground cable of the probe will add significant noise to the transient measurements.

The following V_{cc}/V_{ss} pairs should be measured, and must all meet the voltage specification: AN13/AM10, AN21/AM18, AN29/AM26, AC37/Z36, U37/R36, L37/H36, A25/B28, A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2. These pins are a subset of all V_{cc}/V_{ss} pairs, and hence should not be singled out when placing decoupling capacitors.

The scope settings shown in Table 8 are recommended for accurate measurements. Although the measurement bandwidth of the scope should be set at 20MHz, a probe with a bandwidth of at least 250MHz should be used. This high bandwidth probe ensures a total effective bandwidth of 20MHz. The trigger point should be set in the middle of the range and slowly moved to both the high and low ends of the VRE range.

Table 8. Recommended Oscilloscope Configurations to Capture Voltage Transient

Bandwidth[1]	20 MHz[2]
Sampling Rate	≥ 100 Million Samples / Second
Vertical Reading	≤ 20 mV/division
Horizontal Reading	≥ 500 nS/division
Display	Infinite Persistence

[1] Signals should be attenuated by no more than 3dB at 20MHz, and 6dB at 40MHz.

[2] A probe with a bandwidth of at least 250MHz should be used.

4.3. Measurement Results

The voltage transient measurement shown in Figure 10 was taken on the Pentium Processor Flexible Motherboard Reference Design (FMB) using the technique shown in Figure 9B. The Pentium Processor FMB is an actual motherboard designed to accommodate various Pentium Processors and Pentium OverDrive processors, regardless of specifications. The Pentium Processor FMB ensures accurate voltage regulation and proper decoupling through the Voltage Regulator Module (VRM), a small add-on module. To allow maximum flexibility, a variety of VRM models are available to accommodate all voltage specifications on the Pentium processors. For more detailed specifications of the Pentium Processor FMB or VRM, please refer to the *Pentium® Processor Flexible Motherboard Design Guidelines*, Revision 2.0 (Reference Number SC-0990).

Figure 10 shows the Pentium processor exiting the Stop Grant Mode. Measurements were taken with a Tektronix TDS-684A oscilloscope and P6245 probe, while running the "stress" program with STPCLK# toggling to potentially create worst case transients. STPCLK# was also used to trigger the measurement. The platform used a VRE Spec VRM.

The VRE specification can tolerate voltage transients from 3.4V to 3.6V. The available tolerance of 200mV allows for voltage deviations due to transients and for VRM setpoint accuracy. VRM setpoint accuracy refers to the range in which the VRM maintains the output voltage (i.e. DC offset, noise, regulation tolerance including reference resistor tolerance under line and temperature variations). In this case, the setpoint accuracy is 70mV. The maximum voltage transients measured was about 58mV. This demonstrates that the Pentium Processor Flexible Motherboard Reference Design meets the VRE voltage specification. It is important to note that the VRM and motherboard decoupling should allow for the main processor or Pentium OverDrive processor with the worst case current ramp.

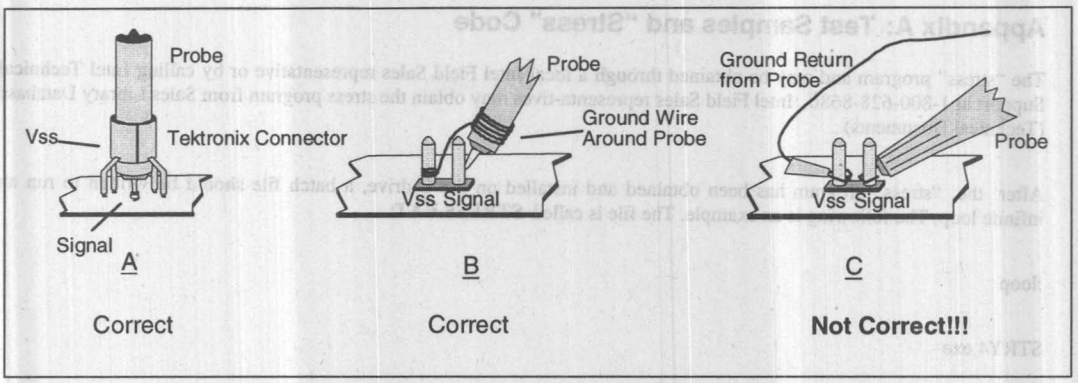


Figure 9. Correct and Incorrect Probe Connections for Measuring Transient

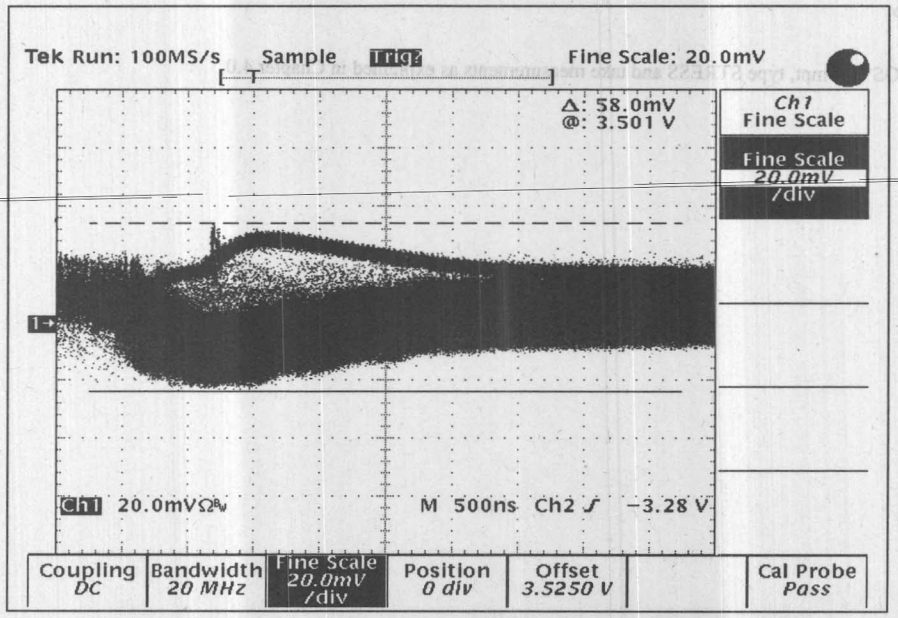


Figure 10. Transient Measurements with VRE Spec VRM

Appendix A: Test Samples and "Stress" Code

The "stress" program and may be obtained through a local Intel Field Sales representative or by calling Intel Technical Support at 1-800-628-8686. Intel Field Sales representa-tives may obtain the stress program from Sales Library Database (Technical Documents).

After the "stress" program has been obtained and installed on the C drive, a batch file should be written to run an infinite loop. The following is an example. The file is called **STRESS.BAT**:

```
:loop

STRY4.exe

echo on

goto loop
```

At the DOS* prompt, type STRESS and take measurements as explained in Chapter 4.0.

Appendix B: SPICE Models for Transient Simulations

OEMs with modeling capabilities may use a SPICE model to simulate voltage and current transient responses. Circuit models and SPICE Files that model the die, package, and sockets of future Pentium processors are being developed. These models may be obtained under the terms of a Non-Disclosure Agreement through a local Intel Field Sales representative.

Appendix C: Third Party Components

The following vendors offer various solutions to ensure a robust VRE-based platform. Please contact the following vendors for specifications, samples, and design support.

Table 9. Voltage Regulator Modules

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Linear Tech	Bob Scott Tel: (408) 432-1900 Fax: (408) 434-0507	Fred Killinger Tel: (49) 89-3197410 Fax: (49) 89-3194821	Dick Collins Tel: (65) 293-5322 Fax: (65) 292-0398	
Maxim/ Ambit[1]	David Timm (Maxim) Tel: (408) 737-7600 Fax: (408) 737-7194		Jacob Huang (Ambit) Tel: 886 35-784975 Fax: 886-35-775100	David Timm (Maxim) Tel: (408) 737-7600 Fax: (408) 737-7194
Power Trends[1]	Phil Lulewicz Tel: (708) 406-0900 Fax: (708) 406-0901		Joe Ywli Tel: (408) 737-7600 Fax: (408) 737-7194	Ken Katsumoto Tel: (81) 3-5367-9000 Fax: (81) 3-5467-0777
Semtech[1]	Art Fury Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-630350 Fax: (44) 592-774781	Art Fury Tel: (805) 498-2111 Fax: (805) 498-3804	
Siliconix	Howard Chen Tel: (408) 970-4151 Fax: (408) 970-3910	Eric Williams Tel: (44) 344-485757 Fax: (44) 344-427371	Howard Chen Tel: (408) 970-4151 Fax: (408) 970-3910	Tony Grizelj Tel: (81) 3-5562-3321 Fax: (81) 3-5562-3316

[1] DP VRM available

Table 10. Socket 7

Vendor	North America	Europe	APAC	Japan
Amp	Jim Crompton Tel: (910) 855-2338 Fax: (910) 855-2224	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Appros	Tony Goulart Tel: (415) 548-1636 Fax: (415) 548-1124		Appros Taiwan Inc. Tel: (886) 2-718-4774 Fax: (886) 2-718-4344	Appros Inc. Tel: (03) 3358-4857 Fax: (03) 3358-5734
Augat	David M. Barnum Tel: (508) 699-9890 Fax: (508) 695-8111	Arif Shahab Tel: (44) 952-670-281 Fax: (44) 952-670-342	Atsushi Sasaki Tel: (81) 44-853-5400 Fax: (81) 44-853-1113	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Ronny Chiou or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Yamaichi	Ann Sheperd Tel: (408) 456-0797 Fax: (408) 456-0779	Mr. Matsuda Tel: (49) 89-451021-43 Fax: (49) 89-451021-10	Alan Liu Tel: (886) 02-546-0507 Fax: (886) 02-546-0509	Mr. Shiwaku Tel: (81) 3-3778-6161 Fax: (81) 3-3778-6181

Table 11. Decoupling Capacitors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1µF, X7S	Dennis Lieberman Tel: (803) 946-0616 Fax: (803) 448-2606	Singapore Steve Chan Tel: (65) 258-2833 Fax: (65) 258-8221
	TPSD107K010R0100	100µF, Tantalum		Korea K.J. Kim Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
Johanson Dielectrics	160R18W105K4	1µF, X7R	Sales Department Tel: (818) 364-9800 Fax: (818) 364-6100	Taiwan Nanco Electronics Bill Yu Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Hong Kong Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100µF, Tantalum	Richey-Cypress Electronics Tel: (408) 956-8010 Fax: (408) 956-8245	Internation Accounts Warren Marshall Tel: (800) 421-7258 Fax: (714) 895-0060
Murata Electronics	GRM40X7R105J016	1µF, X7R	Sales Department Tel: (404) 436-1300 Fax: (404) 436-3030	Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721 Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (708) 803-6100 Fax: (708) 803-6296	Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090 Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108

Table 12. Header 7

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland	Rob Rix	H. Itoh	

	Tel: (717) 780-6045 Fax: (717) 780-7027	Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	Tel: (81) 44-844-8086 Fax: (81) 44-812-3203
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Ronny Chiou or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225

Table 13. Shorting Blocks

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Ronny Chiou or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Molex	Micheal Gits Tel: (708) 527-4801 Fax: (708) 969-1352	(Molex) Tel: (49) 89-413092-0 Fax: (49) 89-401527	(Molex) Tel: (65) 268-6868 Fax: (65) 265-6044	(Molex) Tel: (81) 427-21-5539 Fax: (81) 427-21-5562

Table 14. Resistors

Vendor	Size	Type	Accuracy/ Value	Contact
Beckman	0805	thin	0.1%, 10K-100K ohms	Cathy Whittaker
Industrial		thick	1-5%, 10-1M ohms	(214) 392-7616
	0603	thick	1-5%, 10-1M ohms	
Dale Electronic	0603	thin	0.5%, 10-100K ohms	Gary Bruns
		thick	1%,2%, 10-1M ohms	(402) 371-0080
	0805	thin	0.1%, 100-100K ohms	
Koa Spear	0805	thin	0.1%, 100-100K ohms	T. Yogi
		thick	0.5-5%, 10-1M ohms	(814) 362-5536
Thin Film Technology	1206	thin	0.1%, 100-250K ohms	Thin Film TECH. (607) 625 8445 Regional Sales Managers
			0.5%, 10-250K ohms	Patrick J Lyons ext. 14 All states W. of Mississippi except Texas and S. California
	0805	thin	0.1%, 100-100K ohms	
			0.5%, 10-1M ohms	Mark Porisch ext. 12 Southern U.S. E. of Mississippi including Texas
	0603	thin	0.1%, 100-33K ohms	
			0.5%, 10-330K ohms	Tim Goertzen ext. 13 Northen U.S. E. of Mississippi & Canada
	0402	thin	0.5%, 10-100K ohms	Mike Smith (310) 768-8923 Southern California

Pentium® Processor With Voltage Reduction Technology:

Power Supply Design Considerations for Mobile Systems

June 1997

Order Number: 242558-004

AP-519

APPLICATION NOTE

Pentium® Processor With Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems

June 1997

Order Number: 243328-004

1.0. INTRODUCTION

As the mobile market segment has closed the gap to desktop performance with equivalent notebook performance, the challenges to the system designer have increased tremendously. As the performance requirements have increased, so have the power consumption requirements. This results in the need for careful attention to thermal design to mitigate the potentially higher temperature within the system, to power supply designs which can supply the higher current needs, and to good power management design to extend battery life to an acceptable level. The focus of this application note is the power supply design considerations.

With the addition of the Pentium® processor with Voltage Reduction Technology to the processor roadmap, Intel is able to offer the higher performance level of a 90-MHz Pentium processor at a lower power consumption level than the Pentium processor 610\75 MHz. This allows the Pentium processor notebook designs to migrate to a higher performance Pentium processor without requiring major changes to existing designs. This allows the Pentium processor to migrate into the subnotebook market, which requires lower power consumption processors as well. The Pentium processor with Voltage Reduction Technology achieves lower processor power consumption by lowering the core voltage required by the processor while maintaining compatibility to existing I/O and memory through a separate 3.3 volt supply. The major advantage provided by this splitting of processor voltage requirements is that existing Pentium processor thermal designs will accept the higher performance while requiring minimal or no thermal changes.

The notebook design areas affected by the splitting of processor voltages are in the design of power supplies, the layout of printed circuit boards and the type, quality and quantity of capacitive decoupling provided at the processor. This application note will discuss these areas and make recommendations to allow the designer to minimize the changes to existing designs. This note does not address platform issues such as chip set support, graphics controllers and memory improvements needed to support the faster 60-MHz bus of the Pentium processor 90\60 MHz.

This application note was written for mobile system designers planning to migrate from Pentium processor 610\75 MHz designs to the Pentium processor with Voltage Reduction Technology designs. It is assumed that the reader is familiar with the documents listed in the reference section. It is highly recommended that these be read and understood before using the information in this note since this application note builds on the foundation created by these reports. Section 2 defines the differences between the Pentium processor 610\75 MHz and Pentium processor with Voltage Reduction Technology and outlines the areas to be aware of while designing a system for a Pentium processor with Voltage Reduction Technology. Section 3 discusses power supply design considerations resulting from split voltage requirements between the core and I/O logic. Section 4 discusses the power plane design considerations associated with printed circuit board development for the Pentium processor with Voltage Reduction Technology. Section 5 discusses the requirements for bulk and high frequency decoupling at the processor for both the core and I/O logic. Section 6 summarizes the results of empirical measurements of V_{CC} tolerance using the capacitance values recommended in section 5.0.

Note

The data presented in this application note reflects studies on a selected system. It is recommended that the following information be used as a starting point for designing a Pentium processor with Voltage Reduction Technology system and that measurements be made on individual systems to ensure a robust design.

2.0. DIFFERENCES BETWEEN PENTIUM® PROCESSOR 610\75 MHZ AND PENTIUM® PROCESSOR WITH VOLTAGE REDUCTION TECHNOLOGY

The architecture and internal features of the Pentium processor with Voltage Reduction Technology are identical to the Pentium processor 610\75 MHz, thereby maintaining hardware and software compatibility. The Pentium processor with Voltage Reduction Technology is offered in two versions, 75\50 and 90\60 MHz where the Pentium processor 610\75 MHz was only available in 75\50 MHz version. The Pentium processor with Voltage Reduction Technology will use the same packaging, Tape Carrier Package (TCP), used for the Pentium processor 610\75 MHz as well as the SPGA package. Experience gained in the manufacture of the Pentium processor 610\75 MHz TCP designs can be applied to a Pentium processor with Voltage Reduction Technology design.

The Pentium processor with Voltage Reduction Technology lowers processor power requirements by lowering the voltage required by the core logic of the processor. This results in an approximately 20 percent savings in power over the Pentium processor 610\75 MHz at the same frequency. The Pentium processor with Voltage Reduction Technology also separates the voltage required (V_{CC}) for core functions (2.9 volts) and that required for I/O functions (3.3 volts). The Pentium processor with Voltage Reduction Technology maintains the same V_{CC} tolerance as required on the Pentium processor 610\75 MHz for both the core V_{CC} as well as I/O V_{CC}.

The separation of the processor voltages puts new requirements on the power supply design, layout of PCBs and decoupling requirements at the processor. These areas will be covered in the next sections.

As processors migrate to lower and lower core voltages, it is important that power supply designs take into account this trend and provide flexibility in design to handle these future voltages. This will minimize changes required in the future.

3.0. POWER SUPPLY DESIGN CONSIDERATIONS

With the separation of V_{CC} between the processor core logic and I/O logic, an additional voltage regulator is required to supply the 2.9 volts required by the core. The load handling capability of this regulator will support the majority of the processor requirements (approximately 90 percent of total current) while the processor load handling requirement on the 3.3 volt regulator drops to approximately 10 percent of the total processor current requirement.

The designer can choose between two types of regulators to implement the required core voltage. Section 3.2 discusses the use of commonly available switching and linear regulators from Linear Technology Corporation and Maxim Integrated Products to supply this voltage. Regulators from other power supply vendors are also available.

3.1. Power Supply Current Requirements

The power supply current specifications are shown in the table below. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC} + 165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current charges occurring during transitions from stop clock to full active modes.

Table 1. Pentium® Processor with Voltage Reduction Technology Maximum Power Supply Current Specs

	Pentium® Processor 75 MHz	Pentium Processor 90 MHz
2.9 Volt Max $I_{CC}2$	2096 mA	2515 mA
3.3 Volt Max $I_{CC}3$	265 mA	318 mA

3.2. Voltage Regulator Options

To supply the additional voltage required for the core, designers have a choice of adding a linear or switching regulator to their design and regulating down from the battery output voltage. These two power supply regulators yield different ranges of efficiency. A linear regulator is much like a voltage divider which steps down the input voltage to a specified output level (e.g., from 12V or 5V to 2.9V). The maximum efficiency offered by a 5V to 2.9V linear regulator is 58 percent, as shown by the following equation:

$$Efficiency = \frac{Vout}{Vin} \times 100$$

$$= \frac{2.9V}{5.0V} \times 100$$

$$= 58\ \%$$

In this case, the remaining 42 percent is dissipated as heat. A switching regulator, however, generates an output voltage by pulsing the input voltage through a MOSFET switch and an inductor. Since there are no voltage divider-type losses as in a linear regulator and the AC switching losses are small, there is much less dissipated heat. Switching regulators commonly offer up to 95 percent efficiency. For this reason, it is recommended that a switching regulator be used to generate the 2.9 volt requirement of the core.

There are trade-offs for the increased efficiency. Switching regulators have a larger component count than linear regulators and also a higher cost. However, the efficiency of the switching regulator with its minimum power loss makes it more ideal for the mobile application.

A switching regulator and associated support components require approximately 1.5 square inches of board space to implement. The maximum current supplied by any design will depend on the supporting components used in the design. Most manufacturers supply a reference design to make the design process as easy as possible.

In providing the voltage source for the processor core, the power supply should be designed to provide this output by adding an additional regulator in parallel with the existing 3.3 volt source as indicated in Figure 1a. This will ensure the 2.9 volt regulator will not be affected by any inefficiencies in a previous regulation stage. Figure 1b is an example of an inefficient design since a cumulative effect results from the inefficiency of the 3.3 volt source being supplied to the input of the 2.9 volt regulator.

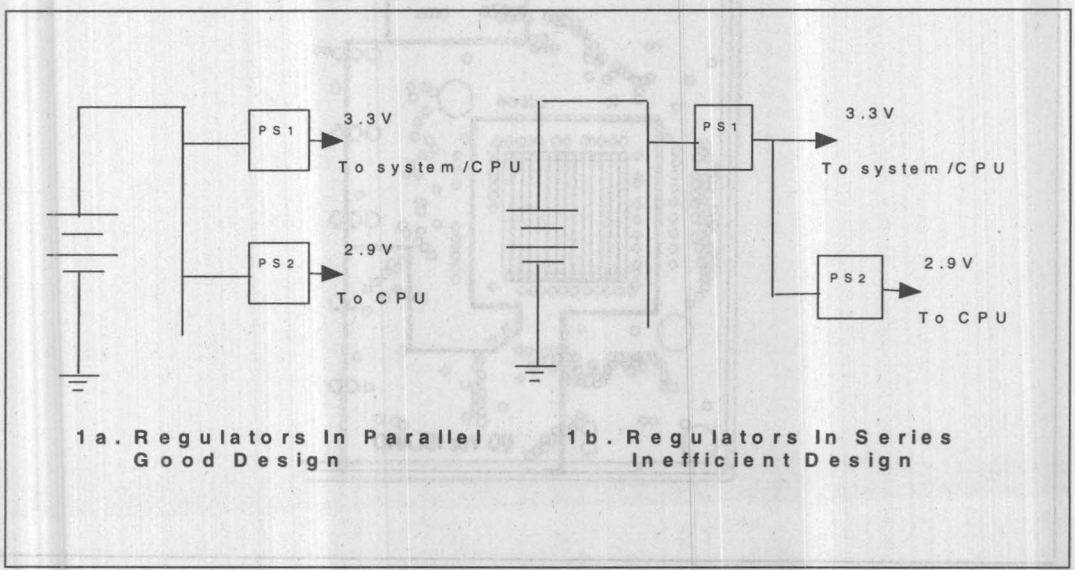


Figure 1. Examples of 2.9 and 3.3 Volt Regulators Connected in Parallel and in Series

Linear Technology Corporation and Maxim Integrated Products offer switching regulators that can be designed into power supplies meeting the maximum current and V_{CC} tolerance specifications of a Pentium processor mobile system (see Appendix C for vendor information). Other solutions may also be available from additional power supply vendors.

4.0. PCB LAYOUT CONSIDERATIONS

In most Pentium processor system board designs, the 3.3 volts for the processor is supplied on the board through a dedicated layer. With the requirement for a new 2.9 volt supply for the processor, it is not necessary to add a completely new power supply layer to the circuit board. It is possible to create a 2.9 volt "island" around the processor in the existing 3.3 volt power plane. The "island" needs to be large enough to include the processor, the required power supply decoupling capacitance (see section 5.0), and the necessary connections to the 2.9 volt source. The power supply regulator should be physically close to the processor.

Figure 2 is an example of a TCP power plane which contains several power islands. A large core voltage island surrounds the TCP package completely on three sides and partially on a fourth. The remainder of the fourth side provides access to I/O voltage pins for creating an I/O voltage island. Similar techniques can be used on SPGA packages as well.

The 2.9 volt voltage source, along with the desired amount of bulk and high frequency capacitance, should be located close to the processor to minimize inductance due to trace length. Trace widths should be kept as wide as possible to provide maximum current capability with minimal inductance.

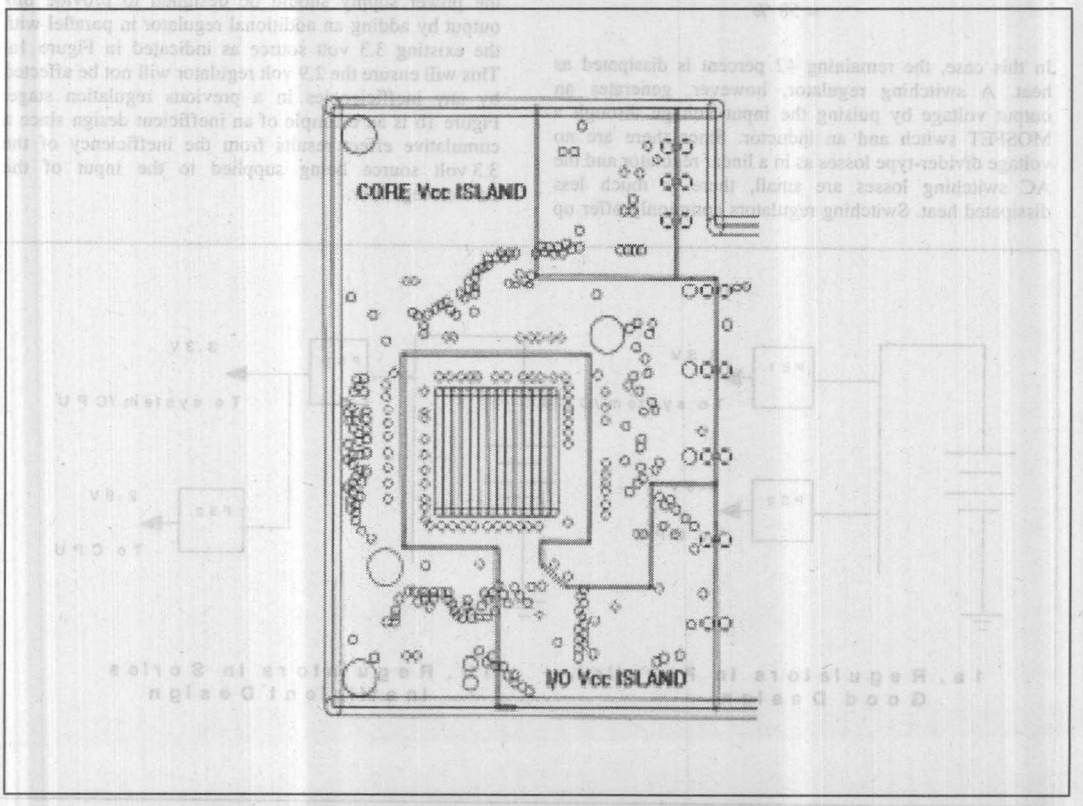


Figure 2. TCP Power Plane with Power Islands for Core and I/O V_{CC}

5.0. PROCESSOR CAPACITIVE DECOUPLING

Processor power supply decoupling is critical for reliable operation. There are two areas that the designer needs to address: high frequency decoupling resulting from small current changes in very fast transition periods (1-10 nS) and lower frequency decoupling resulting from large current changes in fast transition periods (50-300 nS).

The *Pentium® Processor 610\75 MHz Power Supply Considerations for Mobile Systems* application note indicates that the processor experiences rapid current changes transitioning between active operation and low power operation (Auto Halt Powerdown mode or STOP Grant state). These transitions occur in less than 100 nS with as much as 2.0 A in current change. Even during active operation, large current changes can occur from clock cycle to clock cycle, depending on the instruction mix of the application being executed. These rapid current changes result in large load changes to the power supply. When such load transients occur, current must be supplied from the power supply decoupling capacitors, since the power supply cannot change its output current instantly. Negative transients (voltage droop) occur when current load increases, while positive transients (voltage surges) occur when load current decreases.

The response time of a switching regulator power supply to a large transient current is limited by the value of the energy storing inductor, and is typically on the order of 10 uS or less. Adequate bulk capacitance, located as close as possible to the processor, is needed to provide current until the power supply can respond to the change in load. Capacitors with low ESR and ESL values are required to keep the processor supply voltage within the V_{CC} tolerance spec. Suggestions for the type and quantity of bulk decoupling capacitors to be used are provided in Section 5.1. The voltage transients caused by the rapid transitions between active and low power modes are additive to any DC voltage drops between the power supply regulator and the processor. Minimizing board level DC drops provides more margin for transient effects. This can be accomplished by using short, wide power traces to minimize resistance and inductance.

Due to the high internal speed of the processor and rapid transitions on the external bus, high frequency decoupling is also required. High frequency capacitors connected between the power and ground planes near the processor are required to filter these high frequency components of noise. Section 5.2 provides recommendations for the type and quantity of high frequency decoupling capacitors to be used.

5.1. Bulk Decoupling

As pointed out in Section 5.0, bulk decoupling is required with the Pentium processor, since the processor switches between normal and low power states very quickly, causing large instantaneous current changes. The resulting power supply voltage transient is illustrated in Figure 3.

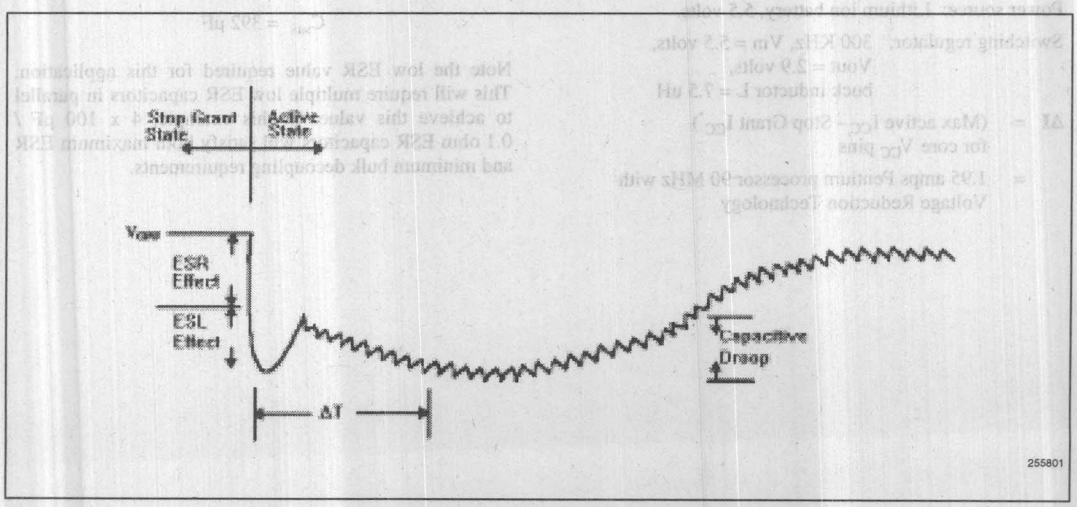


Figure 3. Example of Power Supply Voltage Transient

The voltage initially drops as the current encounters the decoupling capacitor's equivalent series resistance (ESR) and further undershoots by a voltage equal to the decoupling capacitor's equivalent series inductance (ESL) times the rate of change of current (di/dt). Then as the decoupling capacitor discharges, the power supply voltage droops until the power supply regulator reacts and is able to supply the full processor current. Since the processor is now active, high frequency noise also appears on the waveform. The system then settles to the initial voltage regulator setting, offset by any DC voltage drop. The total voltage dip must not exceed the voltage tolerance spec.

Part of the voltage tolerance specification is consumed by regulator tolerance (±2 percent), high frequency noise and any board level DC drops. The remaining amount is available to handle the processor active/low power transitions. Allocating about 1/2 of this amount for the ESR drop and the other 1/2 for the ESL undershoot and capacitive droop results in reasonable required values of ESR and ESL. If we allow too much for ESR, then the budget for ESL becomes prohibitive.

The following examples show how to determine the required component values, using a 60/40 ratio for ESR to capacitive droop. The solution can be fine-tuned to meet design requirements by adjusting the ratio between ESR and capacitive droop.

Core Supply Example

Power source: Lithium ion battery, 5.5 volts.

Switching regulator: 300 KHz, Vin = 5.5 volts, Vout = 2.9 volts, buck inductor L = 7.5 uH

ΔI = (Max active I_{CC} - Stop Grant I_{CC}*) for core V_{CC} pins

= 1.95 amps Pentium processor 90 MHz with Voltage Reduction Technology

= 1.78 amps Pentium Processor 75 MHz with Voltage Reduction Technology

ΔT = Regulator response time (ΔI = 1.95 amps, L = 7.5 uH) = 7 uS

ΔV = Voltage budget for ΔI

= V_{CC} tolerance specification (165 mV) - Regulator tolerance (2 percent) - high frequency noise (20 mV)*

= 165 mV - 2.9V x (0.02) - 20 mV = 87 mV

= $\Delta V_{ESR} + \Delta V_{CAPDROOP}$

* Adequately decoupled high frequency noise measures about 40 mV peak-to-peak.

Assume that the board DC drop is negligible.

Maximum allowable ESR:

$$ESR_{MAX} = \Delta V_{ESR} / \Delta I$$

Bulk decoupling can be calculated as:

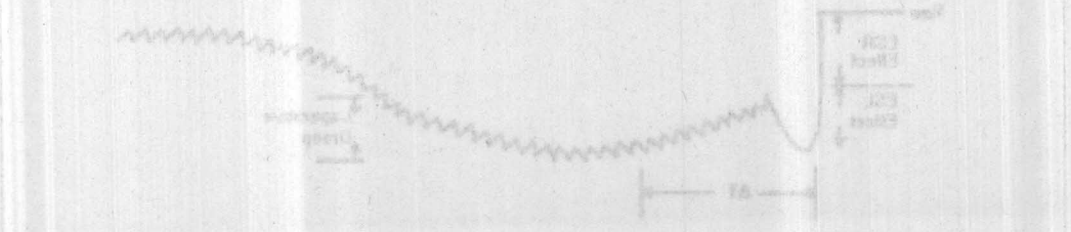
$$C_{MIN} = (\Delta I \times \Delta T) / \Delta V_{CAPDROOP}$$

Allocating 60 percent of ΔV for ESR effects (ΔV_{ESR} = (0.6) x 87 mV, $\Delta V_{CAPDROOP}$ = (0.4) x 87 mV) gives the following results:

$$ESR_{MAX} = 0.027 \text{ ohm}$$

$$C_{MIN} = 392 \ \mu F$$

Note the low ESR value required for this application. This will require multiple low ESR capacitors in parallel to achieve this value. In this example, 4 x 100 µF / 0.1 ohm ESR capacitors will satisfy both maximum ESR and minimum bulk decoupling requirements.



This has now ensured that the maximum power supply voltage droop will not exceed the processor voltage tolerance specification for transitions between active and Stop Grant states. An additional factor that must also be comprehended is the inductive undershoot resulting from the rapid rate of current change times the ESL of the decoupling capacitors. As the processor resumes activity, there are many large, instantaneous demands for power supply current as the various internal circuits start switching. There is a need to ensure that the resulting change in power supply voltage remains within limits. Since this inductive voltage effect is additive to the ESR drop, its magnitude must be less than or equal to the capacitive droop.

Maximum allowable ESL:

$$ESL_{MAX} = (\Delta V_{ESL} \times \Delta T) / \Delta I$$

where

ΔV_{ESL} = voltage drop across the capacitor due to parasitic inductance

ΔI = current change within a specified ΔT

ΔT = period in which current changes

A current slew rate of 40 mA / nS will be used for this calculation. With 40 percent of the previously calculated 87 mV budget as the maximum allowed value for ΔV, an overall ESL of less than or equal to 0.87 nH is needed.

$$ESL_{MAX} = (0.4) \times 87 \text{ mV} / (40 \text{ mA} / \text{nS}) = 0.87 \text{ nH}$$

Surface mount capacitors with short lead lengths are available with an ESL value of 2 nH. Since four capacitors in parallel are needed to achieve the required overall ESR value, using these 2 nH ESL capacitors will result in an overall value of 0.5 nH, and will meet the overall requirement with margin left over for any additional inductance due to board traces.

I/O Supply Example

Switching regulator: 300 KHz, Vin = 5.5 volts, Vout = 3.3 volts, buck inductor L = 7.5 uH

ΔI = IO supply current

= 318 mA Pentium processor 90 MHz with Voltage Reduction Technology

= 265 mA Pentium Processor 75 MHz with Voltage Reduction Technology

ΔT = Regulator response time (ΔI = 318 mA, L = 7.5 uH) = 3.0 uS

ΔV = Voltage budget for ΔI

= V_{CC} tolerance specification (165 mV) - Regulator tolerance (2 percent) - high frequency noise (20 mV) [1]

= 165 mV - 3.3V x (0.02) -20 mV = 79 mV

= $\Delta V_{ESR} + \Delta V_{CAPDROOP}$

[1] High frequency noise (about 40 mV peak-to-peak) from other devices on the 3.3 volt supply. Assume that the board DC drop is negligible.

Note:

This calculation is for the Pentium processor I/O supply bulk decoupling only. Other high power components, including the L2 cache, may require additional bulk decoupling to meet voltage tolerance specs for transitions between active and Stop Grant states.

Maximum allowable ESR:

$$ESR_{MAX} = \Delta V_{ESR} / \Delta I$$

Minimum bulk decoupling:

$$C_{MIN} = (\Delta I \times \Delta T) / \Delta V_{CAPDROOP}$$

Allocating 60 percent of ΔV for ESR effects (ΔV_{ESR} = (0.6) x 79 mV, $\Delta V_{CAPDROOP}$ = (0.4) x 79 mV) gives the following results:

ESR_{MAX} = 0.150 ohm C_{MIN} = 30 µF

Again, please note the significance of low ESR. Use a 33 µF / 0.15 ohm ESR capacitor.

The current transients associated with I/O pin switching are small relative to the processor core and also much faster. Small, high frequency capacitors are needed to handle these current demands. The bulk decoupling capacitor is less important in this respect, and so there is no specific calculation of required ESL. Regardless, low ESL (short lead, surface mount, ESL = 2 nH) capacitors are recommended for I/O supply bulk decoupling.

Table 2. Pentium® Processor with Voltage Reduction Technology Bulk Decoupling Estimates (300-KHz Regulator)

	Pentium® Processor 75 MHz	Pentium Processor 90 MHz
2.9 Volt Core Decoupling	4x 100 µF / 0.1 ohm ESR / 2 nH ESL	4x 100 µF / 0.1 ohm ESR / 2 nH ESL
3.3 Volt I/O Decoupling	33 µF / 0.15 ohm ESR / 2 nH ESL	33 µF / 0.15 ohm ESR / 2 nH ESL

5.2. High Frequency Decoupling

High frequency decoupling is also critical for reliable operation. High frequency transients can be minimized by the use of multiple 1.0 µF and 0.01 µF bypass capacitors. Ceramic high frequency capacitors have the best high frequency performance and should be placed as close as possible to the processor between the processor power and ground pins. As a first approximation it is recommended that in a Pentium processor with voltage reduction technology design, the number of high frequency capacitors to be used should be equivalent to the number of capacitors used in a Pentium processor 610\75 MHz design. These capacitors should be split between the core V_{CC} and I/O V_{CC}.

In the testing to be described in the next section, it was found that using eight ceramic capacitors on the core V_{CC} and eight ceramic capacitors on the I/O provided adequate high frequency decoupling to maintain V_{CC} tolerance limits.

6.0. EXPERIMENTAL VERIFICATION OF CAPACITANCE ESTIMATES

A 90-MHz Pentium processor was used to verify the performance of the processor bulk capacitance recommendations. The 2.9V to the core was supplied by a 300-KHz switching regulator, and the 3.3V was supplied to the I/O by another 300-KHz switching regulator.

The method of measuring worst-case transients used for the experiments required the assertion of the STPCLK# input pin. Mobile chip sets provide support for STPCLK# control through programming a register which toggles STPCLK#. Oscilloscope probes were connected to STPCLK#, $V_{CC}2$ (core V_{CC}), $V_{CC}3$ (I/O V_{CC}) and STPCLK# was used as the trigger source.

Since the STPCLK# pin is toggled through the chip set hardware or by using a pulse generator connected to processor STPCLK# pin, additional software can be executed by the processor to produce high load conditions. DOS Edit with menu pulldown is an example of code which causes steady state high power consumption by the processor (about 5.1 W for the Pentium processor 90 MHz, depending on the system configuration). DOS Edit was used for these experiments. A high-power, FPU-intensive code loop can also be acquired from Intel (contact your local Intel sales representative) which will provide similar results. It should be noted that in making a measurement, sufficient time should be allowed to elapse before the power state is toggled. For example, a 300-KHz switching regulator typically takes about 7 µs to respond to a load change. If the power state is toggled before 7 µs, the overall response of the regulator cannot be viewed since the regulator has not had adequate time to respond.

The following discussions cover three different configurations of decoupling/filtering capacitance applied around the core and I/O V_{CC} pins of the Pentium processor on the daughter card. The first of these traces (Figure 4 below) illustrates the results from the recommended capacitance configuration and shows the overall pattern of STPCLK# used to drive the experiments.

The middle signal in Figure 4 is the I/O V_{CC} and the upper signal is the core V_{CC}. Note that the core voltage increases by 80 mV to 90 mV in the STPCLK# active (low) region, since the current drawn is greatly reduced, and thus so are the voltage drops along the power buses. (In our experimental setup, we had greater resistance in the power busses than recommended for production systems, and thus larger DC offsets between the power states.) Also as expected, the noise level on the V_{CC} pins is reduced in the STPCLK# active region, especially for the core V_{CC}, since the core activity is essentially turned off and most of the noise on the core V_{CC} pins is generated inside the processor itself.

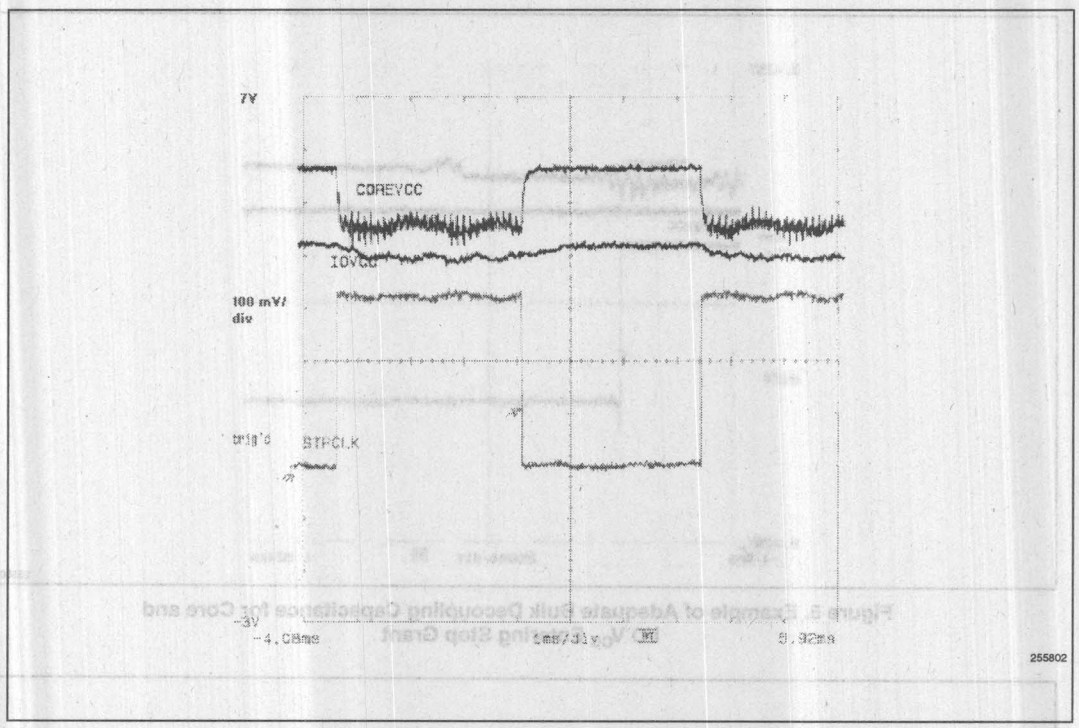


Figure 4. Example of Adequate Bulk Decoupling Capacitance for Core and High Frequency Capacitance

Using the recommended capacitance:

Bulk capacitors: core: 4 - 100 µF, I/O: 1- 47 µF

High frequency capacitor: core: 6 - 0.1 µF, 2 - 0.01 µF, I/O: 2 - 0.1 µF, 6 - 0.01 µF

The example system always operates within V_{CC} specifications and always works reliably. The largest variation from core V_{CC} minimum to maximum (peak-to-peak variation, including the DC offset) is about 150 mV peak-to-peak, which is well within the 214 mV tolerance (core V_{CC} tolerance - core regulator tolerance). The largest peak-to-peak variation in the I/O V_{CC} is about 50 mV, which is also well within the 198 mV tolerance (I/O V_{CC} tolerance - I/O regulator tolerance). (Note that in a production model, more guardband would be obtained by reducing the DC offset between the power states.)

Figures 5 and 6 illustrate the transition into and out of the Stop Grant state with a finer time resolution. The time scale of 200 ns will allow viewing undershoot and overshoot if they occur. The pictures show that using the recommended capacitive decoupling, there is no significant V_{CC} overshoot when STPCLK# is asserted or undershoot when it is deasserted.

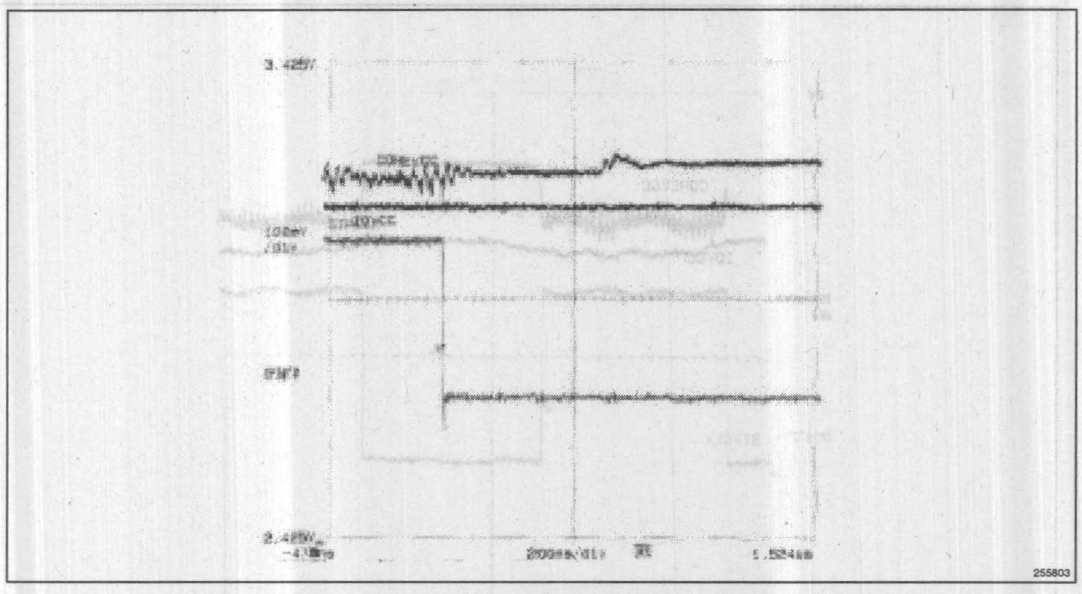


Figure 5. Example of Adequate Bulk Decoupling Capacitance for Core and I/O V_{CC} Entering Stop Grant

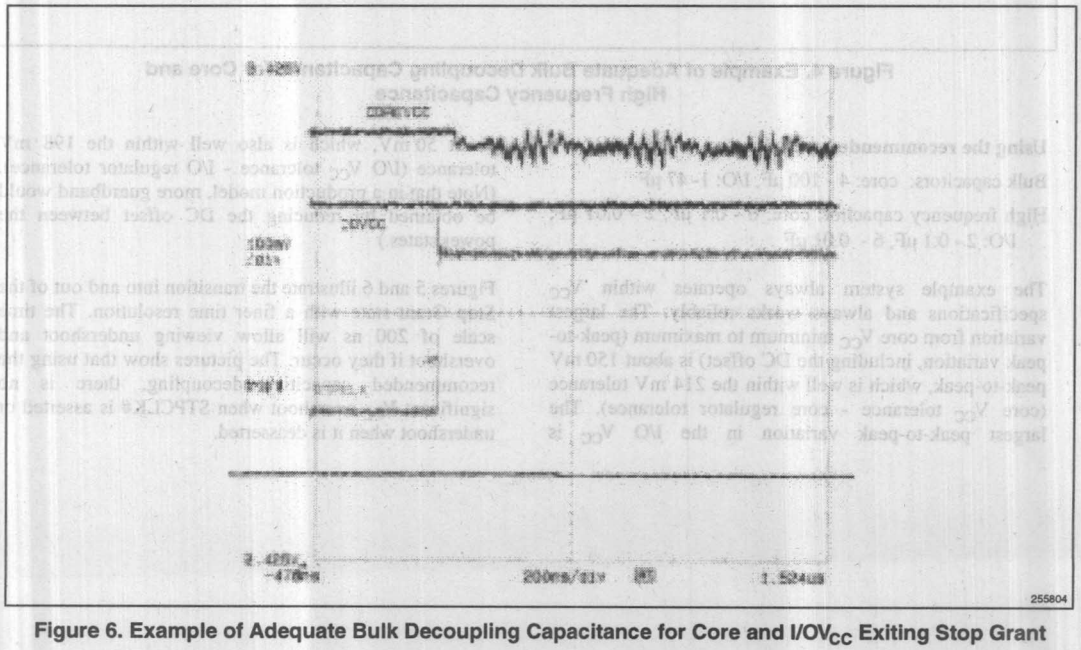


Figure 6. Example of Adequate Bulk Decoupling Capacitance for Core and I/OV_{CC} Exiting Stop Grant

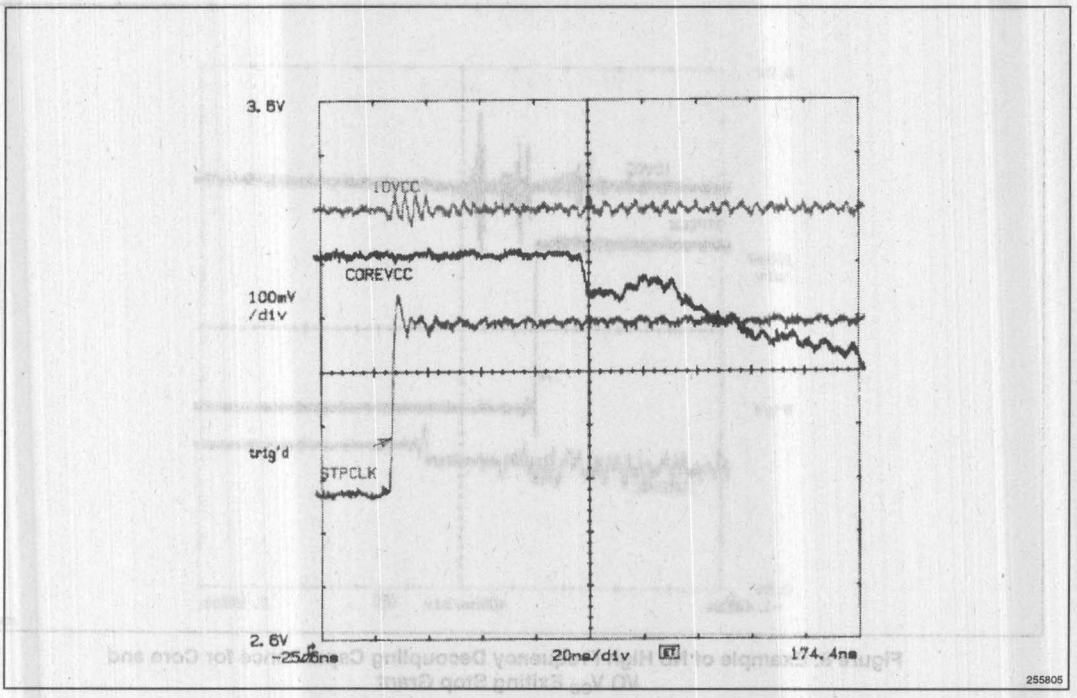


Figure 7. Example of No Bulk Decoupling Capacitance for Core and I/OV_{CC} Exiting Stop Grant

Using only high frequency filter capacitors:

Bulk Capacitors: 0; Standard high frequency filter Capacitors

Frequent large violations of specifications were observed on both I/O and core V_{CC}s. Figure 7 shows sizable ringing in the V_{CC} values after the processor enters the Stop Grant state with a peak-to-peak range of 210 mV on V_{CC} core, and about 65 mV on V_{CC} I/O. As expected, there is a severe droop in the core V_{CC} due to the lack of bulk capacitors to handle the abrupt change in load and the voltage tolerance specification is violated. The picture also illustrates the importance of the bulk decoupling for the core V_{CC}, where the largest load transients occur. Note also that although these experiments were done with no bulk capacitors added to the processor card, there was still capacitance in the power supply, small capacitance from loads and board effects, and a total of 0.88 µF from the high frequency capacitors.

Using *no* high frequency filter capacitors, with recommended bulk capacitors:

Bulk Capacitors: 400 µF core; 47 µF I/O.
High frequency Capacitors: None

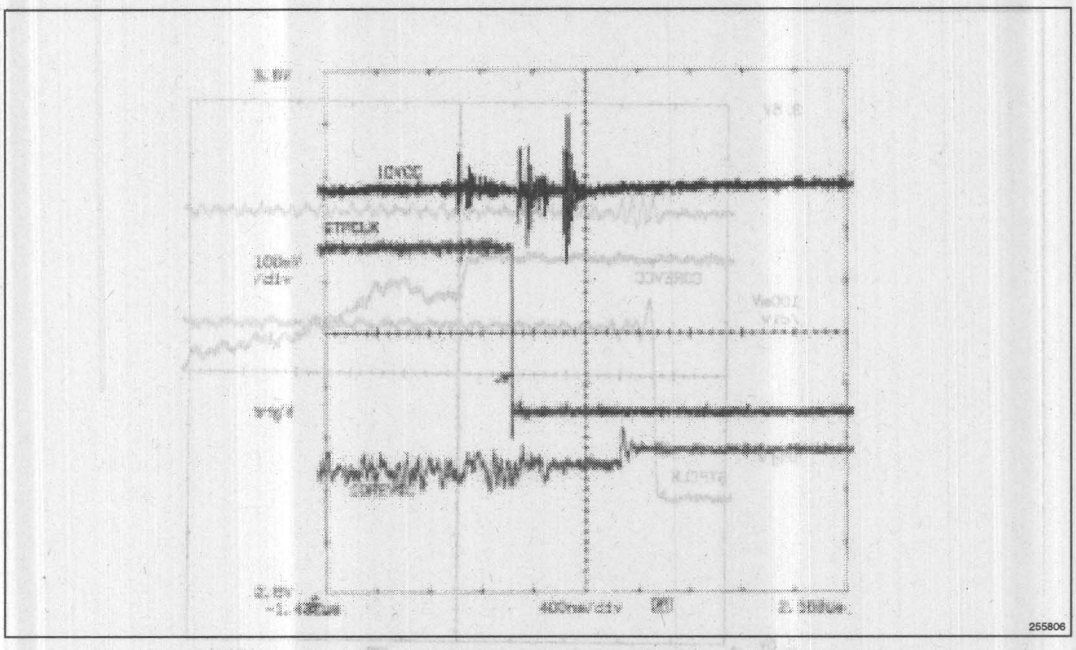


Figure 8. Example of No High Frequency Decoupling Capacitance for Core and I/O V_{CC} Exiting Stop Grant

A high magnitude of high frequency noise was observed on both the core and I/O V_{CC}. Figure 8 shows almost 300 mV of peak-to-peak noise on the I/O V_{CC}, and about 125 mV of peak-to-peak noise on the core V_{CC}. In this case, the system does not meet the voltage tolerance specifications and is not stable.

Note

The data presented in this application note reflects studies on a selected system. It is recommended that the following information be used as a starting point for doing a Pentium processor with voltage reduction technology system and that measurements be made on individual systems to ensure a robust design.

7.0. SUMMARY

With the addition of the Pentium processor 90 MHz to the microprocessors a designer has to choose from, additional design issues must be addressed. The separation of core and I/O voltages requires the use of an additional regulator to supply the 2.9 volt requirement of the core. This in turn requires the separation of power planes on the system board or daughter card. Appropriate decoupling of the core V_{CC} and I/O V_{CC} is also required to ensure the V_{CC} tolerance specifications are met.

Using power islands for core V_{CC} and I/O V_{CC} offer the designer an option to avoid using an additional power plane for the system board or daughter card. There are switching regulator controllers commercially available which can be used to design power supplies to source the worst case current for the Pentium processor with Voltage Reduction Technology. Transients during large current changes can be overcome by using adequate bulk decoupling capacitance. Additional high frequency decoupling will help reduce high frequency noise to an acceptable level. It is recommended that the bulk and high frequency capacitance estimates provided in this note, be used as a starting point for selecting the correct amount of decoupling used in a Pentium processor with Voltage Reduction Technology. It is further recommended that the V_{CC} tolerance for both core and I/O be verified through the use of applications (such as DOS Edit, and I/O intensive benchmarks) which provide a worst case operational scenario. This will ensure that the final design will meet V_{CC} tolerance specifications.

APPENDIX A. EXPERIMENTAL PLATFORM

All measurement data and oscilloscope traces were taken on the following platform/test equipment:

Neptune* 82430 PCI Evaluation System
TCP-to-SPGA Converter Nehemiah Card
300-KHz Switching Regulator Power Supply
Tektronix* TLS216 Logic Scope (16 Channel, 2 Hz)
Tektronix Pulse Generator PG2011

APPENDIX B. REFERENCES

Pentium® Processor at iComp® Index 610\75 MHz (Order Number 242323) †

Pentium® Processor (610\75) Power Supply Considerations for Mobile Systems Application Note, (Order Number 242415)

AP517 Pentium® Processor (610\75) Power Consumption Application Note, (Order Number 242416)

AP515 Pentium® Processor (610\75) TCP System Thermal Design Application Note, (Order Number 242414)

APPENDIX C. VENDORS PROVIDING VOLTAGE REGULATORS AND CAPACITORS

The list below is meant to be representative only, and does not include all vendors of a particular type. Intel has not tested all of the components listed below and cannot guarantee that these components will meet every PC manufacturers specific requirements.

Voltage Regulators:

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
Tel. (408) 432-1900

Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94086
Tel. (408) 737-7600

Decoupling Capacitors:

AVX Corporation TPSE Series
Myrtle Beach, South Carolina 29577 USA

KEMET Electronics Corporation T Series
P.O.Box 5928
Greenville, South Carolina 29606 USA
Tel. (803) 963-6348

Nichicon (American) Corporation PL Series
927 East State Parkway,
Schaumburg, Illinois 60173 USA

Sanyo Video Components OS-CON Series
2001 Sanyo Ave.
San Diego, California 92073 USA
Tel. (619) 661-6835

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intel®

AP-480

APPLICATION NOTE

Pentium® PROCESSOR THERMAL DESIGN GUIDELINES REV. 2.0

November 1995

Order Number: 241575-003

Pentium® PROCESSOR THERMAL DESIGN GUIDELINES REV. 2.0

November 1995

Order Number 241575-003

1.0 INTRODUCTION

In a system environment, the Pentium® processor's temperature is a function of both the system and component thermal characteristics. The system level thermal constraints imposed on the package are local ambient temperature and thermal conductivity (i.e., airflow over the device). The Pentium processor thermal characteristics depend on the package (size and material), the type of interconnection to the printed circuit board (PCB), the presence of a heat sink, and the thermal conductivity and the power density of the PCB.

All of these parameters are aggravated by the continued push of technology to increase the operating speeds and the packaging density. As operating frequencies increase and packaging size decreases the power density increases and the heat sink size and airflow become more constrained. The result is an increased importance on system design to ensure that thermal design requirements are met for each component in the system.

In addition to heat sinks and fans, there are other solutions for cooling integrated circuit devices. A few of these solutions are: fan mounted on heat sink, heat pipes, thermoelectric (peltier) cooling, liquid cooling, etc. While these alternatives are capable of dissipating additional heat, they have disadvantages in terms of system cost, complexity, reliability, and efficiency. These techniques are more expensive than a passive heat sink and fan. The introduction of active devices can also decrease reliability. Finally, the power efficiency of some of these techniques is poor, and gets worse as the amount of power being dissipated increases. Despite these disadvantages, each of these solutions may be the right one for particular system implementations.

However, for the purpose of this application note, Intel has focused its efforts on describing solutions using passive heat sinks and fans.

1.1 Document Goal

The goal of this document is to provide thermal performance information for the Pentium processor and recommendations for meeting the thermal requirements imposed on systems. This application note attempts to provide an understanding of the thermal characteristics of the Pentium processor and some examples of how the thermal requirements can be met.

2.0 IMPORTANCE OF THERMAL MANAGEMENT

Thermal management of an electronic system encompasses all of the thermal processes and technologies that must be employed to remove and transfer heat from individual components to the system's thermal sink in a controlled manner.

The objective of thermal management is to ensure that the temperature of all components is maintained within functional and absolute maximum limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance or cause logic errors. The absolute maximum temperature limit is the highest temperature that a portion of the component may be safely exposed. Temperatures exceeding the limit can cause physical destruction or may result in irreversible changes in operating characteristics. Higher temperatures result in earlier failure of the devices in the system. Every 10°C rise above the operating range means a halving of the mean time between failures.

3.0 Pentium® PROCESSOR POWER SPECIFICATIONS

The Pentium processor's power dissipation and case temperature specs for 60 MHz and 66 MHz are shown in Table 1.

To ensure functionality and reliability of the Pentium processor, maximum device junction temperature must remain below 90°C. Considering the power dissipation levels and typical ambient environments of 40°C to 45°C, the Pentium processor's junction temperatures cannot be maintained below 90°C without additional thermal enhancement to dissipate the heat generated by this level of power consumption.

The thermal characterization data described in Table 2 illustrates that both a heat sink and airflow are needed. The size of heat sink and the amount of airflow are interrelated and can be traded off against each other. For example, an increase in heat sink size decreases the amount of airflow required. In a typical system, heat sink size is limited by board layout, spacing, and component placement. Airflow is limited by the size and number of fans along with their placement in relation to the components and the airflow channels. In addition, acoustic noise constraints may limit the size or types of fans limiting the airflow.

To develop a reliable thermal solution, all of the above variables must be considered. Thermal characterization and simulation should be carried out at the entire system level accounting for the thermal requirements of each component.

4.0 THERMAL PARAMETERS

Component power dissipation results in a rise in temperature relative to the temperature of a reference point. The amount of rise in temperature depends on the net thermal resistance between the junction and the reference point. Thermal resistance is the key factor in determining the power handling capability of any electronic package.

Thermal resistance from junction to case (θ_{JC}), and from junction to ambient (θ_{JA}) are the two most often specified thermal parameters for integrated circuit packages.

4.1 Ambient Temperature

Ambient temperature is the temperature of the undistributed ambient air surrounding the package. Denoted T_A, ambient temperature is usually measured at a specified distance away from the package. In the laboratory test environment, ambient temperature is measured 12 inches upstream from the package under investigation. In a system environment, ambient temperature is the temperature of the air upstream to the package and in its close vicinity.

Table 1. Pentium® Processor Power Dissipation

	Package Type	Total Pins	Pin Array	Package Size	Power (Typical)	Power (Max)	Max Case Temp (°C)
Pentium Processor 60 MHz	PGA	273	21 x 21	2.16" x 2.16"	11.9W	14.6W	80
Pentium Processor 66 MHZ	PGA	273	21 x 21	2.16" x 2.16"	13W	16W	70

4.2 Case Temperature

Case temperature, denoted T_C, is measured at the center of the top surface (on top of the heat spreader, see Figure 1) of the package, typically the hottest point on the package case. Special care is required when measuring the case temperature to ensure an accurate temperature measurement. Thermocouples are often used to measure T_C. Before any temperature measurements, the thermocouples have to be calibrated. When measuring the temperature of a surface which is at a different temperature from the surrounding ambient air, errors could be introduced in the measurements. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface, heat loss by radiation or by conduction through thermocouple leads. To minimize the measurement errors, it is recommended to use the following approach:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number: OB-100).
- The thermocouple should be attached at a 90° angle as shown in Figure 1. When a heat sink is attached a hole (no larger than 0.15") should be drilled through the heat sink to allow probing the center of the package as shown in Figure 1.
- If the case temperature is measured with a heat sink attached to the package, drill a hole through the heat sink to route the thermocouple wire out.

4.3 Junction Temperature

Junction temperature, denoted T_J, is the average temperature of the die within the package.

The junction temperature for a given junction-to-ambient thermal resistance, power dissipation, and ambient temperature is given by the following formula:

$$T_J = P_D * \theta_{JA} + T_A$$

If a heat sink with thermal resistance of θ_{SA} (sink-to-ambient) is used, then the thermal resistance from the junction-to-case, θ_{JC}, is given by the following formula:

$$T_J = P_D * (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

where:

θ_{CS} is the thermal resistance from the component (case) to the heat sink.

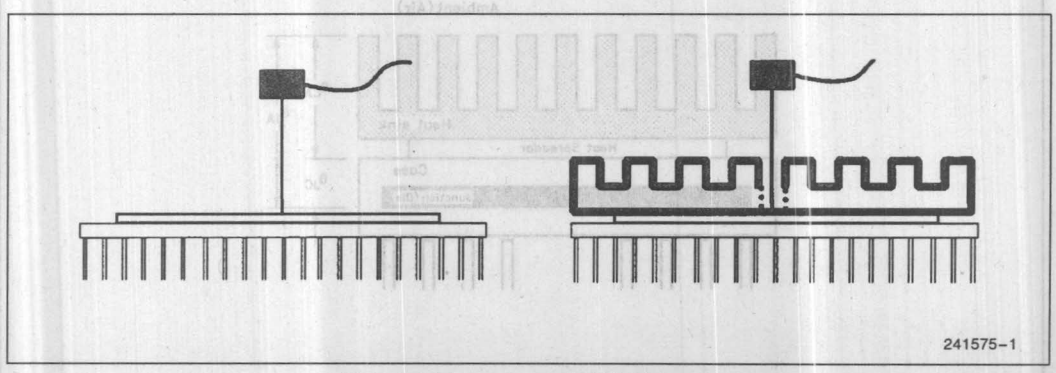


Figure 1. Thermocouple Attachment

4.4 Thermal Resistance

Thermal resistance (Figure 2) values for junction-to-ambient, θ_{JA} and junction-to-case, θ_{JC}, are used as measures of IC package thermal performance. θ_{JC} is a measure of the package's internal thermal resistance along the major heat flow path from silicon die to package exterior. This value is strongly dependent on the material, thermal conductivity, and geometry of the package. θ_{JC} values also depend on the location of the reference point (in this case center of the package top surface), the external cooling configurations and the heat flow paths from the package to the ambient. For example, if a heat sink is attached to the package top surface or more heat is pulled into the board through the pins, the θ_{JC} values measured with reference to the center of the package top surface will change. θ_{JA} values include not only internal thermal resistance, but also the radiative and convective thermal resistance from the package exterior to ambient air. θ_{JA} values depend on the material, thermal conductivity, and geometry of the package and also on ambient conditions such as airflow rates and coolant physical properties.

In order to obtain thermal resistance values, junction temperature is measured using the temperature sensitive parameter (TSP) method. With this method, special design thermal test structures are used which are approximately the same size as the Pentium processor die. The test structure consists of resistors and diodes. Resistors are used to simulate the Pentium processor power dissipation and thereby heat up the package. Diodes, which are located at the center of the thermal test die, are used to measure the die temperature. The measurements are carried out in a wind tunnel environment. The air flow rate and the ambient temperature are measured 12 inches away from the package in the upstream air.

The parameters are defined by the following relationships:

$\theta_{JA} = (T_J - T_A)/P_D$

$\theta_{JC} = (T_J - T_C)/P_D$

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

where:

θ_{JA} = junction-to-ambient thermal resistance (°C/W)

θ_{JC} = junction-to-case thermal resistance (°C/W)

θ_{CA} = case-to-ambient thermal resistance (°C/W)

T_J = average die (junction) temperature (°C)

T_C = case temperature at a pre-defined location (°C)

T_A = ambient temperature (°C)

P_D = device power dissipation (W)

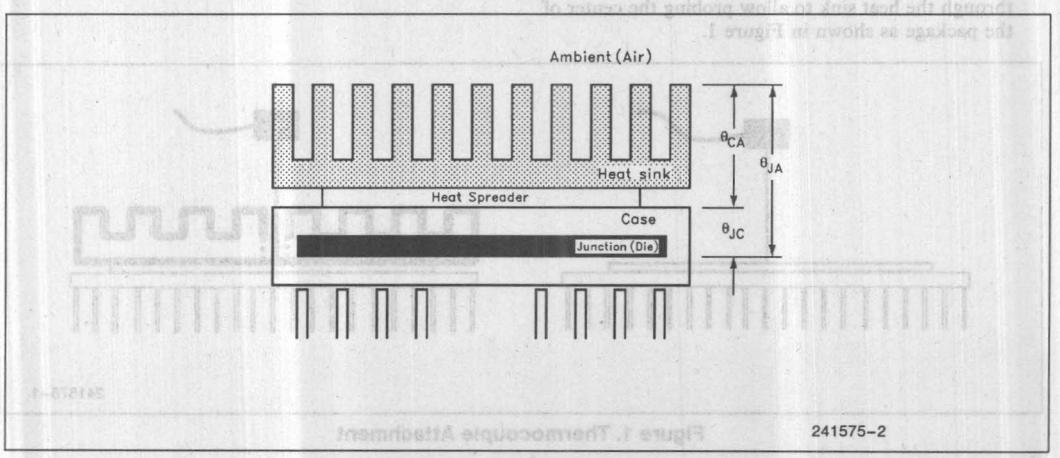


Figure 2. Thermal Resistance Parameters

Table 2 lists the junction-to-case and case-to-ambient thermal resistances for the Pentium processor (with and without a heat sink).

Table 2. Thermal Characterization Data

	θ_{JC}	θ_{CA} **vs Airflow (ft/min.)					
		0	200	400	600	800	1000
With 0.25″ Heat Sink	0.6	8.3	5.4	3.5	2.6	2.1	1.8
With 0.35″ Heat Sink	0.6	7.4	4.5	3.0	2.2	1.8	1.6
With 0.65″ Heat Sink	0.6	5.9	3.0	1.9	1.5	1.2	1.1
Without Heat Sink	1.2	10.5	7.9	5.5	3.8	2.8	2.4

NOTE:
Heat Sink: 2.1 in^2 base, omni-directional pin Al heat sink with 0.050 in. pin width, 0.143 in. pin-to-pin center spacing and 0.150 in. base thickness. Heat sinks are attached to the package with a 2 to 4 mil thick layer of typical thermal grease. The thermal conductivity of this grease is about 1.2 w/m c.
** θ_{CA} values shown in this table are typical values. The actual θ_{CA} values depend on the air flow in the system (which is typically unsteady, non-uniform and turbulent) and thermal interactions between Pentium CPU and surrounding components through PCB and the ambient.

5.0 DESIGNING FOR THERMAL PERFORMANCE

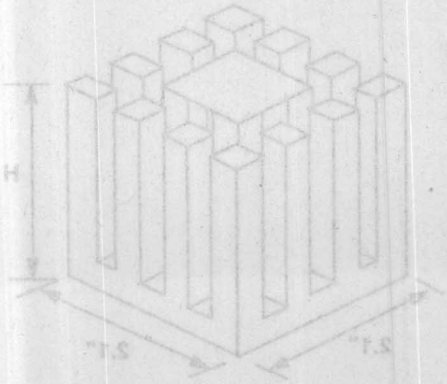
At this point the application note turns from describing the characteristics that define thermal performance to describing how designers should use these characteristics to assess thermal requirements of PC system designs. The Pentium processor specifies a maximum case temperature, T_C, of 70°C @ 66 MHz. This case temperature limit along with the Pentium processor's power and thermal resistance characteristics can be used to determine the ambient temperature required to keep the Pentium processor operating within its specified limits. Using these parameters in the following equations:

$$T_A = T_C - (P^* \theta_{CA})$$

$$T_A = 70°C - (16W^* 10.5°C/W)$$

$$T_A = -98°C$$

The maximum ambient temperature required in a Pentium processor system without any additional thermal enhancement is −98°C at 66 MHz. Obviously, this ambient temperature is impractical and unachievable in a PC system. In order to be able to maintain the case temperature at 70°C in a typical system ambient with air temperature of 40°C to 45°C, the thermal resistance between the case and the ambient must be reduced.



5.1 Heat Sinks

The most common way to improve the package thermal performance is to increase the surface area of the device by attaching a large piece of metal (a heat sink) to the package. The heat sink is usually made of Aluminum and is chosen for its price/thermal-performance ratio. There are materials that offer higher conductivity such as copper, but cost becomes prohibitive. To maximize the flow of heat for a given junction temperature rise over the ambient temperature, the thermal resistance from heat sink to air can be reduced by a) maximizing the surface area, and b) maximizing the air flow across the surface area (maximizing air flow **through** heat sink fins in most cases).

Intel has used test data to determine what size of heat sink and airflow is needed to properly cool a Pentium processor system. The data was derived assuming an adhesive attach process that offers thermal resistance of about 0.2°C/W.

The testing was done in a wind tuunel in the configuration (in Figure 3) where the heat sink was mounted on a real Pentium processor package with a thermal die mounted inside to generate the 16W of power. The package is then mounted in a socket which is soldered to a 2-layer PCB that brings power to the die.

Based on these tests, three specific heat sink and airflow combinations have been identified that properly dissipate the Pentium processor's 16W and maintains a case temperature below 70°C @ 66 MHz. The three heat sinks are shown in Figure 4.

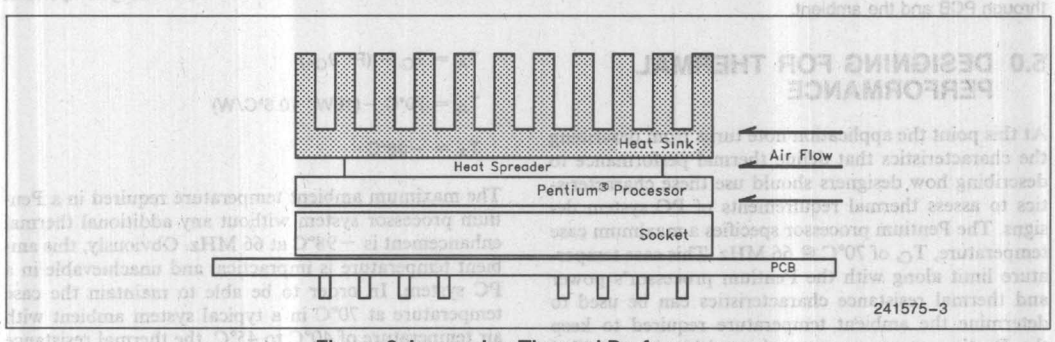


Figure 3. Improving Thermal Performance

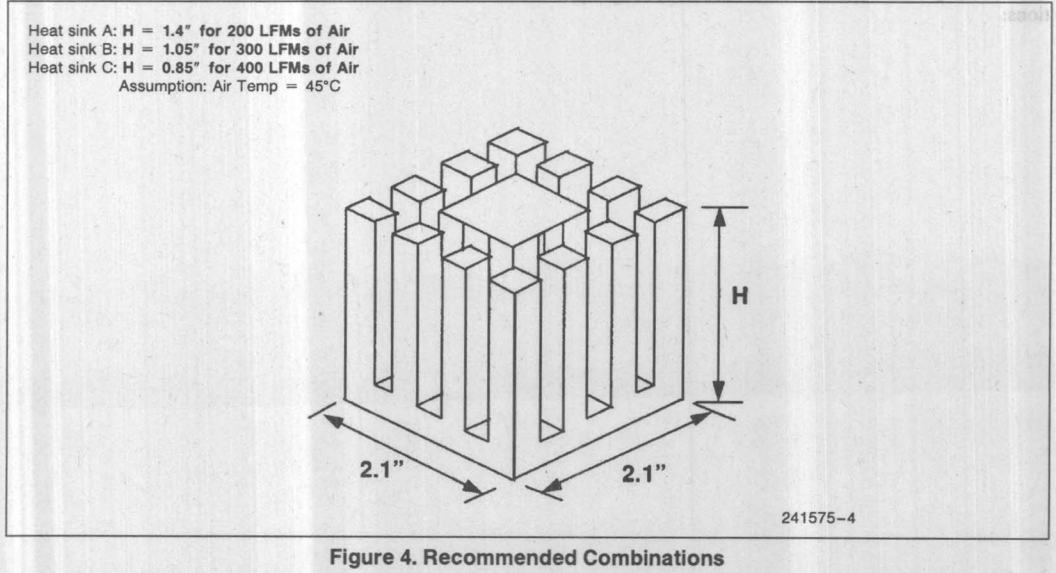


Figure 4. Recommended Combinations

In addition, testing has been done to provide more general guidelines which allow deviating from the above conditions. These guidelines allow systems to derive various combinations of heat sink size and airflow that ensure the Pentium processor thermal specifications are met. For example, by increasing the heat sink x-y dimensions and extending it over the package footprint, the heat sink height can be reduced while maintaining the same thermal performance as the taller heat sink with the same footprint as that of the package. The first three charts (Figures 5, 6, 7) show the thermal resistance as a function of heat sink size and airflow. The last three charts (Figures 8, 9, 10) show the power dissipation achievable with a given heat sink size and airflow. The power dissipation calculations assume T_C = 70°C @ 66 MHz, T_A = 45°C, and θ_{JC} = 0.6°C/W.

$$P_{max} = (T_C - T_A)/\theta_{CA} = 25/\theta_{CA}$$

A key assumption in all of these calculations is that a perfect thermal connection can be achieved between the case and the heat sink. One ban extrapolate the heat sink solutions by adding the additional thermal resistance of any chosen heat sink attach process. See Appendix B for case to heat sink thermal interface options.

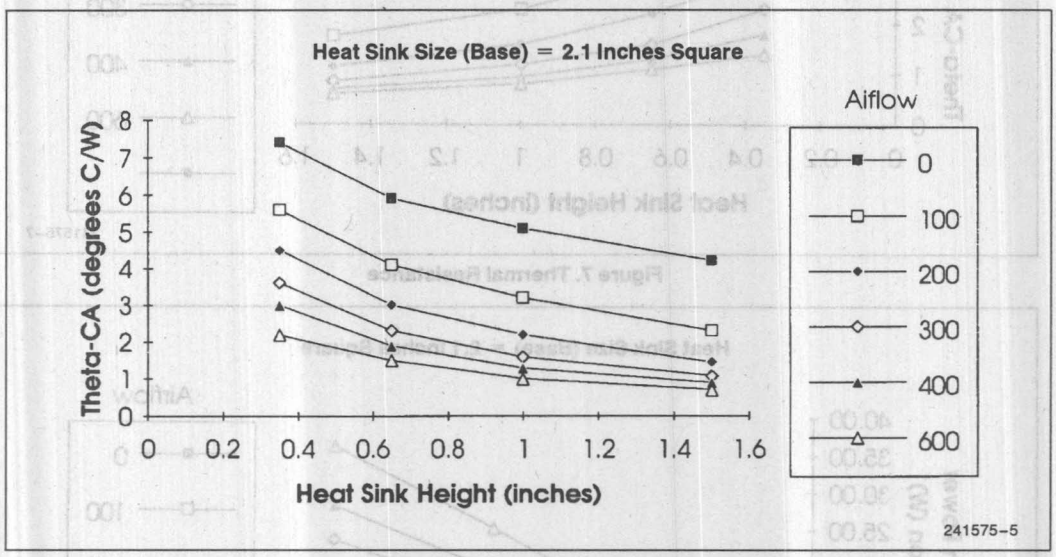


Figure 5. Thermal Resistance

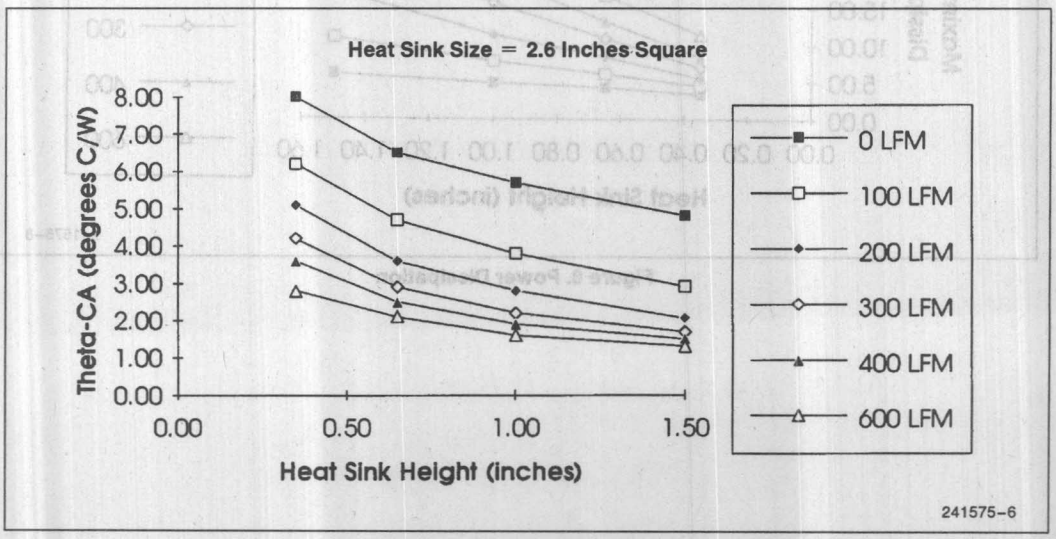


Figure 6. Thermal Resistance

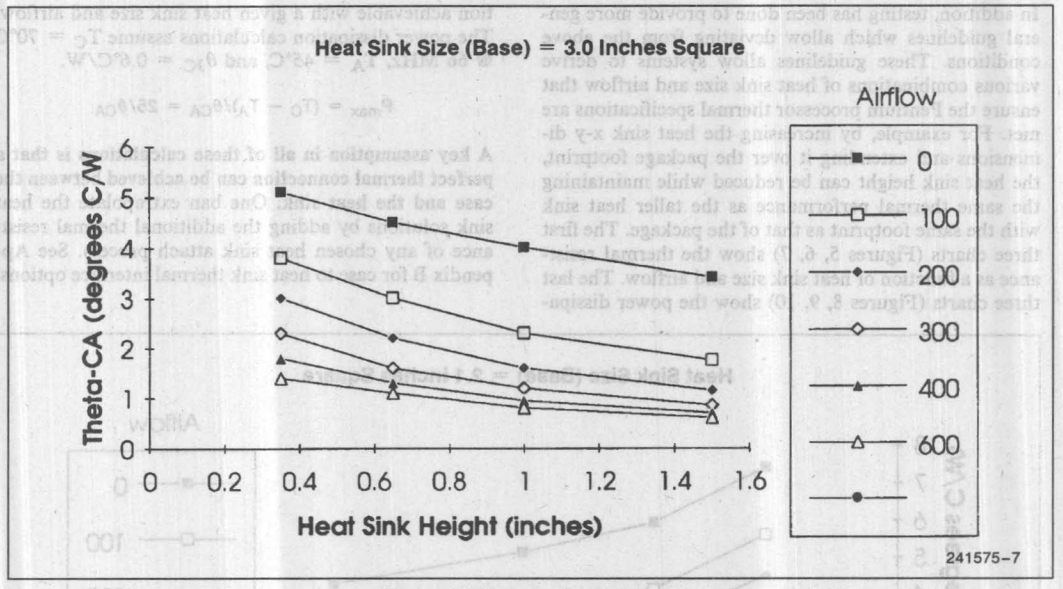


Figure 7. Thermal Resistance

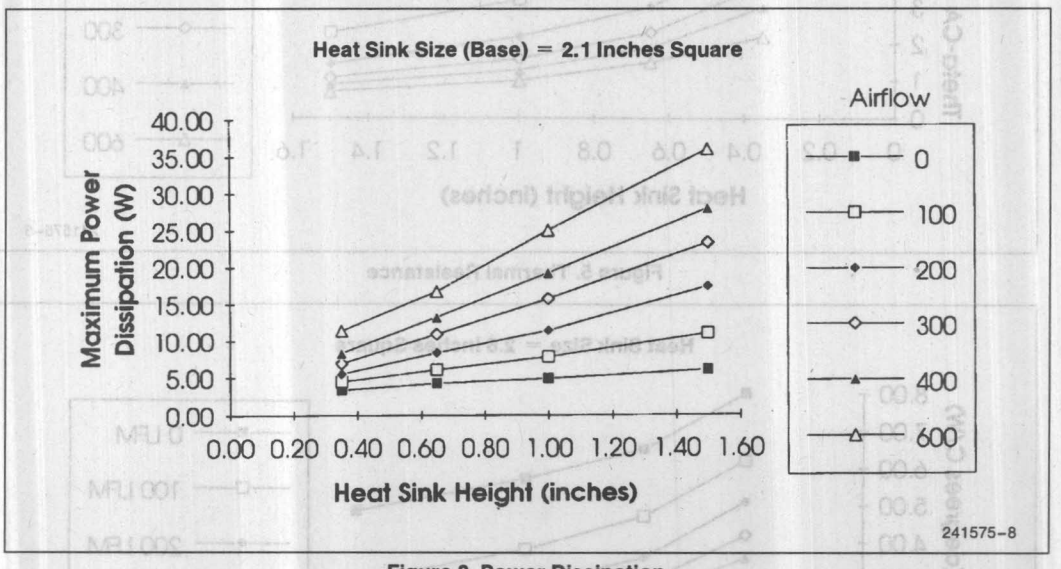


Figure 8. Power Dissipation

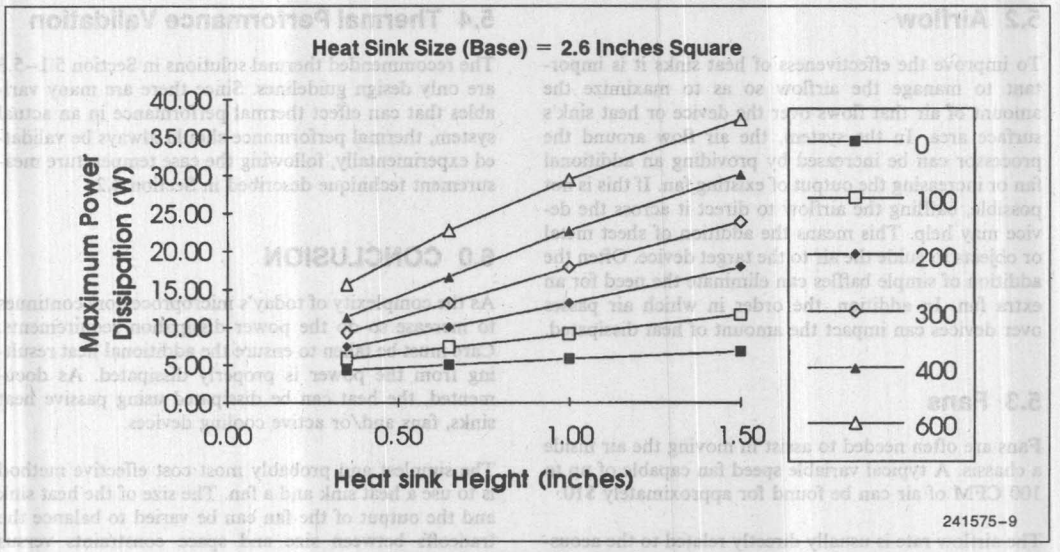


Figure 9. Power Dissipation

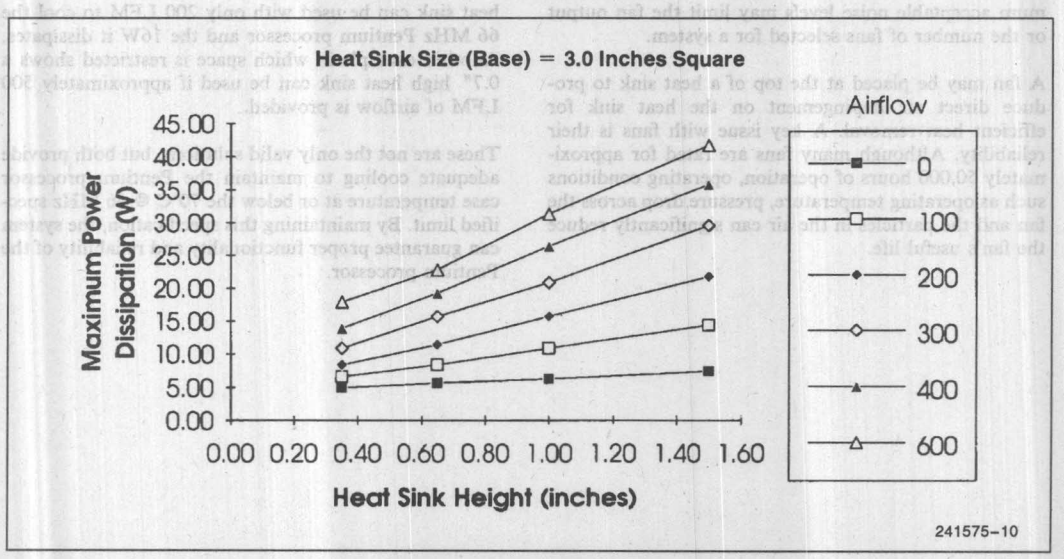


Figure 10. Power Dissipation

5.3 Fans

Fans are often needed to assist in moving the air inside a chassis. A typical variable speed fan capable of up to 100 CFM of air can be found for approximately $10.

The airflow rate is usually directly related to the acoustic noise level of the fan and system. Therefore maximum acceptable noise levels may limit the fan output or the number of fans selected for a system.

A fan may be placed at the top of a heat sink to produce direct air impingement on the heat sink for efficient heat removal. A key issue with fans is their reliability. Although many fans are rated for approximately 50,000 hours of operation, operating conditions such as operating temperature, pressure drop across the fan and the particles in the air can significantly reduce the fan's useful life.

Care must be taken to ensure the additional heat resulting from the power is properly dissipated. As documented, the heat can be dissipated using passive heat sinks, fans and/or active cooling devices.

The simplest and probably most cost effective method is to use a heat sink and a fan. The size of the heat sink and the output of the fan can be varied to balance the tradeoffs between size and space constraints versus noise. For example, if space is available a 1.4″ high heat sink can be used with only 200 LFM to cool the 66 MHz Pentium processor and the 16W it dissipates. Another example in which space is restricted shows a 0.7″ high heat sink can be used if approximately 500 LFM of airflow is provided.

These are not the only valid solutions, but both provide adequate cooling to maintain the Pentium processor case temperature at or below the 70°C @ 66 MHz specified limit. By maintaining this specification, the system can guarantee proper functionality and reliability of the Pentium processor.

APPENDIX A
EXAMPLES

Thermal management examples, designing with the Pentium processor. Using the best known methods.

Appendix Goal

The goal of this appendix is to measure the operating temperatures in a real system versus the wind tunnel laboratory measurements. These experiments are done with heat sinks that are similar to the ones suggested in Section 5.1 of the main document. The thermocouples and attachment methods suggested in Section 4.2 of the main document are also used. The appendix begins by reviewing the variables that the system designer has control over and uses tables to describe thermal resistance in the context of where the system designer can have the most effect The importance of the case to heat sink thermal interface and correct attachment methods are reviewed and different options given. The appendix proceeds to describe the system used for these tests and the tools and equipment needed. The lab set up procedures are discussed in detail and the measurements are presented with comments at the conclusion.

WHAT ARE THE VARIABLES?

Table A-1 shows the cooling options that customers can control when designing a system. From Table A-1 it is obvious that changing the heat sink and air flow are the two most effective ways for a system designer to affect the thermal performance of a system.

Table A-1. Variables

COOLING OPTIONS UNDER CUSTOMER CONTROL	
Variables	**Options for Cooling**
Device	• Use Power Management SW in the System • Clock the Device at a Lower Speed
Heat Sink	• Increase Heat Sink Area, Width or Height • Use Interface Materials with Lower Thermal Resistance • Use Active Cooling Devices • Use a Combination of Active and Passive Cooling Devices
Air Flow	• Increase Air Flow • Manage Air Flow • Place Hottest IC's near Highest Airflow
Ambient Temperature	• Place System in a Controlled Climate

Figure A-1 sums up the thermal tradeoff picture succinctly. Looking at Figure A-1 reiterates the previous statement that increasing the heat sink size and air flow rate provide the largest thermal performance improvements. In addition it shows the variables that are constant. Note that the θ_{JC} (junction-to-case thermal resistance) of the Pentium processor is fixed and a system designer can have no effect on this parameter. Also note that the θ_{CS} (case-to-heat sink thermal resistance) is a constant. Even though θ_{CS} is shown as a constant in Figure A-1 it can move up and down the Y axis depending on the interface material chosen. The case to heat sink interface is critical to the overall success of the thermal solution and cannot be overlooked. The next section will go into detail on this subject.

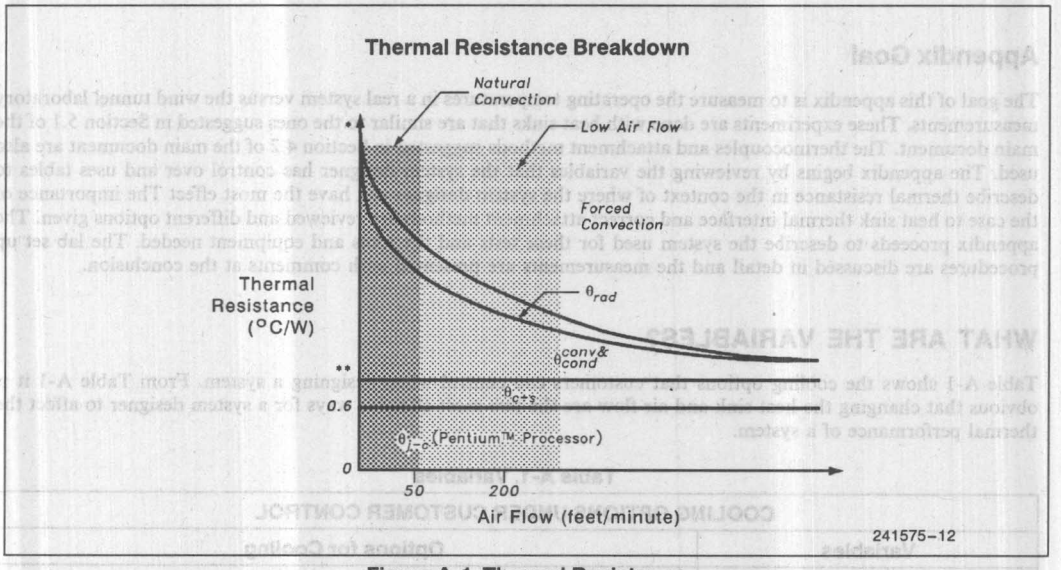


Figure A-1. Thermal Resistance

The main of purpose Figure A-2 is to show that packages and heat sinks are not perfectly flat and this requires that the air gap be filled with an interface material that has a lower thermal resistance than air. The whole point is to try and minimize the contact thermal resistance. The different types of thermal interface materials are listed to show the wide array of materials available to the system designer. Intel's data books have a mechanical section that list the flatness of the package. Heat sink vendors should be able to provide specifications for their heat sink offerings.

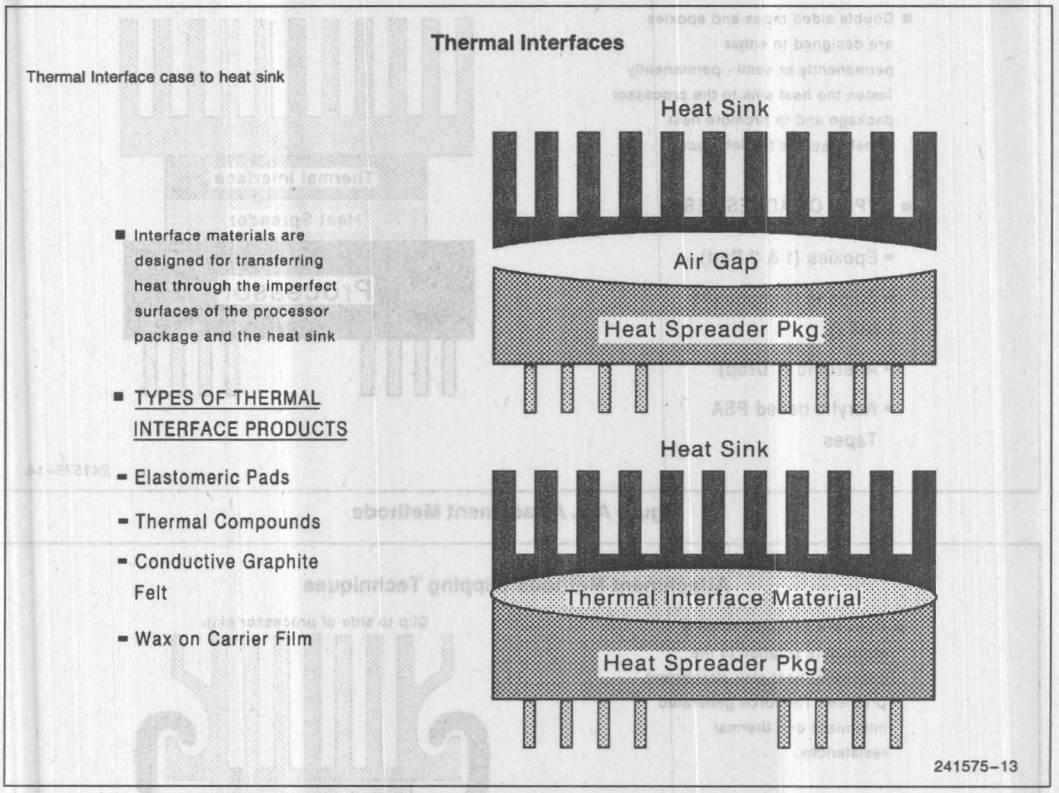


Figure A-2. Thermal Interfaces

The next section (Figures A-3 through A-5) covers attachment methods which generally fall into the categories shown; epoxies, double sided tapes or manual clips to either chip or socket.

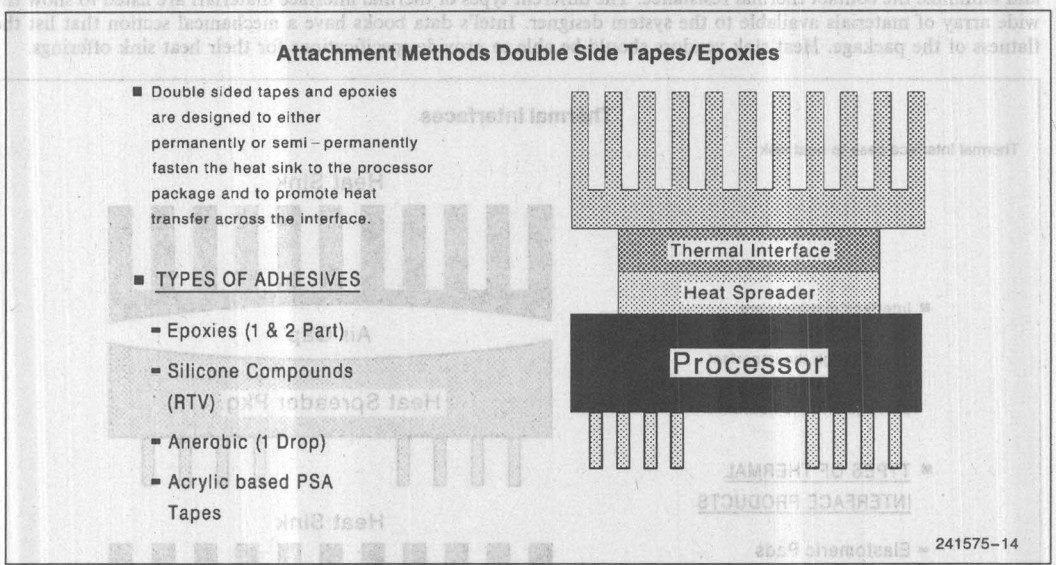


Figure A-3. Attachment Methods

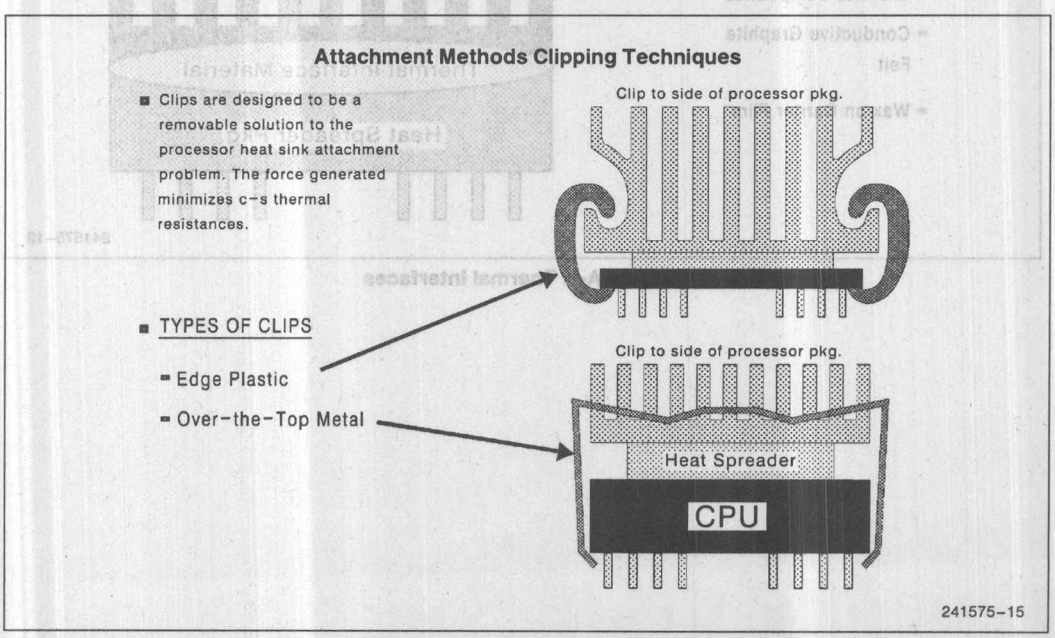


Figure A-4. Attachment Methods

Note that some clips don't allow the package to be pushed all the way into the socket and this could be a problem with short lead packages. The main advantage of this type of system is that a low profile socket can be used to lower the height of the processor heat sink assembly.

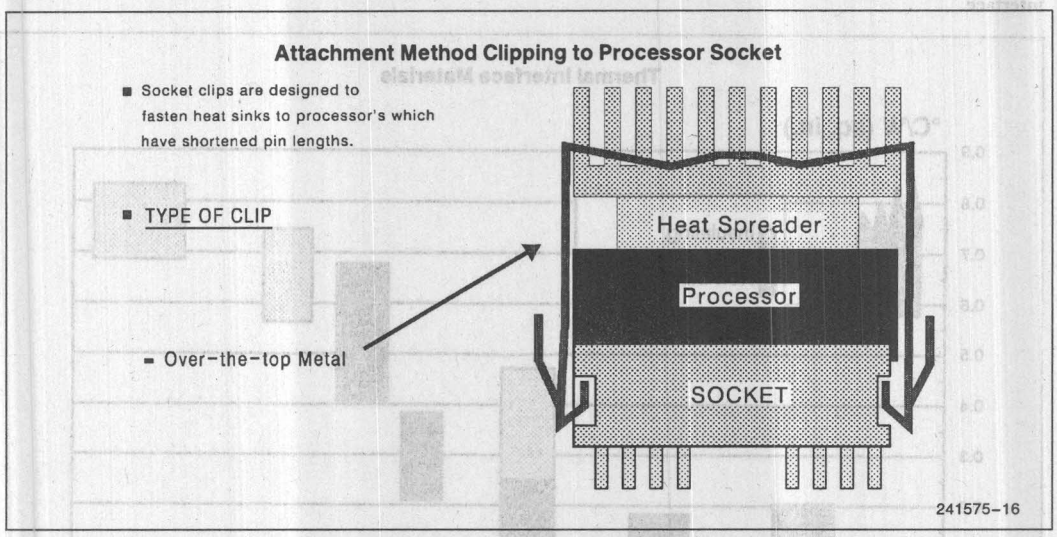


Figure A-5. Attachment Methods

Table A-2 lists pros and cons of the different attachment methods covered.

Table A-2. Attachment Methods

ATTACHMENT METHODS	ADVANTAGES	DISADVANTAGES
DOUBLE SIDED TAPES	• Quick to Use • Low Installed Cost • Compliant	• High Thermal Resistance • Requires Flat Interfaces • Assembly Contact Pressure
EPOXIES	• Low Potential Thermal Resistance • Low Contact Pressure	• Mixing, Curing, Messy • Timing Consuming (if not automated) • CTE Stress, High Rigidity • Variable Thickness (theta)
CLIPS	• Centralized Pressure Points • Removable • Easily Installed • Solution to Upgrade • Accommodates Wide Tolerance	• Removable • Force Limits vs Assembly • Insufficient Shock and Vibration Data • Potential for Loss of Pressure

The materials chart Figure A-6 shows the performance of each type of thermal interface material. Note that even though thermal grease has a deserved reputation for being messy and harder to control it still performs well as a thermal interface. All the examples that are shown in Appendix A use thermal grease as the case to heat sink interface.

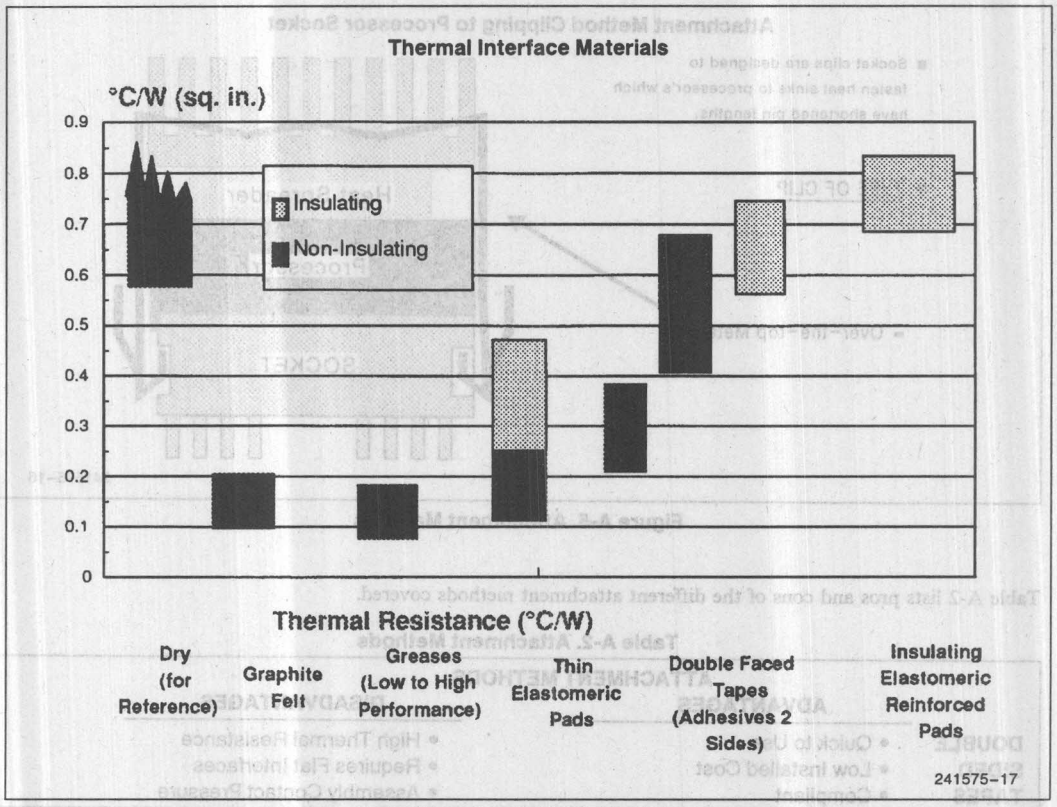


Figure A-6. Materials

The next step is to chose a heat sink. Figure A-7 shows the wide range of choices and the cost associated with each technology.

Now that all the variables and options are known for this problem we can proceed on to do some real system measurements using the recommendations and data shown in the first part of this application note.

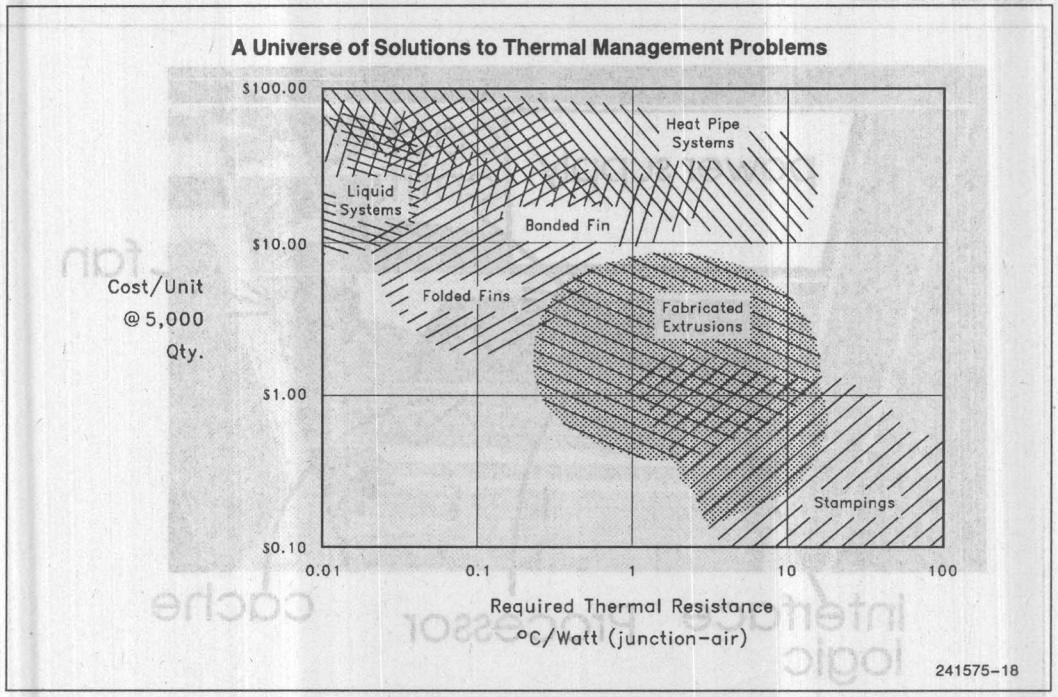


Figure A-7. Solutions

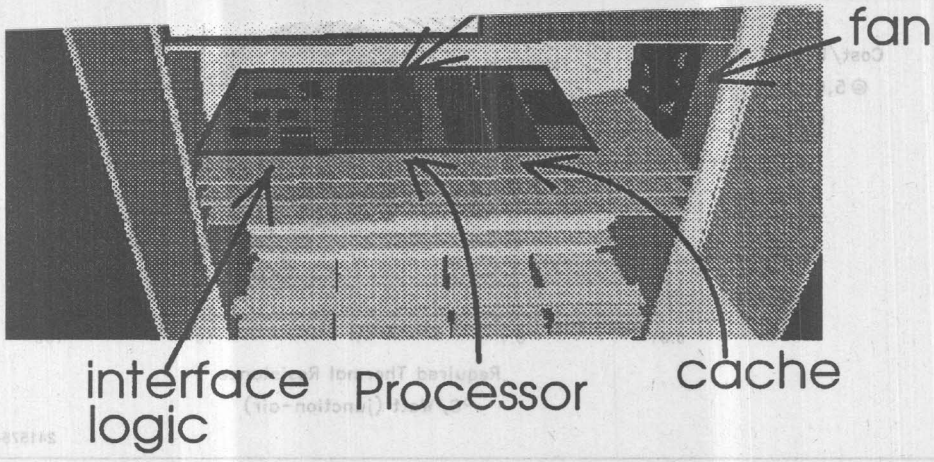


Figure A-8. Pentium® Processor System

Objectives

- To measure a Pentium processor system operating under real working conditions.
- To compare the measured results to the predicted results shown in the beginning of this application note. The reader should always keep the main goal in mind; **the main goal is always to meet the case temperature specification for the Pentium processor**. Any combination of heat sink and air flow rate is fine as long as the case temperature specification is met. The heat sinks used in test #1 thru #4 will match the suggested heat sinks as close as possible to accurately correlate with the wind tunnel data. This is meant to illustrate how a system designer might start by using the suggested heat sinks and air flow rates as starting points to thermally tune their particular system. Test #5 uses a heat sink and a fan combination. The fan heat sink is best described as a fan attached directly to the heat sink on the Pentium processor. It is an active device used for spot cooling ICs. We will concentrate on traditional passive heat sink solutions with only one set of measurements being done for a fan heat sink assembly.

Tools and Equipment

1. Pentium processor-based system running at 40 MHz.
2. Hot wire anemometer to measure airflow rate.
3. Thermocouples and high thermal conductivity cement as recommended in the application note.
4. Homemade jig for accurate and repeatable attachment of the thermocouples to the package.
5. Homemade power supply isolation socket for setting the V_{CC} and reading the I_{CC} of the processor independently of the rest of the system.
6. Adjustable power supply with adequate current capabilities and both current and voltage read out.
7. Multimeter to read the voltage and current.
8. Cables to connect everything up.
9. Software test suite that simulates "worst case conditions for a typical real application." In this case it was Microsoft Excel and Word for Windows test suites.
10. Drill and drill bits.
11. Thermal grease.

The lab procedure was as follows:

Preparing the System

1. Load the test software on the system disk (or floppy) and make sure everything runs correctly before you start. After everything works satisfactorily proceed to the next step.
2. Remove the covers, choose several places (random) around the processor to measure the air flow of the system. Then drill holes large enough to allow the anemometer to be inserted. Five holes were drilled in the system cover.
3. In this case we had a 12″ long ¼″ diameter directional anemometer. To get more repeatable measurements the shaft of the probe was marked with a pencil to get the same depth, into the box, for each measurement
4. We then removed the processor card from the chassis (use anti-static procedures to prevent IC damage).
5. Remove the Pentium processor from the card and install the isolation socket.

Preparing the Pentium Processor for Testing

1. Using the jig carefully attach the thermocouple to the center of the processor package using cement and let it cure as recommended by the manufacturer of the cement.
2. Drill holes no larger than 0.125″ in the centers of the heat sinks to be tested just large enough to get the thermocouple wires through the hole. In the case of the fan heat sink, the fan was removed and the heat sink was drilled the same as the others and then re-assembled. Each of the holes were counter sunk on the bottom to better conform to the tear drop shape the thermocouple and cement naturally forms into. The idea is to not disturb or break the contact between the cement and the package. If it is broken or cracked the measurements will be incorrect
3. Apply the thermal grease (less than 0.004″ thick) evenly, with no voids, to the processor package.
4. Slide the heat sink down the thermocouple wires being careful not to disturb the thermocouple while at the same time firmly seating the heat sink to the package. Attach the plug for the temperature meter to the other end of the thermocouple wire terminals.
5. Re-install the processor/thermocouple/heat sink assembly into the isolation socket on the processor board, again being careful not to disturb the thermocouple connection.

Preparing for Measurements

1. Re-install the processor card into the system.
2. Connect the power supply wires to the power supply and the isolation socket.
3. Connect the multimeter to the the power supply to monitor the V_{CC} and set the power supply meter to measure I_{CC}.
4. Connect the thermocouple to the meter.
5. Turn on the processor power supply and then the system supply.
6. Wait for the system to boot and then run the test software.

Thermal Measurements

The next step was to determine the baseline airflow in the system without a heat sink attached to the processor. Measure the airflow at several locations using the access holes in the system and the marks on the probe to ensure accurate placement of the probe and repeatability of the measurements. Table A-3 shows the results. Be cautious when placing the fan in a system relative to the processor. All fans have a dead spot (low airflow) in the center of the fan. Avoid the dead spot. Even several inches away from the fan the dead spot can influence airflow considerably.

Test #1

The next step is to compare how close the suggested values and tables are to the measured results. Use the formulas described in the beginning of the application note and the values from Table A-4.

$$P_D = V_{CC} * I_{CC} = (1.82*4.89) = 8.827W$$

$$\theta_{JC} = (T_J - T_C)/P_D = 0.6$$

$$\theta_{JA} = (T_J - T_A)/P_D$$

$$\theta_{CA} = \theta_{JA} - \theta_{JC} = [(T_J - T_A) - (T_J - T_C)]/P_D = [T_C - T_A]/P_D$$

$$\theta_{CA} = (55.3 - 29)/(1.8*4.85) = 24/8.827 = 2.97$$

θ_{CA} = 2.7°C/W is the measured value in the system for this configuration.

Table A-3. Baseline Airflow

Airflow Measured, LFM	120–160
Location of probe	~ 2 inches (upstream from the fan) @ center of the processor (above the heat sink)

Table A-4. Test Conditions Test #1

Heat Sink Size, Inches H x W	Temperature, degrees C			I_{CC} Amps	V_{CC} Volts	Air Flow LFM
	Room T_A	System T_A	Case T_C			
1.2 x 2.1 sq.	23	29	55.3	1.82	4.85	100–150

The graph (Figure A-9) from the application note, for heat sink size size of 2.1" x 2.1", is used to compare the predicted θ_{CA}, for a 1.2" tall heat sink, to the measured value of θ_{CA}.

The predictions from the graph (Figure A-9) are:

θ_{CA} = 2.9°C/W @ 100 LFM

θ_{CA} = 2.4°C/W @ 150 LFM

θ_{CA} = 1.9°C/W @ 200 LFM

And the measured value is:

θ_{CA} = 2.97°C/W @ 100–150 LFM

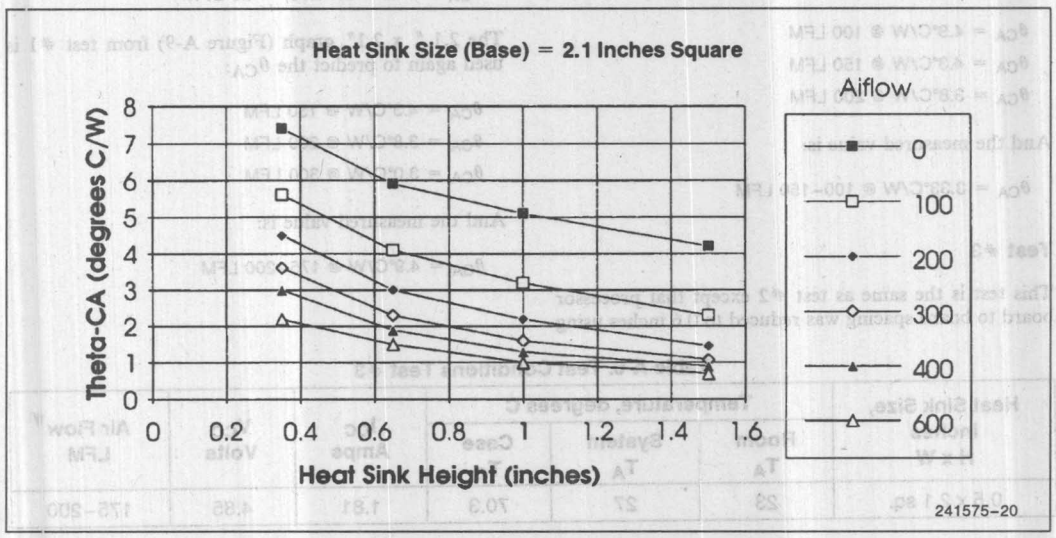


Figure A-9. Thermal Resistance

Table A-5. Test Conditions Test #2

Heat Sink Size, Inches H x W	Temperature, degrees C			I_{CC} Amps	V_{CC} Volts	Air Flow LFM
	Room T_A	System T_A	Case T_C			
0.5 x 2.1 sq.	22	29	58.3	1.81	4.85	100–150

Test #2

The same test only the heat sink height was reduced to 0.5 inch height.

$\theta_{CA} = (T_C - T_A)/P_D$

$\theta_{CA} = 58.3 - 29/8.79 = 3.33°C/W$

The 2. 1" x 2.1" graph (Figure A-9) from test #1 is used again and it predicts:

$\theta_{CA} = 4.9°C/W$ @ 100 LFM

$\theta_{CA} = 4.3°C/W$ @ 150 LFM

$\theta_{CA} = 3.8°C/W$ @ 200 LFM

And the measured value is:

$\theta_{CA} = 3.33°C/W$ @ 100–150 LFM

Test #3

This test is the same as test #2 except that processor board to board spacing was reduced to 0.6 inches using a cardboard baffle to simulate a system with very tight board spacing. An existing system that is upgrading from an Intel 486 processor to the Pentium processor might have this type of spacing. Note that this particular configuration actually has more airflow than test #2. It could have just as easily been lower. It all depends on the particular system being measured.

$\theta_{CA} = (T_C - T_A)/P_D$

$\theta_{CA} = 70.3 - 27/8.79 = 4.9°C/W$

The 2.1 " x 2.1" graph (Figure A-9) from test #1 is used again to predict the θ_{CA}:

$\theta_{CA} = 4.3°C/W$ @ 150 LFM

$\theta_{CA} = 3.8°C/W$ @ 200 LFM

$\theta_{CA} = 3.0°C/W$ @ 300 LFM

And the measured value is:

$\theta_{CA} = 4.9°C/W$ @ 175–200 LFM

Table A-6. Test Conditions Test #3

Heat Sink Size, Inches H x W	Temperature, degrees C			I_{CC} Amps	V_{CC} Volts	Air Flow LFM
	Room T_A	System T_A	Case T_C			
0.5 x 2.1 sq.	23	27	70.3	1.81	4.85	175–200

Table A-7. Test Conditions Test #4

Heat Sink Size, Inches H x W	Temperature, degrees C			I_{CC} Amps	V_{CC} Volts	Air Flow LFM
	Room T_A	System T_A	Case T_C			
0.65 x 3.1 sq.	23	29	55.3	1.8	4.85	100–140

Test #4

This test uses a 0.65″ tall heat sink that is 3.1″ sq. This type of heat sink might be used when height is limited and there is room to spread out by adding more area to the heat sink base.

$\theta_{CA} = (T_C - T_A)/P_D$

$\theta_{CA} = (55.3 - 29)/8.73 = 3.0$

The 3.0″ x 3.0″ graph (Figure A-10) from the application note is used since it is similar to the heat sink used. The 3.0″ x 3.0″ graph predicts:

θ_{CA} = 3.0°C/W @ 100 LFM

θ_{CA} = 2.6°C/W @ 150 LFM

And the measured value is:

θ_{CA} = 3.0°C/W @ 100–140 LFM

Test #5

The last test was done using a fan/heat sink assembly that has become popular for prototyping, debug and spot cooling in some situations. We were not able to measure the airflow on the processor with this configuration because the air flow is not directional enough to get a reading with the probe available. The case temperature however was monitored by mounting a thermocouple in the same manner used above. We did modify the setup by bringing the thermocouple wires out the side to clear the fan. This will change the measurements the thermocouple produces and should be factored into any data. We do not have any wind tunnel data on the fan/heat sink combination. Note that the case temperature is within specification.

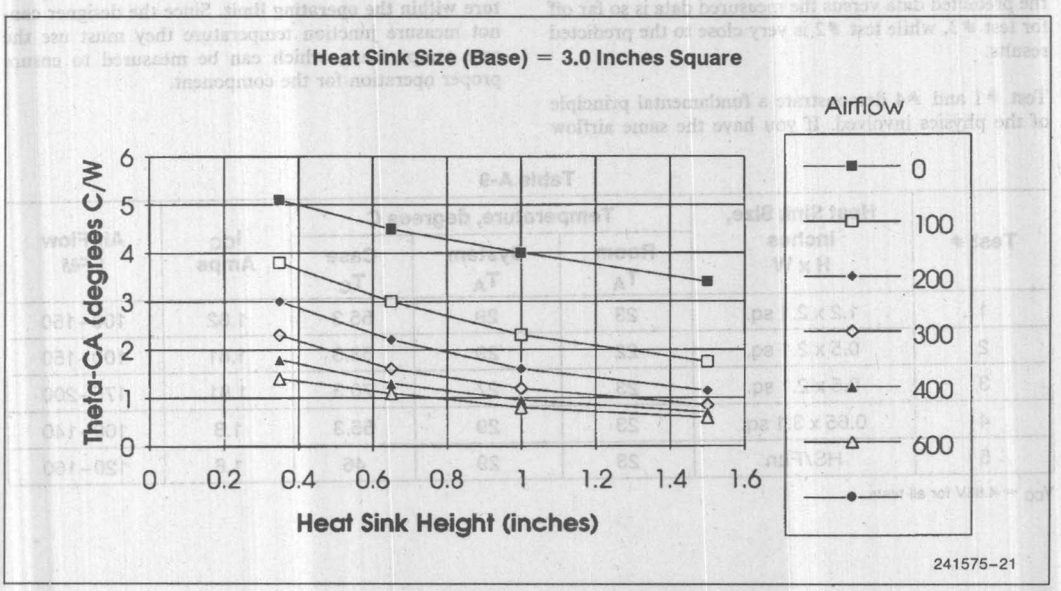


Figure A-10. Thermal Resistance

Table A-8. Test Conditions Test #5

Heat Sink Size, Inches H x W	Temperature, degrees C			I_{CC} Amps	V_{CC} Volts	Air Flow LFM
	Room T_A	System T_A	Case T_C			
HS/Fan	23	29	46	1.8	4.85	120–160

Conclusion

Table A-9 shows all the tests in one table. The data shows that the suggestions in the application note are a very good starting point to begin tuning any Pentium processor system and that there is no one cookbook answer that fits all systems because of the complexity of air flow and variations from each type of system. Indeed the results show that airflow can be changed dramatically even in the same system by changing one variable. For example test #2 and #3 are exactly the same except that board to board spacing was reduced significantly. Note that case temperature rose significantly even though the airflow sensor was reading a higher value. This suggests that the airflow through the heat sink was lower even though the anemometer, 2 inches away, was reading higher airflow at its position. Note also that test #2 more closely approximates the wind tunnel test setup because it has open space above the board instead of a board nearby. This is also why the predicted data versus the measured data is so far off for test #3, while test #2 is very close to the predicted results.

Test #1 and #4 demonstrate a fundamental principle of the physics involved. If you have the same airflow and must reduce the height of the heat sink, you have to spread out the area of the heat sink to compensate for the reduced height. Test #1 uses a 1.2″ height heat sink that is the same size as the package. Test #4 was able to produce the same case temperature with a shorter heat sink and more area.

Test #5 demonstrates that a fan/heat sink assembly can spot cool effectively if you have enough space above and around it to allow the required back pressure. This is the only active device tested. If you look back at the "A Universe of Solutions to Thermal Management Problems" (Figure A-7) chart you will see the reason why. While the Pentium processor is at the outer envelope of passive cooling, this method of cooling still offers lower cost, power usage and reliability in most cases.

Most of all the system designer should **never lose sight of the real goal which is to keep the junction temperature within the operating limit**. Since the designer cannot measure junction temperature they must use the case temperature, which can be measured to ensure proper operation for the component.

Table A-9

Test #	Heat Sink Size, Inches H x W	Temperature, degrees C			I_{CC} Amps	Air Flow LFM
		Room T_A	System T_A	Case T_C		
1	1.2 x 2.1 sq.	23	29	55.3	1.82	100–150
2	0.5 x 2.1 sq.	22	29	58.3	1.81	100–150
3	0.5 x 2.1 sq.	23	27	70.3	1.81	175–200
4	0.65 x 3.1 sq.	23	29	55.3	1.8	100–140
5	HS/Fan	23	29	46	1.8	120–160

V_{CC} = 4.85V for all tests.

APPENDIX B
HEAT SINK VENDORS

Aavid Engineering
One Kool Path
P.O. Box 400
Laconia, NH 03247
(603) 528-3400
(603) 525-1478 (FAX)
Contact: Gary F. Kuzmin (Product Marketing Manager)

EG&G Wakefield Engineering
60 Audubon Rd.
Wakefield, MA 01880
(617) 245-5900
(617) 246-0874 (FAX)
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135 W. Magnolia Blvd.
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Thermalloy
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Dallas, TX 75234-8993
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APPENDIX B
HEAT SINK VENDORS

Aavid Engineering
One Kool Path
P.O. Box 400
Laconia, NH 03247
(603) 528-3400
(603) 525-1478 (FAX)
Contact: Gary P. Kuzmin (Product Marketing Manager)

EOS&D Wakefield Engineering
60 Audubon Rd.
Wakefield, MA 01880
(617) 246-2900
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Pentium® Processor Clock Design

November 1995

Order Number: 241574-002

intel

AP-479

APPLICATION
NOTE

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November 1995

Order Number: 241574-002

1.0 INTRODUCTION

Today's high speed microprocessors place a heavy demand on clock generation and distribution. To maintain a synchronous system, well-controlled and precise clocking solutions are required. Pentium® processor, with operating frequencies of 60 MHz and 66 MHz, has tight system clock specifications. In order to bring clock signals of acceptable quality and minimal skew to the Pentium processor and the rest of the system, system designers have to contend with high speed issues for clock distribution and limited number of precise clock driver devices. In this application note, the key issues in the design of a 60 MHz or 66 MHz clock for a Pentium processor-based system will be discussed, available clock drivers will be listed and discussed, and detailed design examples of a clock solution for the Pentium processor with 256K second-level cache subsystem, using the 82496 Cache Controller and the 82491 Cache SRAMs, are provided.

The Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM form a CPU-Cache core or chip set. Along with a memory bus controller (MBC), the chip set provides a CPU-like interface for many types of memory buses.

This application note is intended for system designers concerned with clock generation and distribution for the Pentium processor and CPU-Cache chip set based systems. It reflects data collected from several quarters of characterization of the Pentium processor and experience with some of the clock driver devices, as well. This application note gives readers a good understanding of the issues and solutions of high speed clocking, particularly that for the Pentium processor. The reader should be familiar with the Pentium processor and CPU-Cache chip set electrical and mechanical specifications, *Clock Design in 50 MHz Intel486™Systems*, and transmission line theory. If not, please read materials listed in Section 9.0 before proceeding.

1.1 General Clocking Issues

There are two major problems with distributing clock signals at 66 MHz: clock signal quality and clock skew. At high speed, one set of effects which has been minor in slower designs is now significant—the effects of transmission line. At high frequencies and fast edge rates, long traces behave like transmission lines. The "lumped" circuit assumption which assumes instantaneous signal transmission is no longer valid. Instead, signals travel in a finite time. When a transmission line is not properly terminated, one can observe severe overshoot, undershoot and ringback, all of which degrade logical signals. Bad signal quality can cause false switching or multiple switching, and can in extreme cases damage the devices. To maintain a clean clock signal, designers must consider clock driver characteristics, signal routing, load characteristics, and transmission line termination.

There are four basic ways to terminate a transmission line, series, parallel, Thevenin, and AC terminations (Figure 1). Series termination is recommended when driver output impedance is less than the transmission line characteristic impedance (true for most TTL drivers) and the line is driving a small number of devices. Series termination consumes low power and uses only one device; however, the termination method increases signal rise and fall times. Series termination ensures good signal quality by eliminating secondary reflection off the driver end. The rest of the termination methods eliminate reflection at the load end. All of the termination methods can provide good, clean clock signals at the load. Both parallel and Thevenin terminations consume a large amount of power. Thevenin termination consumes less power than parallel but requires one more device. AC termination consumes low power but adds capacitive load to the driver and delay due to RC time constant. Design examples provided with this application note use series termination. For more information on transmission line effects and design issues, please refer to [ref. 3, ref. 4, ref. 5]

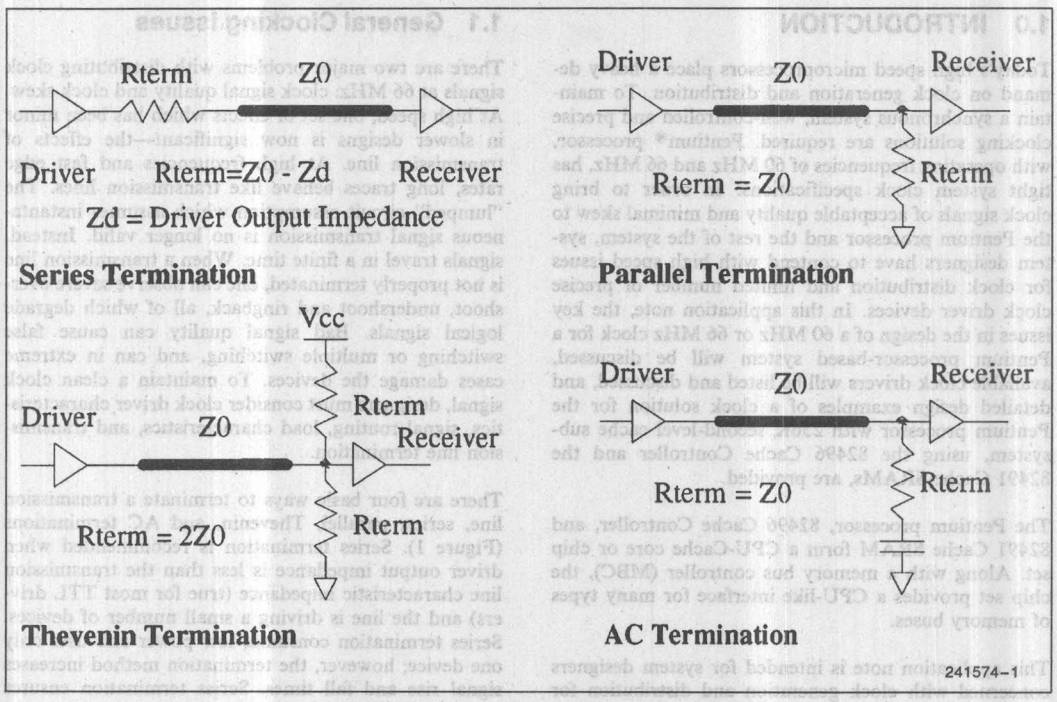


Figure 1. Common Termination Techniques

Skew is defined as the time difference between when the clock signal reaches each component. As frequency increases, there is less and less time for computation in a given clock period for a synchronous design. For a typical design, the time from one rising edge to the next is composed of the largest path-delay, setup time, propagational delay through logic elements, and skew. Clock skew then, takes away from the time available for propagational delay, thereby restricting the amount of logic done in a clock cycle. For high speed designs, skew must be minimized.

To minimize skew, designers must tune clock traces so that the propagational delay from driver through each trace to load is the same for each load. For balanced loads, tuned traces have same lengths. For unbalanced loads, trace lengths can be adjusted to make up for loading differences. If possible, designers should try to keep the loading on each clock line the same.

2.0 PENTIUM® PROCESSOR, 82496 AND 82491 SYSTEM CLOCK SPECIFICATIONS

System clock specifications can be divided into 2 categories: signal quality requirements and skew specifications. Clock signal quality requirements are the same for the Pentium processor and CPU-Cache chip set. Skew specifications are only required for CPU-Cache chip set.

Signal quality requirements define boundaries for acceptable signal shapes and levels. There are two parts to signal quality requirements: signal quality specifications (Table 1) and guidelines (Table 2). Please refer to the latest revision of the Pentium processor and CPU-Cache chip set specifications for more details and for the most up-to-date information.

Table 1. Clock Signal Quality Specifications

Symbol (5)	Parameter	Minimum	Maximum	Unit	Notes
	CLK Frequency	33.33	66.66	MHz	(1)
t2	CLK Period	15		ns	
t3	CLK High Time	4		ns	(2)
t4	CLK Low Time	4		ns	(3)
t5	CLK Rise Time	0.15	1.5	ns	(4)
t6	CLK Fall Time	0.15	1.5	ns	(4)
	CLK Stability		±250	ps	(6), (7), (8), (9)
	V_{IH}	2	V_{CC} + 0.3	V	
	V_{IL}	−0.3	0.8	V	

NOTES:
1. Below 66 MHz only functionality is guaranteed.
2. High times are measured between 2.0V crossing points.
3. Low times are measured between 0.8V crossing points.
4. Rise and fall times are measured between 0.8V and 2.0V.
5. Symbols in Figure 2.
6. Functionality is guaranteed by design/characterization.
7. Measured on rising edge of adjacent CLKs at 1.5V.
8. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency.
9. The amount of jitter present must be accounted for as a component of CLK skew between devices.

Table 2. Clock Signal Quality Guidelines

Parameter	Maximum	Unit	Notes
Overshoot	1.6	V	(1)
Undershoot	1.6	V	(1)
Ringback	0.8	V	(2)

NOTES:
1. Overshoot (undershoot) is the absolute value of the maximum voltage above V_{CC} (or below V_{SS}). The guideline assumes the absence of diodes on the input.
2. Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC} (or above V_{SS}) relative to V_{CC} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

The overshoot guideline should be used in simulations, without diodes present, to ensure overshoot (undershoot) is within the acceptable range. The ringback guideline is provided for verification in an actual system. System designers do not have to worry about ringback if the signal does not overshoot or undershoot, respectively. Figure 2 summarizes clock waveform requirements listed in Table 1.

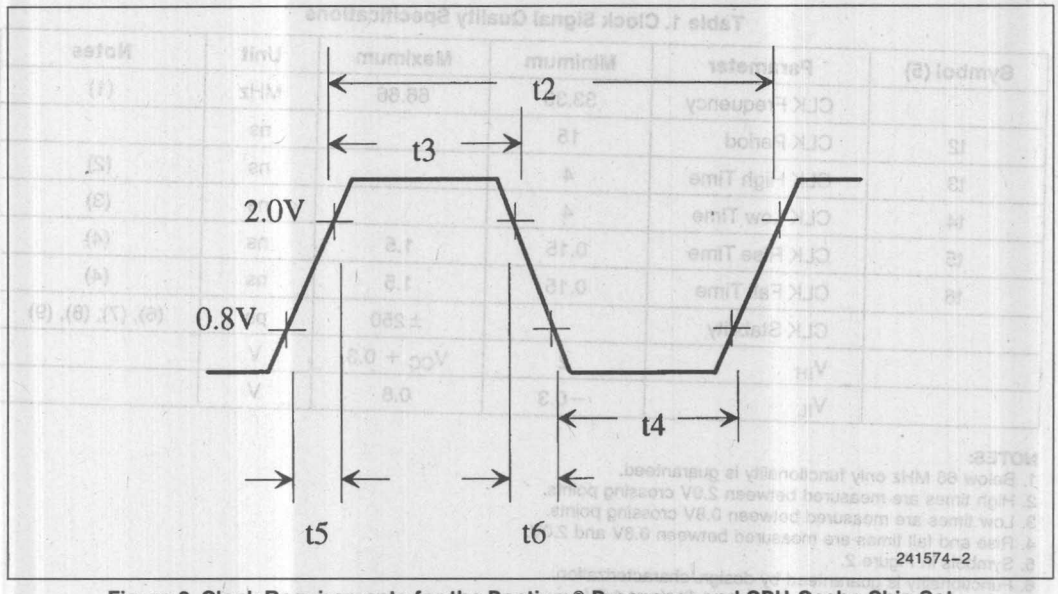


Figure 2. Clock Requirements for the Pentium® Processor and CPU-Cache Chip Set

Figure 3 to Figure 5 illustrates examples of acceptable and unacceptable clock waveforms. Waveform in Figure 3 is for an input model without diodes. Waveform in Figure 4 is for an input model with diodes. The diodes clamp the voltage and prevent it from going more than a diode drop above V_{CC} or below V_{SS}. Waveform in Figure 5 is for an input model without diodes. The waveform is not acceptable for several reasons. It violates the minimum low time specification (4 ns), the maximum fall time specification (1.5 ns), and it does not follow the maximum undershoot guideline (1.6V).

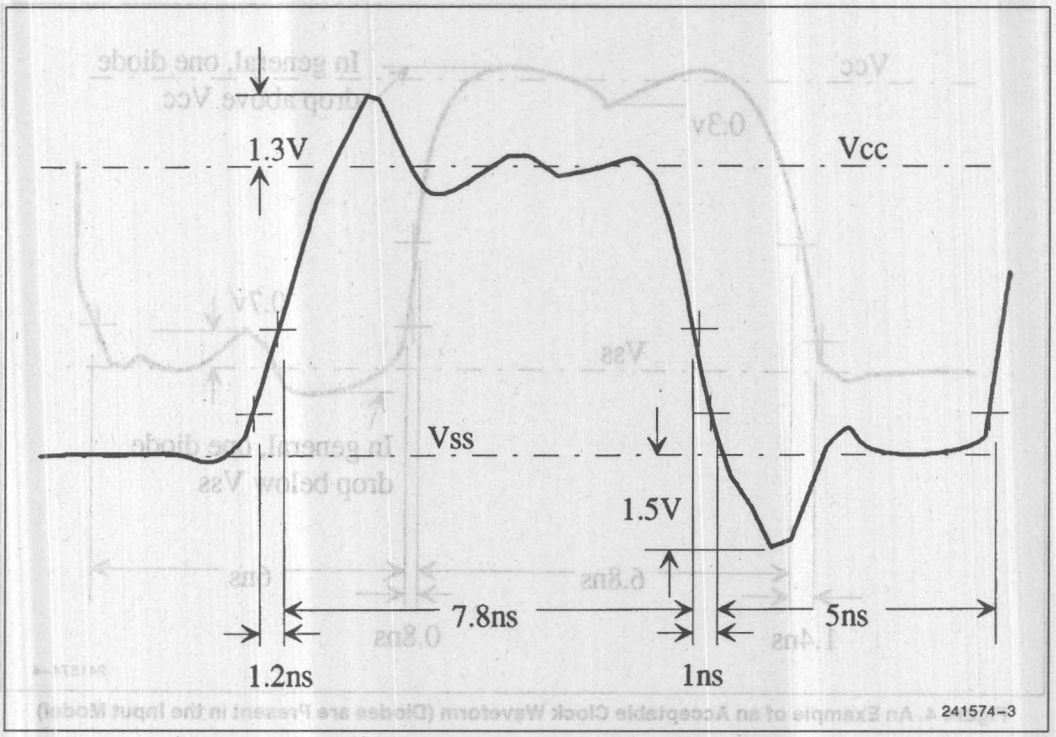


Figure 3. An Example of an Acceptable Clock Waveform (Diodes are Absent from the Input Model)

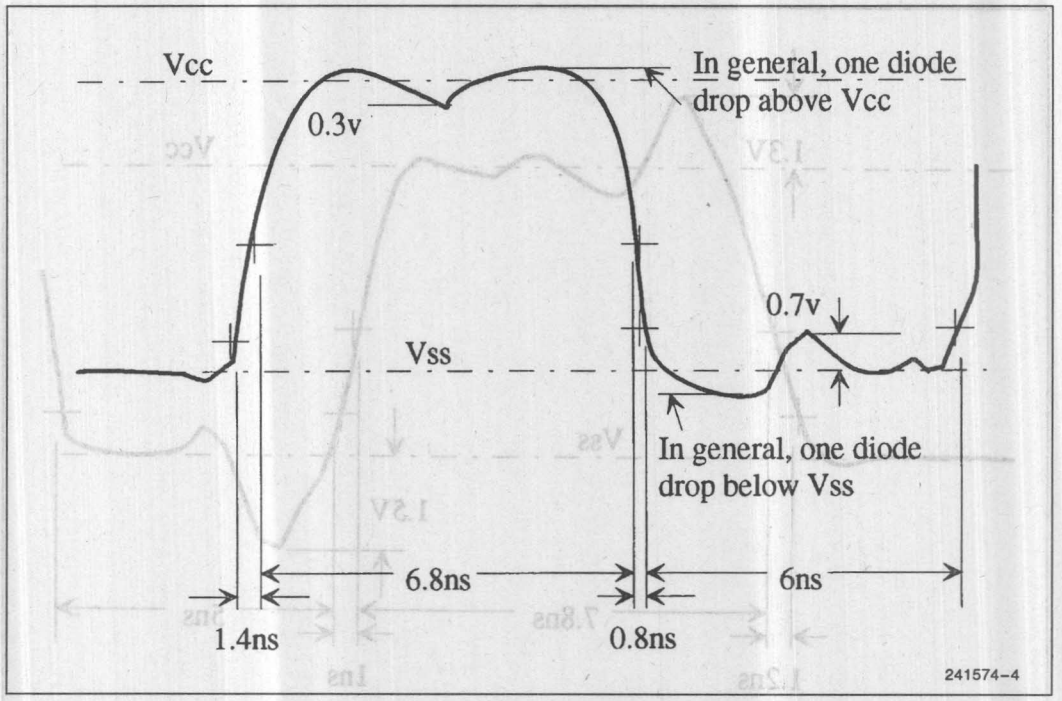


Figure 4. An Example of an Acceptable Clock Waveform (Diodes are Present in the Input Model)

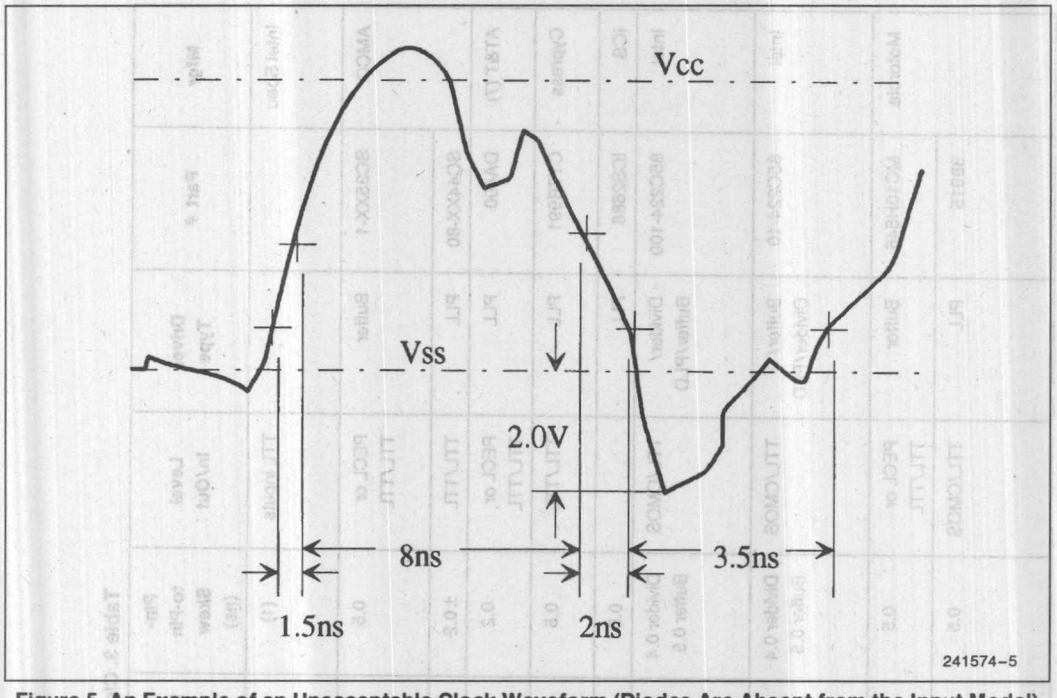


Figure 5. An Example of an Unacceptable Clock Waveform (Diodes Are Absent from the Input Model)

Clock skews for the CPU-Cache chip set are measured at 0.8V, 1.5V, and 2.0V on the rising edge. Worst case skew between the Pentium processor and the 82496 is 0.2 ns, and worst case skew between any 82491 and either the Pentium processor or the 82496 is 0.7 ns.

3.0 AVAILABLE CLOCK DRIVERS

Intel has held discussions with many clock driver component companies. The intent has been to enable these companies to offer clock driver solutions that meet the Pentium processor specifications. It has also been to ensure that the super set of these companies can provide support and distribution worldwide on a schedule that closely matches the Pentium processor's availability. Based on information available, Table 3 lists a number of companies who are planning to offer solutions to meet these requirements. All the clock drivers listed in Table 3 have maximum output frequency equal or above 66 MHz. Preliminary data sheets show that solutions listed in Table 3 meet the CPU or CPU-Cache chip set requirements. The specifications listed are based on preliminary data provided by each company and may be subject to change. Designers should contact each company for the latest specifications and availability. Some evaluation has been done by simulating an example clock layout using output models supplied by a subset of the companies listed, along with interconnect models and preliminary clock input model of the CPU-Cache chip set. For more detail on the simulations and example routing, please see Section 5.0. Intel has been and will be working closely with the listed companies to ensure they have the latest specifications for the Pentium processor. With published preliminary data sheets, all the listed parts meet either the CPU or the chip set clock specifications (including the signal quality and skew specifications). Please contact individual manufacturers for data sheets and sample availability.

Table 3. Clock Driver Options

Mfgr	Part #	Driver Type	Level In/Out	Pin-to-Pin Skew (ns)	Part-to-Part Skew (ns)	t_r/t_f (0.8V–2.0V) (ns)	Clock Stability	# of Outputs (per pkg)	Spec'd Loading	Max. Freq.
Intel Spec			TTL inputs	(1)		1.5/1.5	±250 ps (2)			66 MHz and 60 MHz
AMCC	SC35XX-1	Buffer	PECL or TTL/TTL	0.5	1.0	1.5/1.5		20 Outputs Which Vary with Part #	10 pF	80 MHz
	SC44XX-80	PLL	TTL/TTL	±0.2	1.0 (9)	1.5/1.5		6–12 Outputs	35 pF	80 MHz
AT&T (7)	DA400	PLL	PECL or TTL/TTL	0.2	0.5	1.5/1.5		8@1, 0.5X (Prog Shift)	50 pF	100 MHz
Cypress	CY7B991	PLL	TTL/TTL	0.5	1.2 (6)	1.5/1.5	0.5%	4@1X 4@1, 0.5, 0.25X	50Ω/ 30 pF	80 MHz
ICS	ICS2686	PLL		0.5	0.6	1.5/1.5		5@1, 0.5X	20 pF	
Intel	85C224-100	Divider/ Buffer/PLD	TTL/CMOS	Divider 0.4 Buffer 0.5	NA	Divider 1.2/1.1 Buffer 1.4/1.1		8 @ + 1X, −1X, 0.5X	70Ω/ 50 pF	Divider 100/50 Buffer 133
Intel	85C224-10	Buffer/ Divider/PLD	TTL/CMOS	Divider 0.4 Buffer 0.5	NA	Divider 12./1.1 Buffer 1.4/1.1		8 @ + 1X, −1X, 0.5X	70Ω/ 50 pF	Divider 58/29 Buffer 100
Motorola	MC10H646	Buffer	PECL or TTL/TTL	0.5	1.0	1.2/1.2	NA	8	50Ω/ 50 pF	100 MHz
	88915	PLL	TTL/CMOS	0.5	NA	2.5/2.5(11)	NA	5@1X 1@2X 1@.5X 1 Inverted X	50Ω	66 MHz

Table 3. Clock Driver Options (Continued)

Mfgr	Part #	Driver Type	Level In/Out	Pin-to-Pin Skew (ns)	Part-to-Part Skew (ns)	t_r/t_f (0.8V–2.0V) (ns)	Clock Stability	# of Outputs (per pkg)	Spec'd Loading	Max. Freq.
National	CGS74CT2524	Buffer	TTL/CMOS	0.45	NA	1.5/1.5		4	50 pF	100 MHz
	CGS74CT2527	Buffer	TTL/CMOS	0.45	NA	1.5/1.5		8	50 pF	100 MHz
	CGS74B2528	Buffer	TTL/TTL	0.55	NA	1.5/1.5		10	50 pF	70 MHz
Pioneer	PI6B2407	PLL	TTL/TTL	±0.25	NA	1.5/1.5	100 ps	12@1, 0.5, 2X (Prog Shift)		80 MHz
TI (8)	CDC328	Buffer	TTL/TTL	0.7	NA	1.2/0.5	NA	6	500Ω/ 50 pF	Not Spec'd.
Triquint (10)	GA1085	PLL	TTL/TTL	0.25	NA	1.4/1.4	75 ps (typ.)	5@1X 4@0.5X 2@0.5X (Prog Shift)	50Ω	66 MHz
	GA1086	PLL	TTL/TTL	0.25	NA	1.4/1.4	75 ps (typ.)	9@1X 1@0.5X	50Ω	66 MHz
	GA1087	PLL	TTL/TTL	0.25	NA	1.4/1.4	75 ps (typ.)	6@1X 4@0.5X	50Ω	66 MHz
Vitesse	VSL4485	PLL	TTL/TTL	0.5	NA	1.5/1.5		6@1X 2@1, 2, 4X	50 pF	70 MHz
	VSL4586	PLL	TTL/TTL	0.5	NA	1.5/1.5		2@1X 6@1, 2, 4X	50 pF	70 MHz

NOTES:
1. 0.7 ns between Pentium processor-82491, 82496-82491, 82491-82491. 0.2 ns between Pentium processor-82496. Assumed 0.5 ns between clock driver outputs, leaving 0.2 ns for routing or trace skew.
2. See complete specification in Table 1 or the data book.
3. Manufacturers listed in alphabetical order.
4. Contact manufacturers for price and availability information.
5. Intel does not guarantee specifications for other manufacturer's devices. All clock driver specifications listed were provided by the manufacturer and are subject to change. Designers should contact the manufacturer for the latest specification/data sheet information.
6. As low as 0.75 ns in some configurations.
7. First samples in March '93. Specifications may improve during characterization.
8. Other Solutions are under development. Contact TI for preliminary details.
9. Maximum phase erro quoted in the manufacturer's data sheet for the entire frequency range.
10. Other configurations available. Contact Triquint for details.
11. Between 0.2 V_{CC} and 0.8 V_{CC}. Contact Motorola for details between 0.8 and 2.0V.

AMCC offers the SC35XX-1 series of buffered clock drivers and the SC44XX-80 series of PLL based clock drivers. The SC35XX-1 series must be driven with a TTL or PECL 2X frequency input. Each member of the series provides 20 outputs. Depending on the specific part within the series, these 20 outputs can be configured to provide the primary frequency, 1/2, or 1/4 the primary frequency. The SC3502-1 even provides 5 inverted outputs of the primary frequency. The SC44XX-80 series must be driven with a TTL input. The PLL design allows for very low skew (±200 ps) between the outputs.Different members of the series offer different numbers and configurations of outputs. Between 4 and 8 outputs are available at the primary frequency. These devices also allow a subset of the outputs to be configured for 1/2X or 2X the primary frequency. In addition, the PLL allows the outputs to be skewed in phase from one another.

AT&T DA400 is a PLL clock driver. Its inputs can be driven by TTL or PECL levels. Eight outputs are provided. They can be configured for the primary frequency or 1/2X the primary frequency. In addition each output has a programmable delay line which allows 1/32 or 1/64 increments of the clock period of delay between outputs.

Cypress's CY7B991 is a PLL clock driver. It requires a TTL input and is able to drive 8 outputs. A subset of the outputs can be configured as 1/2X, 1/4X, or inverted outputs. As with other PLL solutions, the skew between outputs is small and the outputs can be configured for a fixed amount of delay or skew between outputs.

ICS's ICS2686 is a PLL clock driver. Five outputs are available. Both primary and 1/2X frequencies are available. The ICS2686 has been designed to work with the 74ABT240 type buffer to provide more than 5 outputs. A unique feature of the ICS2686 is the multiple feedback inputs. This feature allows synchronizing multiple outputs at their destination or load with the input clock.

Intel's 85C224-100 is a "20V8" architecture programmable logic device. From its TTL inputs it provides 8 TTL outputs which can be configured to provide 1X, 1X inverted, and 1/2X versions of the primary frequency, in any combination. When programmed to function as a frequency divider, the primary frequency can be as high as 100 MHz and the 1/2X frequency outputs will maintain output skew below 400 ps. When programmed to operate as a straight 1X buffer, it supports frequencies of up to 133 MHz with less than 500 ps of output skew. The 85C224-100 provides a combination of superior output signal quality including fast rise and fall times and low output skew. A particularly unique feature of the 85C224-100 is in its programmable logic circuitry. Its flexibility satisfies programmable logic needs such as control line signals and widespread glue logic. With this minimized output skew PLD, a single 28-pin PLCC can provide low output skew clock distribution, frequency division, and programmable logic; for the low price of a 20V8 PLD.

Motorola offers both a buffered and a PLL clock solution. Motorola's 10H646 is a buffered clock driver. It offers both TTL and ECL inputs which supports backplane routing using ECL levels. The clock driver's outputs are clamped to 3V, not V_{CC}. 10H646's output stage has similar rise and fall output resistances. Similar rise and fall output resistances makes series termination easier since the termination resistance is the difference between the characteristic impedance of the transmission line connecting the output to the load and the driver's output impedance. 10H646 has 8 1x outputs. As a straight buffer, 10H646 does not offer any multiples of the input besides 1x. The Motorola 88915 is a PLL clock driver. It provides a 0.5 ns skew between outputs. The 88915 provides 5 1X outputs along with 1 2X, 1 0.5X, and 1 inverted X outputs.

National's clock buffers are packaged to function reliably at high frequencies. Their output rise and fall resistances are approximately equal. The CGS74CT2524 and 2527 provide 0.45 ns of output skew. The CGS74CT2528's output skew, 0.55 ns, allows for only 0.15 ns skew due to board traces or any unbalanced loading effects when using the 82496/82491 cache, however this amount may be sufficient for other cache solutions. These parts offer a range of 4, 8, and 10 outputs. The CGS74CT2524 and 2527 have CMOS level outputs, which transition from rail to rail.

Pioneer's PI6B2407 is a PLL clock driver. From its TTL input, it provides twelve TTL outputs, which can be configured to operate at 1X or 2X the input frequency. In addition, the outputs can be phase adjusted from the input clock. The PI6B2407 is able to provide ±0.25 ns of skew between outputs while maintaining the fast 1.5 ns rise and fall times.

Texas Instruments' ABT328 driver provides six outputs with an output skew of 0.7 ns. Please contact Texas Instruments for the availability of 0.5 ns output skew parts. 0.7 ns output skew is too large for the chip set application. In the design example on Section 5.0, 0.5 ns output skew is assumed. As a buffered driver, the ABT328 offers only 1x outputs.

TriQuint's GA1086 is a Gallium Arsenide-based product. It takes a 66 MHz input and produces nine 66 MHz outputs and one 33 MHz output. The availability of a low skew 33 MHz output facilitates clock distribution for systems that have synchronous 33 MHz memory buses. Since the part is phase-lock-loop based, one of the outputs can be fed back to the input so that all the outputs are synchronized with the input clock. Such a set up is ideal for cascading clock drivers to achieve maximum fanout. The specified output skew of the GA1086 is 0.25 ps, the smallest skew number available. Triquint also offers the GA1085 and GA1087. These products are similar to the GA1086, however, they offer different combinations of outputs between 1X and 0.5X.

Vitesse's VSL4485 is also a Gallium Arsenide-based product. It offers 1x, 2x, and 4x options on two of its eight outputs. Thus, to obtain both 33 MHz and 66 MHz signals with low skew, for example, the clock input frequency of the VSL4485 can be 33 MHz. For the chip set application, two 66 MHz outputs are not enough, and thus cascading another driver is necessary. Alternatively, the input can be 66 MHz and all of its outputs can be at 66 MHz. It offers 0.5 ns output skew, and a low effective delay. In addition, VSL4485 can generate programmable, multiple phase relationships among its outputs.

4.0 CLOCK GENERATION FOR THE Pentium® PROCESSOR AND THE CPU-CACHE CHIP SET

Clock generation is the generation of copies of clock signals from a signal oscillator or any other source which then are distributed to the various loads. The function of a clock driver is to generate multiple copies of clocks from a single source. In general, Pentium processor-based systems have three types of memory interface: fully synchronous, divided synchronous, and asynchronous. Each interface requires different methods of clock generation. The basic setup of a processor card is illustrated symbolically in Figure 6. Depending on the configuration, the Clock In signal can come from the memory bus or a separate oscillator.

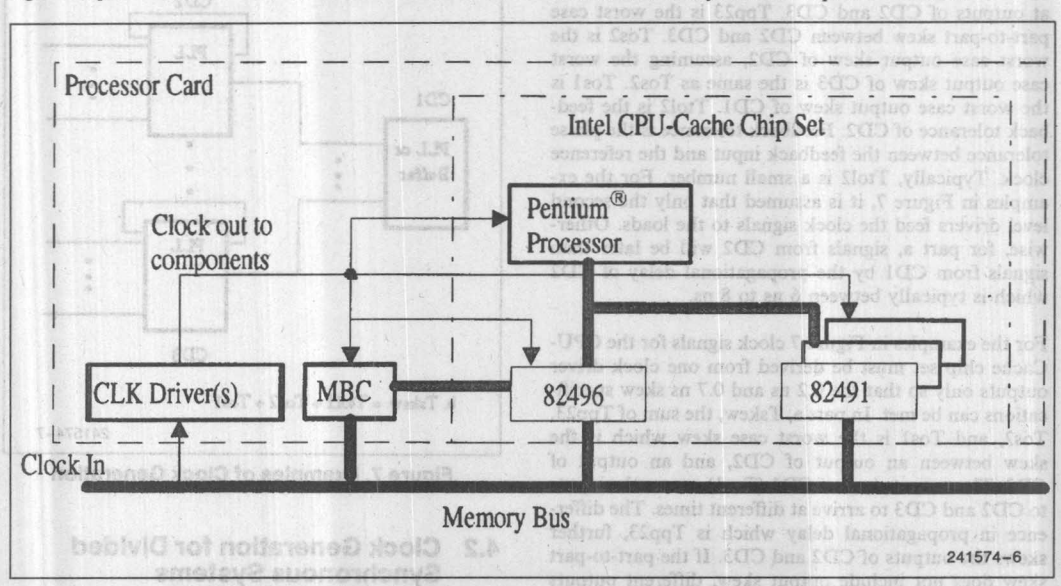


Figure 6. A CPU Module with the Pentium® Processor, 82496 and 82491 CPU-Cache Chip Set

4.1 Clock Generation for Fully Synchronous Systems

A fully synchronous system is one which everything in the system runs synchronous to the CPU. In particular, the memory bus interface is synchronous to the CPU. In Figure 6, the memory bus is at 66 MHz, synchronous to the CPU module. Clock In signal must be synchronous to the memory bus. Clocking for this case involves the generation of tightly controlled copies of clock signals that are distributed to all the clocked parts. The task of clock generation and distribution is the most difficult for this type of set up. All copies of clock signals must come from a single source, and must be deskewed appropriately. For Pentium processor-based systems that run at 66 MHz, the most critical parameter in choosing a clock driver is its output skew, as well as its part-to-part skew if more than one driver is needed. Since all the clock signals are at 66 MHz, only 1x outputs are needed. All of the drivers listed in Section 3.0 can be used here.

For a fully synchronous configuration, it is likely that a single clock driver cannot provide enough copies of clock signals. Then, some kind of cascading of drivers is necessary. Figure 7 shows two ways of clock generation by cascading drivers. Tskew is the total worst case skew at outputs of CD2 and CD3. Tpp23 is the worst case part-to-part skew between CD2 and CD3. Tos2 is the worst case output skew of CD2, assuming the worst case output skew of CD3 is the same as Tos2. Tos1 is the worst case output skew of CD1. Ttol2 is the feedback tolerance of CD2. Feedback tolerance is the phase tolerance between the feedback input and the reference clock. Typically, Ttol2 is a small number. For the examples in Figure 7, it is assumed that only the second level drivers feed the clock signals to the loads. Otherwise, for part a, signals from CD2 will be later than signals from CD1 by the propagational delay of CD2 which is typically between 6 ns to 8 ns.

For the examples in Figure 7 clock signals for the CPU-Cache chip set must be derived from one clock driver outputs only so that the 0.2 ns and 0.7 ns skew specifications can be met. In part a, Tskew, the sum of Tpp23, Tos2, and Tos1 is the worst case skew which is the skew between an output of CD2, and an output of CD3. The output skew of CD1 (Tos1) causes the inputs to CD2 and CD3 to arrive at different times. The difference in propagational delay which is Tpp23, further skews the outputs of CD2 and CD3. If the part-to-part skew does not include output skew, different outputs from CD2 and CD3 can also be skewed by the output skew. For part b, Tskew, the sum of Ttol2, Tos2, and Tos1, is also the worst case skew between the outputs of CD2 and the outputs of CD3. Once again, Tos1 causes the inputs to CD2 and CD3 to arrive at different times. The feedback in CD2 synchronizes all its outputs in the input. The feedback output of CD2 is different from the input reference clock only by Ttol2. All the other outputs are further skewed from the feedback output by Tos2. The analysis for CD3 is the same.

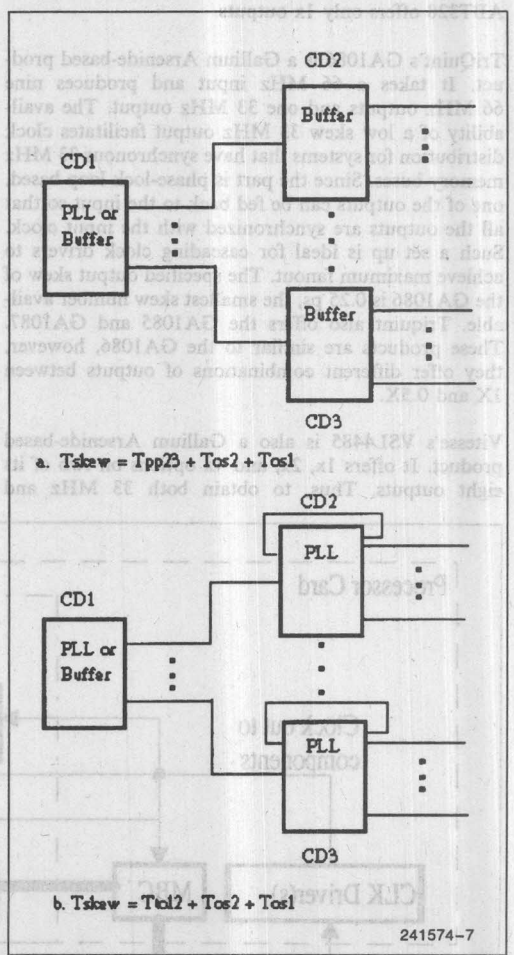


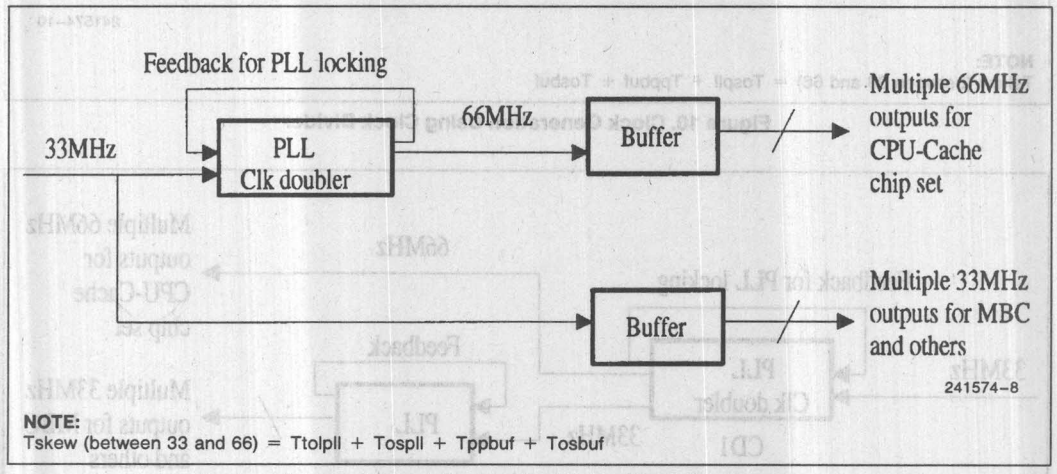
Figure 7. Examples of Clock Generation

4.2 Clock Generation for Divided Synchronous Systems

For a divided synchronous system, the memory bus is at half the speed of the CPU-Cache chip set; i.e.,

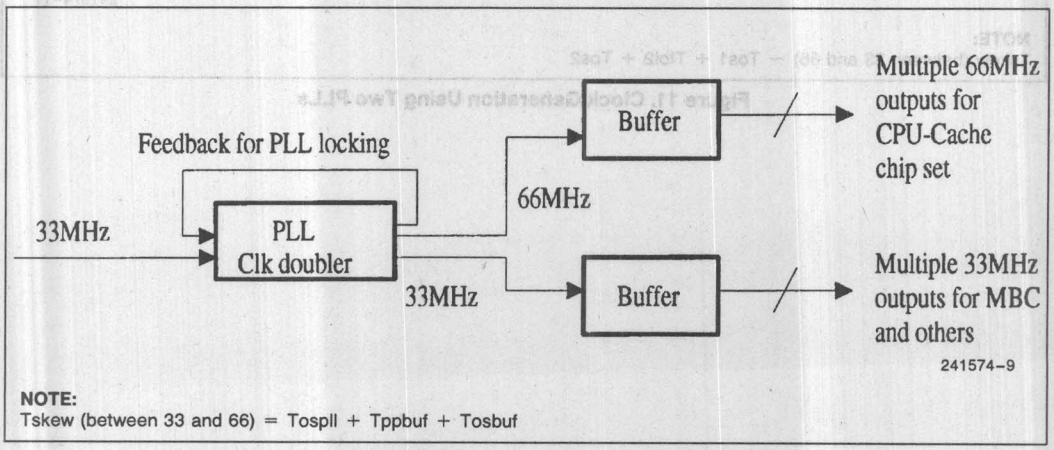
the memory bus runs at 33 MHz for the Pentium processor or the CPU-Cache chip set based systems. A 33 MHz reference clock (Clock In) can come from the backplane from which all the clocks serving the CPU-cache module (Figure 6) must be synchronized. The memory bus controller (MBC) itself requires both 33 MHz and 66 MHz clocks. For this configuration, clock drivers that can provide both 33 MHz and 66 MHz outputs are needed.

There are several ways of providing the two frequencies. They are shown in Figure 8 through Figure 12. Tskew is the worst skew between 33 MHz signals and 66 MHz signals. The skews among 66 MHz signals or among 33 MHz signals are simply the output skew of the driving devices. Ttolpll is the PLL CLK doubler or PLL CLK divider's feedback tolerance. Tospll is the PLL CLK doubler or PLL CLK divider's worst case output skew. Tppbuf is the worst case part-to-part skew of the second level buffers. Those buffers can be phase-lock-loops also in which case Tppbuf is the feedback tolerance of the PLLs if feedback is used. Tosbuf is the worst case output skew of the second level buffers. Tos1 is the output skew of CD1, Ttol2 is the feedback tolerance of CD2, and Tos2 is the output skew of CD2.



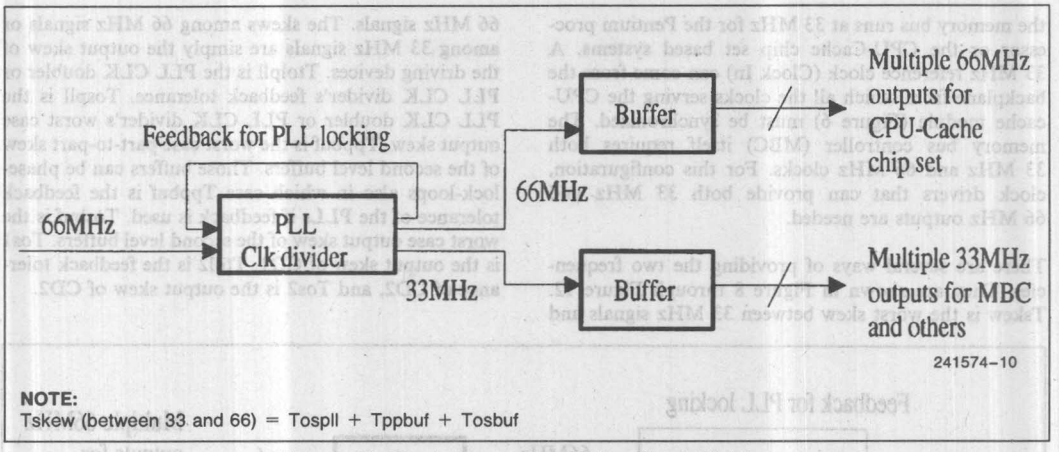
NOTE:
Tskew (between 33 and 66) = Ttolpll + Tospll + Tppbuf + Tosbuf

Figure 8. Clock Generation Using Clock Doubler



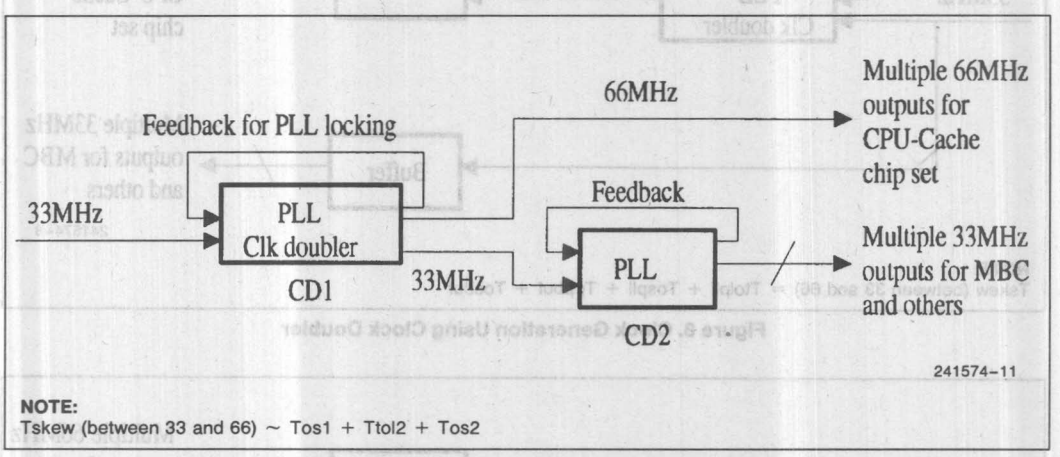
NOTE:
Tskew (between 33 and 66) = Tospll + Tppbuf + Tosbuf

Figure 9. Clock Generation Using Clock Doubler



NOTE:
Tskew (between 33 and 66) = Tospll + Tppbuf + Tosbuf

Figure 10. Clock Generation Using Clock Divider



NOTE:
Tskew (between 33 and 66) ~ Tos1 + Ttol2 + Tos2

Figure 11. Clock Generation Using Two PLLs

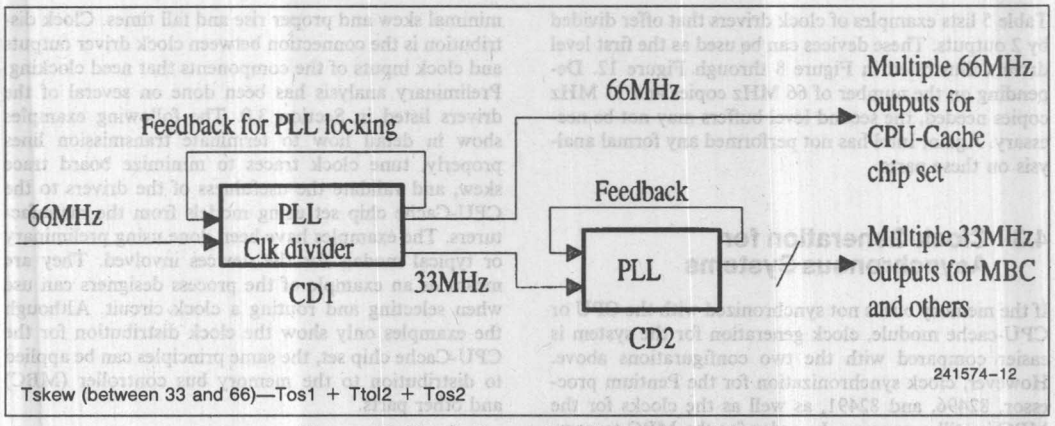


Figure 12. Clock Generation Using Two PLLs

Since the outputs of the first level PLL CLK doublers and dividers go directly to inputs of another clock driver, the signal quality requirements of these outputs are not as stringent as if the outputs drive the loads of the Pentium processor and others. One of the functions of a clock driver is to buffer and clean up a clock signal in addition to generating multiple copies of the same. However, the output skew of the PLL used for the first level is very important. Depending if feedback is used, the feedback tolerance is of importance. When choosing a clock driver, also be sure that its maximum output frequency is greater than 66 MHz for 66 MHz outputs and 33 MHz for 33 MHz outputs. The parts listed in Table 4 and Table 5 are examples of devices that can be used as first level drivers as illustrated in Figure 8 through Figure 12.

Table 4. List of Clock Doubler Parts

Manufacturer	Part #	Driver Type	# of Outputs (per pkg)
Motorola	88915	PLL	1 @ 2x 6 @ 1x (1) 1 @ 0.5x
Motorola	88916	PLL	1 @ 2x 4 @ 1x (1) 1 @ 0.5x
TI	ABT338	PLL	1 @ 2x 4 @ 1x 1 @ 0.5x
Vitesse	VSL4485	PLL	6 @ 1x 2 @ 1, 2, or 4x

NOTES:
1. One of the outputs is inverted.
2. This list is not meant to be complete. Other solutions may be available.

The phase-lock-loop drivers listed in Table 4 can be used to drive the Pentium processor loads directly if only one copy of 66 MHz clock signal is needed. In this case, the second level buffers are not necessary if the driver used can provide enough 33 MHz copies. Intel has not done formal analysis on these parts.

Table 5. List of Clock Divider Parts

Manufacturer	Part #	Driver Type	# of Outputs (per pkg)
Motorola	88915	PLL	1 @ 2x 6 @ 1x (1) 1 @ 0.5x
Motorola	88916	PLL	1 @ 2x 4 @ 1x (1) 1 @ 0.5x
Texas Instruments	ABT338	PLL	1 @ 2x 4 @ 1x 1 @ 0.5x
Texas Instruments	ABT337	Buffer	4 @ 1x 4 @ 0.5x
Texas Instruments	ABT339	Buffer	4 @ 1x 4 @ 0.5x
TriQuint	GA1086	PLL	9 @ 1x 1 @ 0.5x

NOTES:
1. One of the outputs is inverted.
2. This list is not meant to be complete. Other solutions may be available.

Table 5 lists examples of clock drivers that offer divided by 2 outputs. These devices can be used as the first level drivers illustrated in Figure 8 through Figure 12. Depending on the number of 66 MHz copies and 33 MHz copies needed, the second level buffers may not be necessary. Again, Intel has not performed any formal analysis on these parts.

4.3 Clock Generation for Asynchronous Systems

If the memory bus is not synchronized with the CPU or CPU-cache module, clock generation for the system is easier compared with the two configurations above. However, clock synchronization for the Pentium processor, 82496, and 82491, as well as the clocks for the MBC is still a concern. In order for the MBC to communicate properly with the CPU-Cache chip set, some synchronized clocks at 66 MHz are needed. Since the system is asynchronous to the CPU-Cache chip set, the number of synchronous MBC clock signals is less than the synchronous case. The examples in Section 5.0 illustrate how the synchronization is done. Since the system is asynchronous, one can use a different clock source for the CPU-Cache chip set from the rest of the system.

5.0 Pentium® PROCESSOR WITH 256K 82496/82491 SECOND LEVEL CACHE CLOCK DISTRIBUTION DESIGN EXAMPLES

After a clock generation scheme is determined, careful analysis must be done on clock distribution to ensure minimal skew and proper rise and fall times. Clock distribution is the connection between clock driver outputs and clock inputs of the components that need clocking. Preliminary analysis has been done on several of the drivers listed in Section 3.0. The following examples show in detail how to terminate transmission lines properly, tune clock traces to minimize board trace skew, and validate the usefulness of the drivers to the CPU-Cache chip set using models from the manufacturers. The examples have been done using preliminary or typical models for the devices involved. They are meant as an example of the process designers can use when selecting and routing a clock circuit. Although the examples only show the clock distribution for the CPU-Cache chip set, the same principles can be applied to distribution to the memory bus controller (MBC) and other parts.

5.1 Clock Routing for the 256K CPU-Cache Chip Set

Analysis for CPU-Cache chip set clock routing is done using first order input models for the three chips, shown in Figure 13. Specific to CLK inputs, the models shown are **typical models** based on on-going simulation efforts, and are subject to change. Refer to the Intel data books or contact Intel for the latest models (including minimum and maximum conditions). The models include package inductance, package capacitance, and input buffer capacitance of the clock pins.

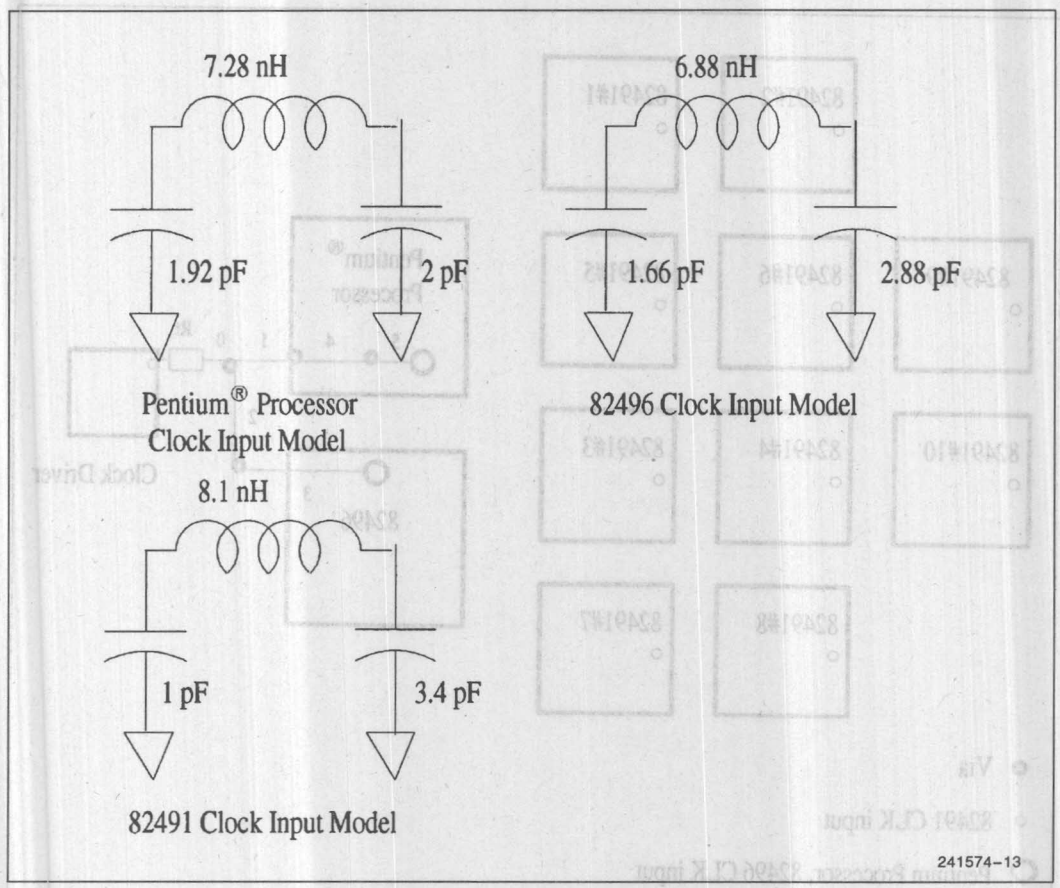
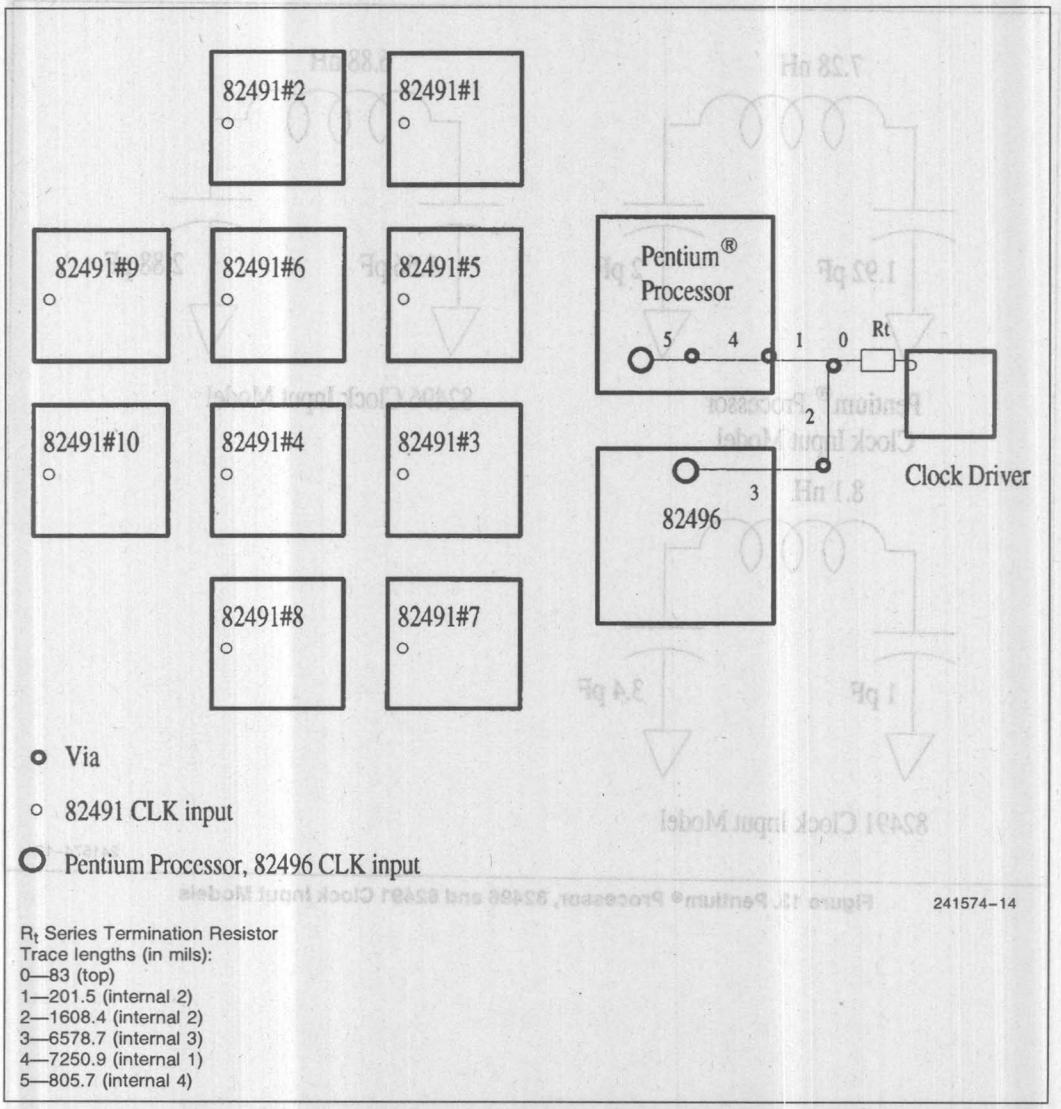
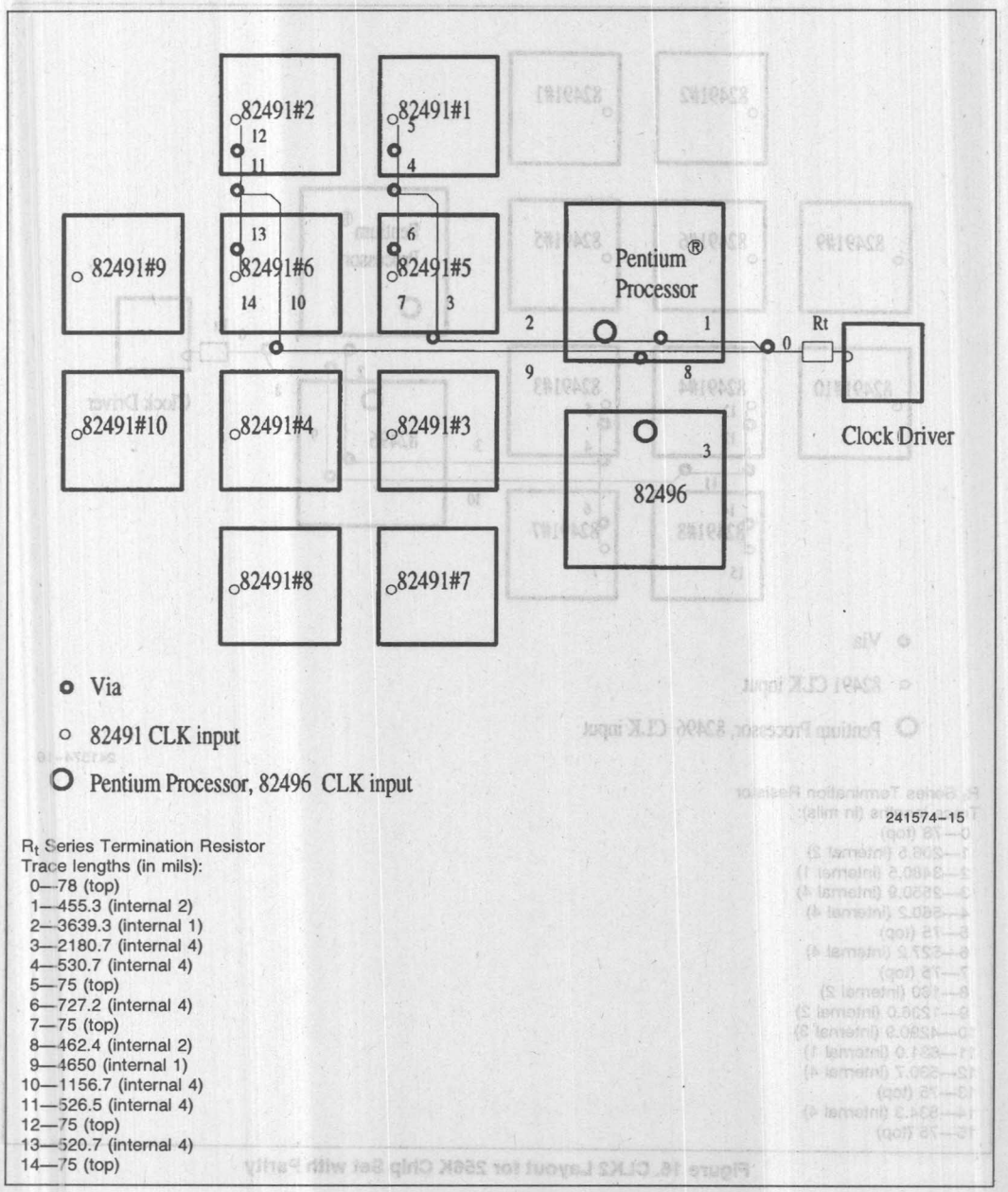


Figure 13. Pentium® Processor, 82496 and 82491 Clock Input Models



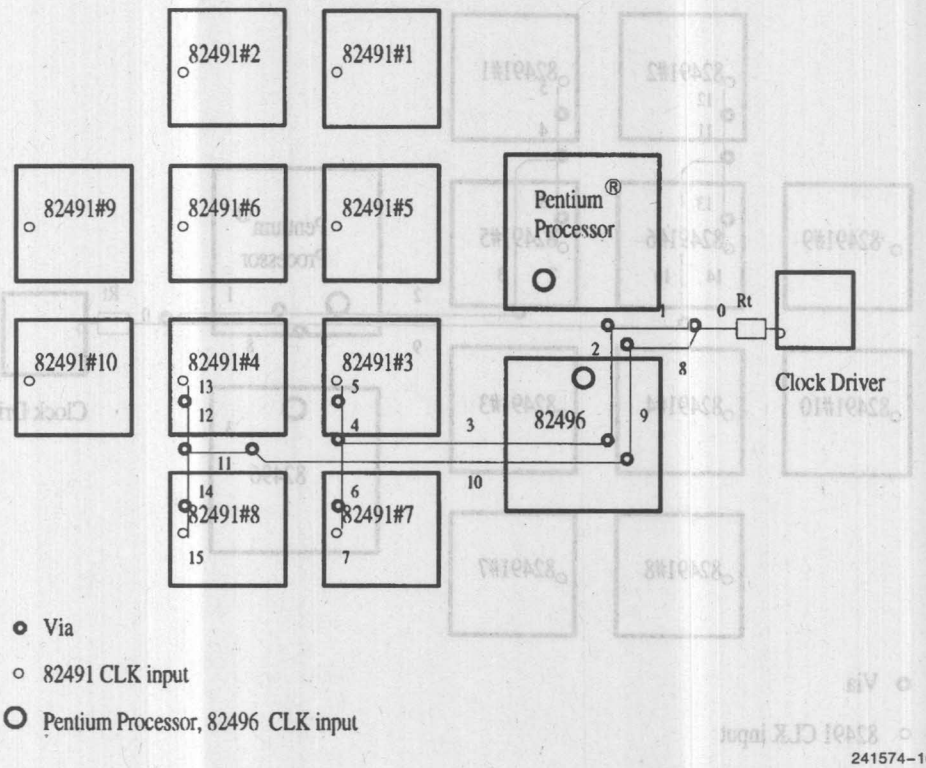
R_t Series Termination Resistor
Trace lengths (in mils):
0—83 (top)
1—201.5 (internal 2)
2—1608.4 (internal 2)
3—6578.7 (internal 3)
4—7250.9 (internal 1)
5—805.7 (internal 4)

Figure 14. CLK0 Layout for 256K Chip Set with Parity



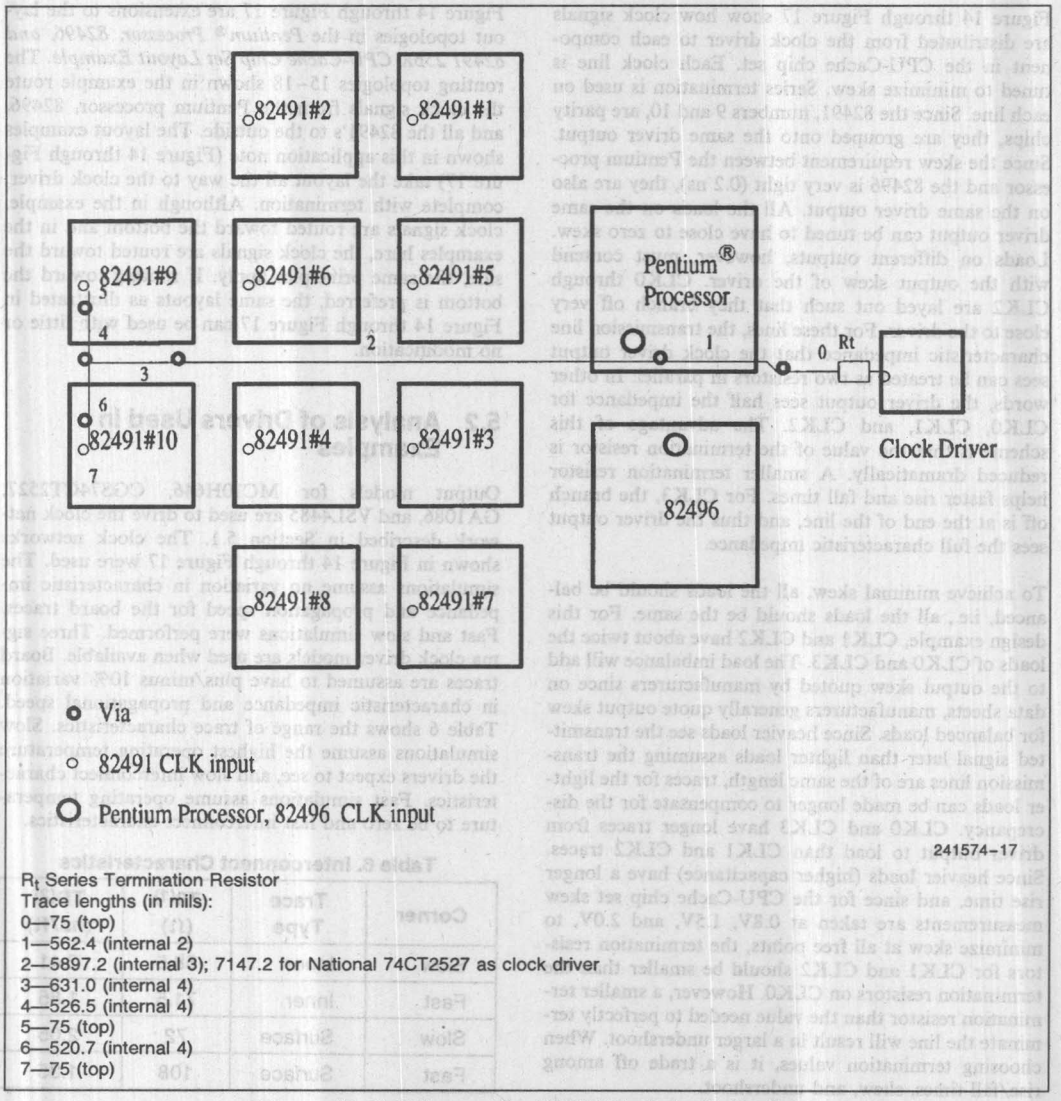
R_t Series Termination Resistor
Trace lengths (in mils):
0—78 (top)
1—455.3 (internal 2)
2—3639.3 (internal 1)
3—2180.7 (internal 4)
4—530.7 (internal 4)
5—75 (top)
6—727.2 (internal 4)
7—75 (top)
8—462.4 (internal 2)
9—4650 (internal 1)
10—1156.7 (internal 4)
11—526.5 (internal 4)
12—75 (top)
13—520.7 (internal 4)
14—75 (top)

Figure 15. CLK1 Layout for 256K Chip Set with Parity



R_t Series Termination Resistor
Trace lengths (in mils):
0—78 (top)
1—206.5 (internal 2)
2—3480.5 (internal 1)
3—2550.9 (internal 4)
4—560.2 (internal 4)
5—75 (top)
6—527.2 (internal 4)
7—75 (top)
8—160 (internal 2)
9—1236.0 (internal 2)
10—4290.9 (internal 3)
11—631.0 (internal 1)
12—530.7 (internal 4)
13—75 (top)
14—534.3 (internal 4)
15—75 (top)

Figure 16. CLK2 Layout for 256K Chip Set with Parity



R_t Series Termination Resistor
Trace lengths (in mils):
0—75 (top)
1—562.4 (internal 2)
2—5897.2 (internal 3); 7147.2 for National 74CT2527 as clock driver
3—631.0 (internal 4)
4—526.5 (internal 4)
5—75 (top)
6—520.7 (internal 4)
7—75 (top)

Figure 17. CLK3 Layout for 256K Chip Set with Parity

sees can be treated as two resistors in parallel. In other words, the driver output sees half the impedance for CLK0, CLK1, and CLK2. The advantage of this scheme is that the value of the termination resistor is reduced dramatically. A smaller termination resistor helps faster rise and fall times. For CLK3, the branch off is at the end of the line, and thus the driver output sees the full characteristic impedance.

To achieve minimal skew, all the loads should be balanced, i.e., all the loads should be the same. For this design example, CLK1 and CLK2 have about twice the loads of CLK0 and CLK3. The load imbalance will add to the output skew quoted by manufacturers since on data sheets, manufacturers generally quote output skew for balanced loads. Since heavier loads see the transmitted signal later than lighter loads assuming the transmission lines are of the same length, traces for the lighter loads can be made longer to compensate for the discrepancy. CLK0 and CLK3 have longer traces from driver output to load than CLK1 and CLK2 traces. Since heavier loads (higher capacitance) have a longer rise time, and since for the CPU-Cache chip set skew measurements are taken at 0.8V, 1.5V, and 2.0V, to minimize skew at all free points, the termination resistors for CLK1 and CLK2 should be smaller than the termination resistors on CLK0. However, a smaller termination resistor than the value needed to perfectly terminate the line will result in a larger undershoot. When choosing termination values, it is a trade off among rise/fall times, skew, and undershoot.

When choosing a termination value, it is important to know the output impedance of the driver. For many TTL drivers, output rise impedance is different from output fall impedance. [Reference 3, Section 9] shows how to measure output impedance, or the driver manufacturer can be contacted for the information. Typically, output fall impedance is 5Ω–10Ω, and rise impedance is 5Ω–50Ω.

5.2 Analysis of Drivers Used in Examples

Output models for MC10H646, CGS74CT2527, GA1086, and VSL4485 are used to drive the clock network described in Section 5.1. The clock networks shown in Figure 14 through Figure 17 were used. The simulations assume no variation in characteristic impedance and propagation speed for the board traces. Fast and slow simulations were performed. Three sigma clock driver models are used when available. Board traces are assumed to have plus/minus 10% variation in characteristic impedance and propagational speed. Table 6 shows the range of trace characteristics. Slow simulations assume the highest operating temperature the drivers expect to see, and slow interconnect characteristics. Fast simulations assume operating temperature to be zero and fast interconnect characteristics.

Table 6. Interconnect Characteristics

Corner	Trace Type	Z0(1) (Ω)	TD(2) (ns/ft)
Slow	Inner	58.5	2.41
Fast	Inner	71.5	1.85
Slow	Surface	72	2.05
Fast	Surface	108	1.35

NOTES:
1. Characteristic Impedance
2. Propagational Speed

Since simulation can only account for skew due to board trace and load imbalance, total skew is assumed to be the sum of the worst case output skew published by driver manufacturers and skew from simulation. Skew from simulation is derived by using identical driver models for each driver output, thus assuming zero

output skew. The board traces and termination resistances are tuned with 0.5 ns output skew in mind which leaves 0.2 ns for trace skew. For TriQuint's GA1086, the output skew is 0.25 ns; thus, there is a larger window for trace skew. Table 7 summarizes simulation results of the tightest parameters for each driver. All of the drivers can meet the 4 ns minimum high and low times easily. Most clock drivers guarantee a 45/55 duty cycle, which exceeds Intel's requirement.

Series termination resistors are chosen to minimize skew and undershoot. To achieve similar rise time for each load, termination resistance values are smaller for heavier loaded lines such as CLK1 and CLK2 compared to the resistance values for CLK0. Since CLK3 splits off at the end of the line, its termination value is about twice as CLK0's. Table 8 lists the termination values for each line and for each driver. Waveforms for each driver are attached. Notice the signals at the CLK input for each load is relatively clean whereas the signals at the driver side are not. Since the clock signals are only important to the component receiving the signal, how dirty the signal is at the driver end is not important, providing that the signal does not cause any damage or other ill effects on the driver.

Figures attached in this section show some waveforms from the simulations. V(201) is the voltage at the Pentium processor clock input, V(202) is the voltage at the 82496 clock input, and V(213), V(214), V(217), and V(218) are voltages at the 82491 clock inputs for the 82491s on CLK1 line. For 74CT2527, V(8) is the voltage at driver output, V(100) is the voltage at the junction of the series termination resistor and the beginning of board trace. For 10H646, V(9) is the voltage at driver output, V(20) is the voltage at the junction of the series termination resistor and the beginning of board trace.

Table 7. Compilation of Simulation Data

Mfr.	Clock Driver	Worst Skew P5-C5C (ns)(1)			Worst Skew C8C-Others (ns)			Worst Skew C8C (No Parity) (ns)(2)			Undershoot (−mV)(3)			Tr/Tf (ns)(4)		
		Slow	Fast	Spec	Slow	Fast	Spec	Slow	Fast	Spec	Slow	Fast	Spec	Slow	Fast	Spec
Motorola	10H646	0.021	0.023	0.2	0.65	0.67	0.7	0.65	0.67	0.7	468	816	1600	0.90/ 1.13	0.74/ 0.67	1.5/ 1.5
National	74CT2527	0.0071	(5)	0.2	0.67	(5)	0.7	0.61	(5)	0.7	285	(5)	1600	1.14/ 0.42	(5)	1.5/ 1.5
TriQuint	GA1086	0	0	0.2	0.55	0.45	0.7	0.45	0.45	0.7	150	400	1600	0.9/ 1.9 (6)	0.6/ 1.2	1.5/ 1.5
Vitesse	VSL4485	0.02	0.05	0.2	0.7	0.57	0.7	0.66	0.57	0.7	275	800	1600	0.95/ 0.78	0.78/ 0.6	1.5/ 1.5

NOTES:
1. All Skews are worst case numbers
2. Not using the parity chips
3. Worst Undershoot of all the CLK nodes
4. Slowest rise and fall times of all the CLK nodes
5. Only typical model at 25°C is available. Thus, only simulation performed is with slow interconnect corner
6. Simulation done on driver slow corner. Device specification for t_f is 1.4 ns worst case. Device was still under development when simulation was done. Please contact TriQuint for more information.

Clock distribution method for the memory bus controller (MBC) is very similar to that of the chip set. When distributing clocks for the MBC, be sure to load each driver output with similar loads as for the chip set, and route clock traces with similar lengths as for the chip set. For example, CLK1 and CLK2 have an aggregate load of about 20 pF, and the total clock trace length is about 7" from driver output to a load. To minimize the clock skew of the MBC clock from loads on CLK1 and CLK2 lines, the clock lines should fan out 2.9 pF per inch. Also, be sure to terminate the line properly. It is important to keep the loading similar to the loadings on clock lines of the chip set if skew is to be kept close to 0.7 ns. Adjusting trace lengths and termination resistance can compensate for load imbalance to a degree, but not perfectly and not always.

Simulations results provided here are based on best available models at the time. Some models were for parts still under development at the time of simulation. Therefore, the simulation results are subject to change.

Table 8. Series Termination Resistor Values for Each Line

Manufacturer	Clock	CLK Line	R_t (Ω)
Motorola	10H646	CLK0	26
		CLK1	20
		CLK2	20
		CLK3	59
National	74CT2527	CLK0	20
		CLK1	15
		CLK2	15
		CLK3	45
TriQuint	GA1086	CLK0	30
		CLK1	30
		CLK2	30
		CLK3	50
Vitesse	VSL4485	CLK0	32
		CLK1	23
		CLK2	23
		CLK3	48

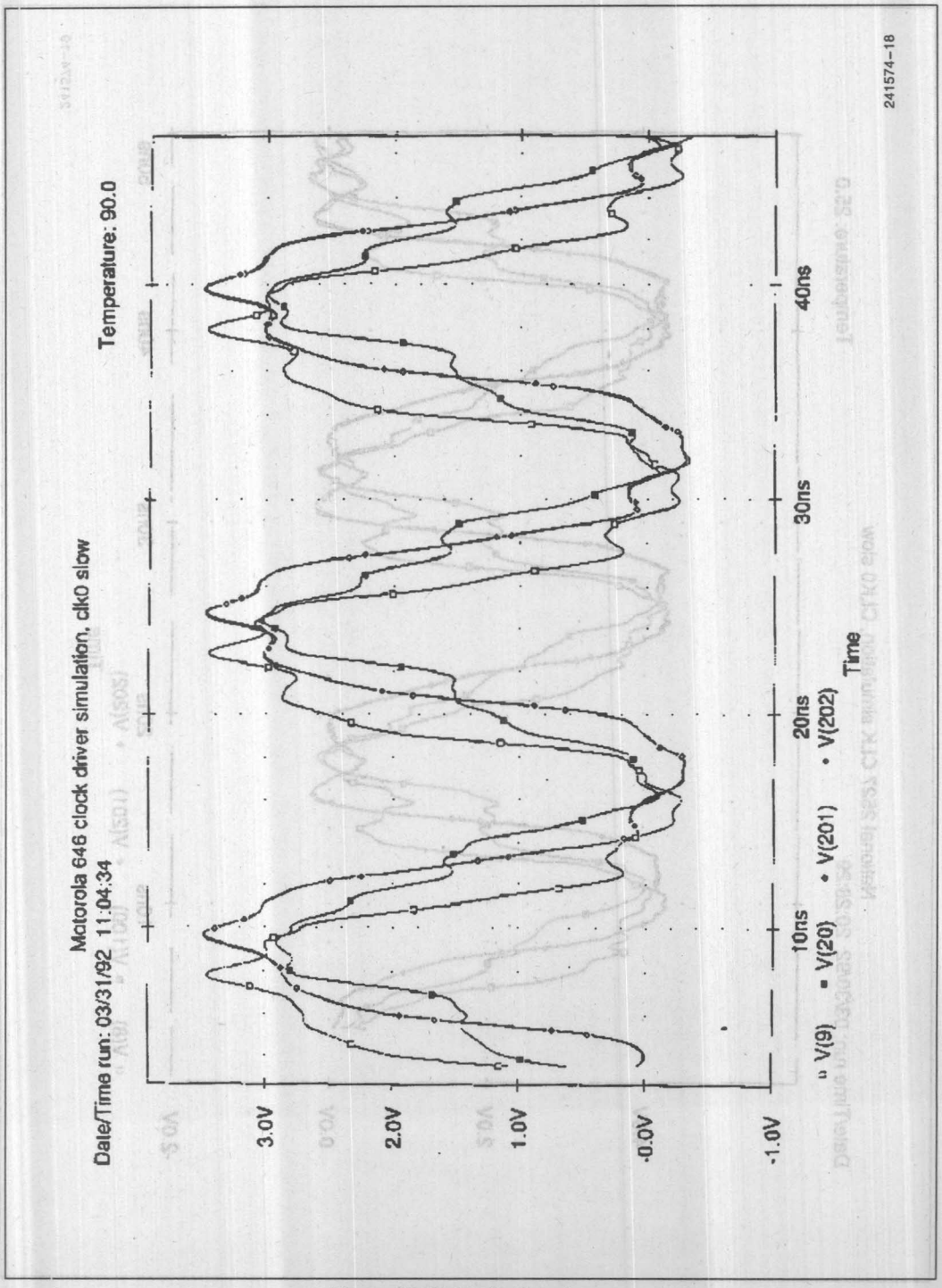


Figure 18. Motorola Waveform

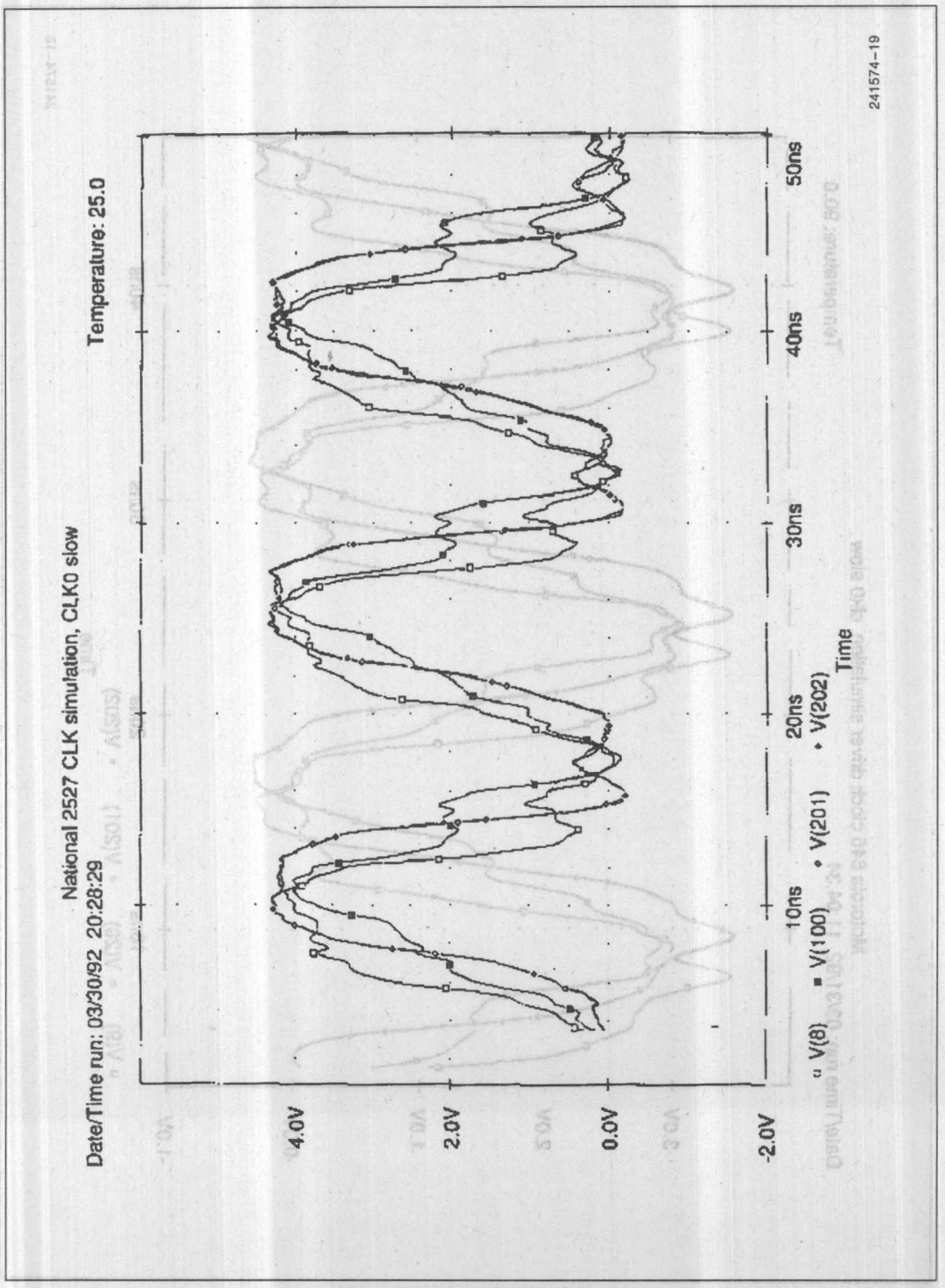


Figure 19. National Waveform

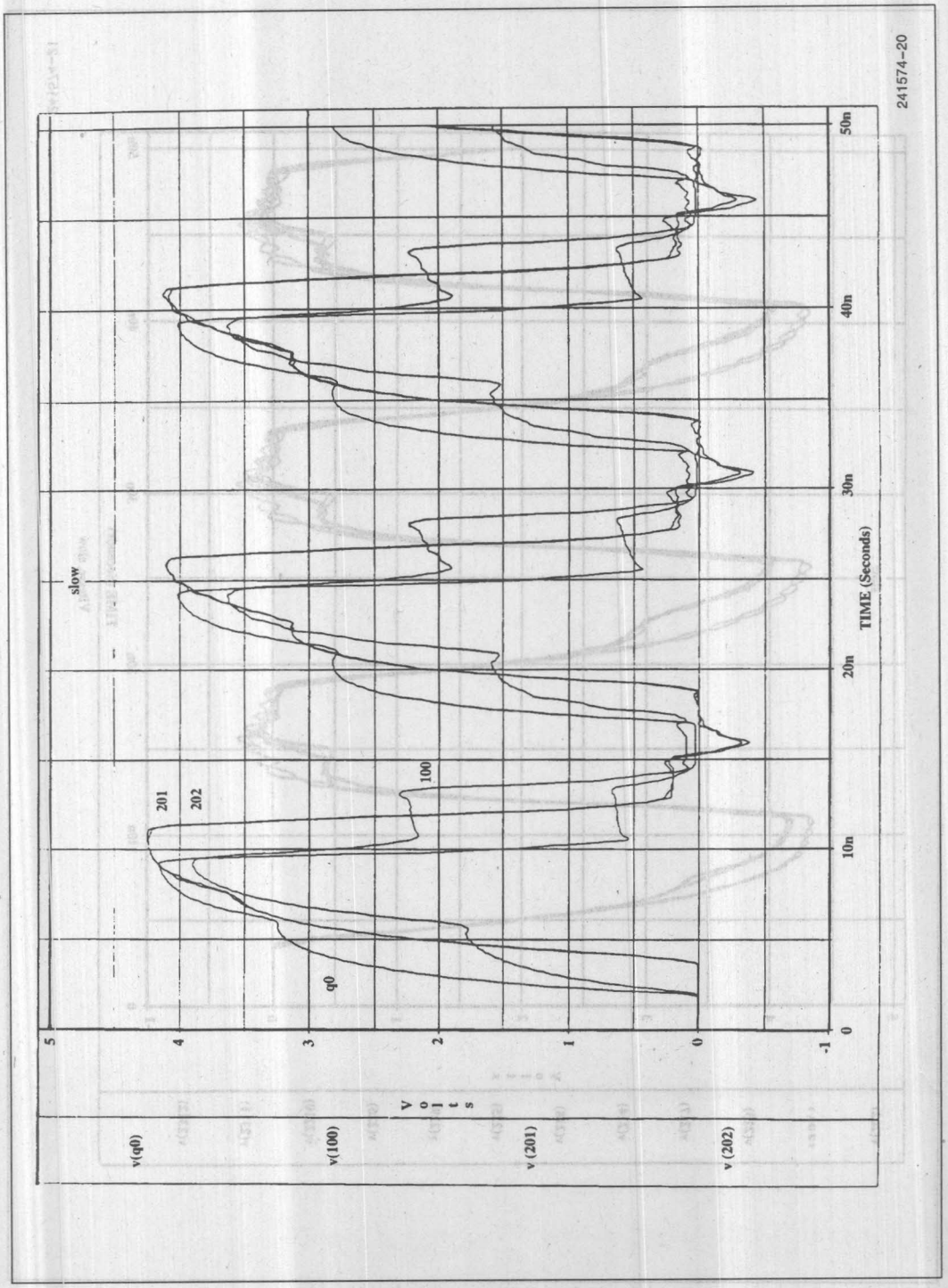


Figure 20. Vitesse (Slow) Waveform

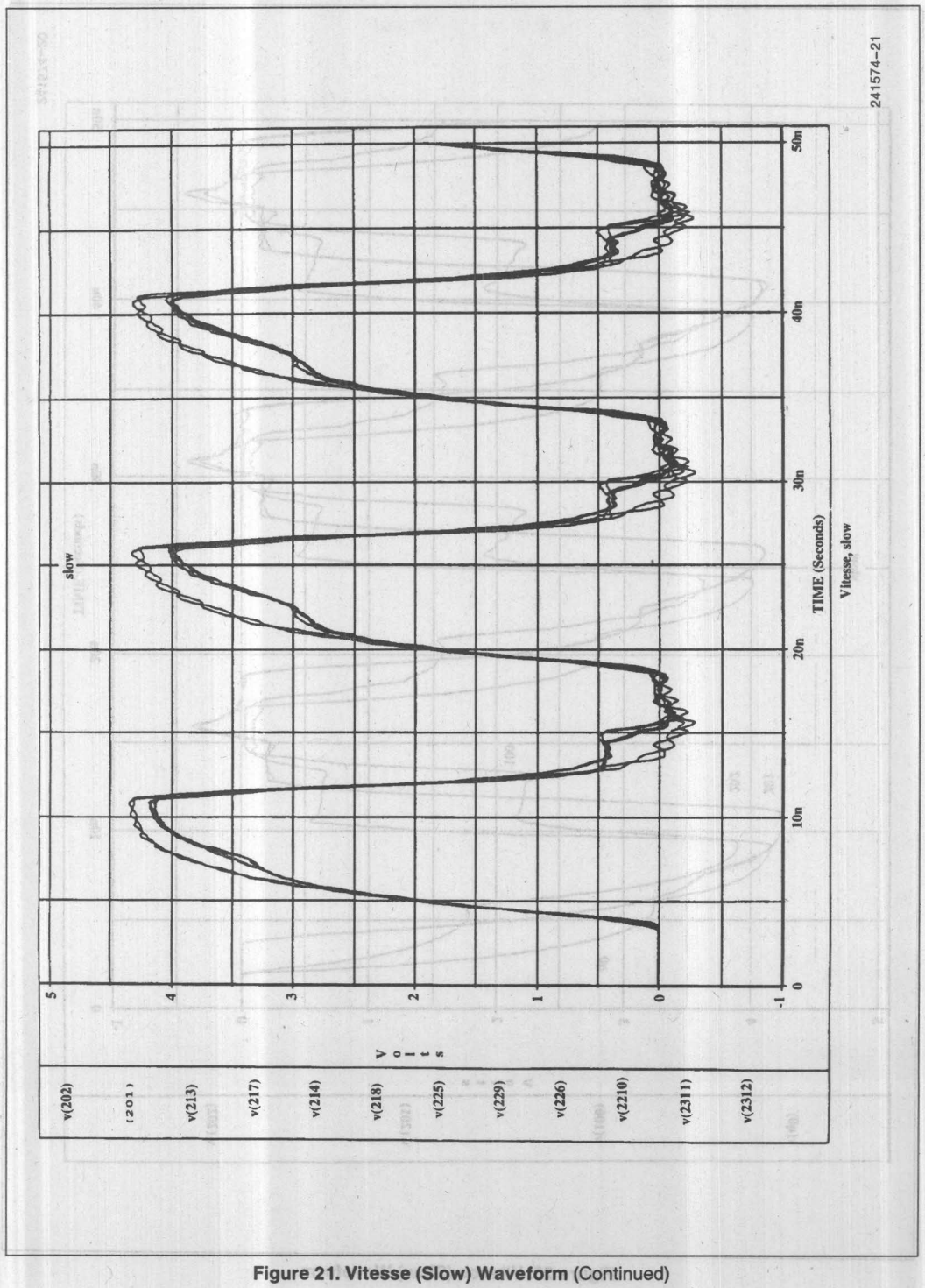


Figure 21. Vitesse (Slow) Waveform (Continued)

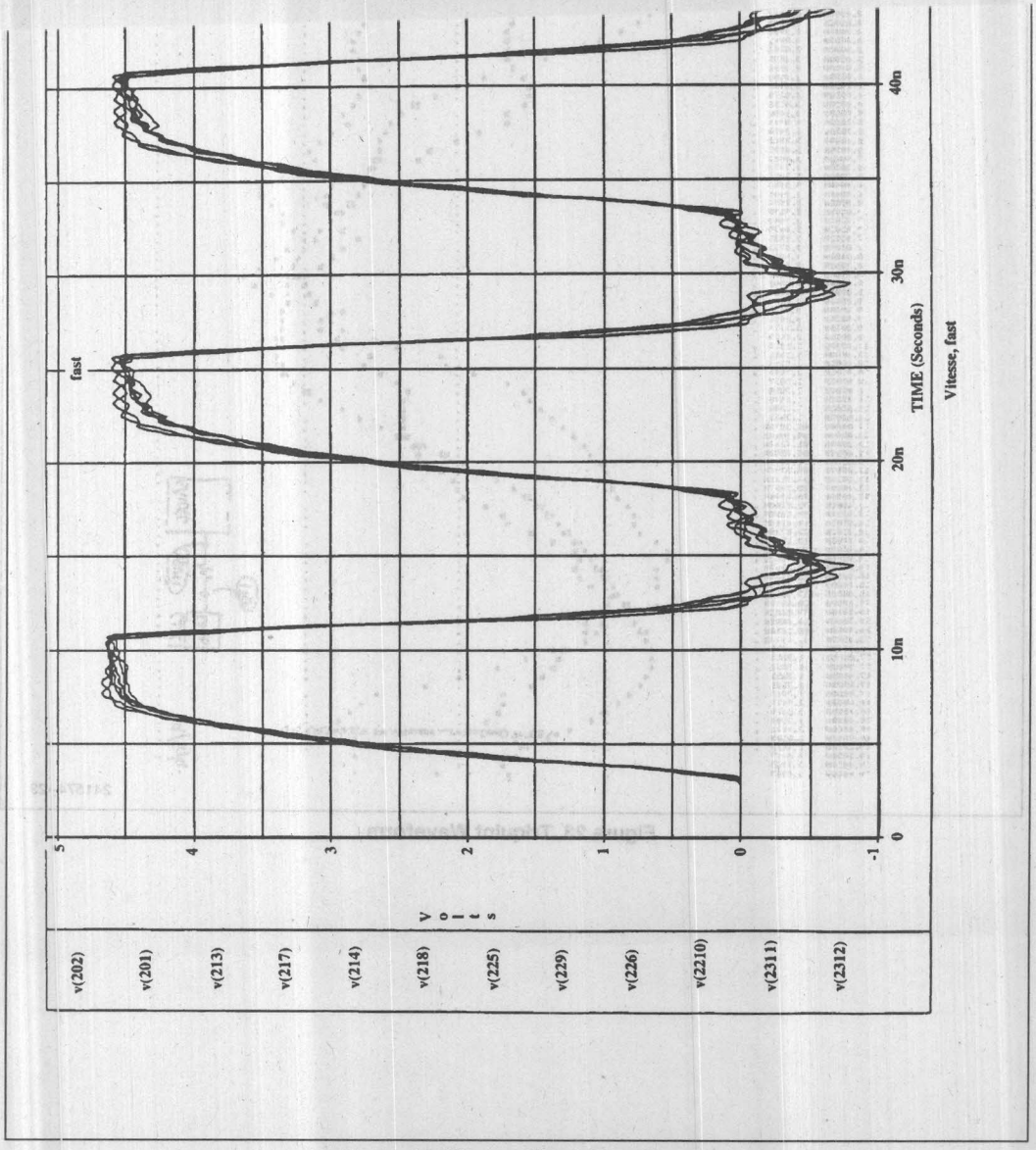


Figure 22. Vitesse (Fast) Waveform

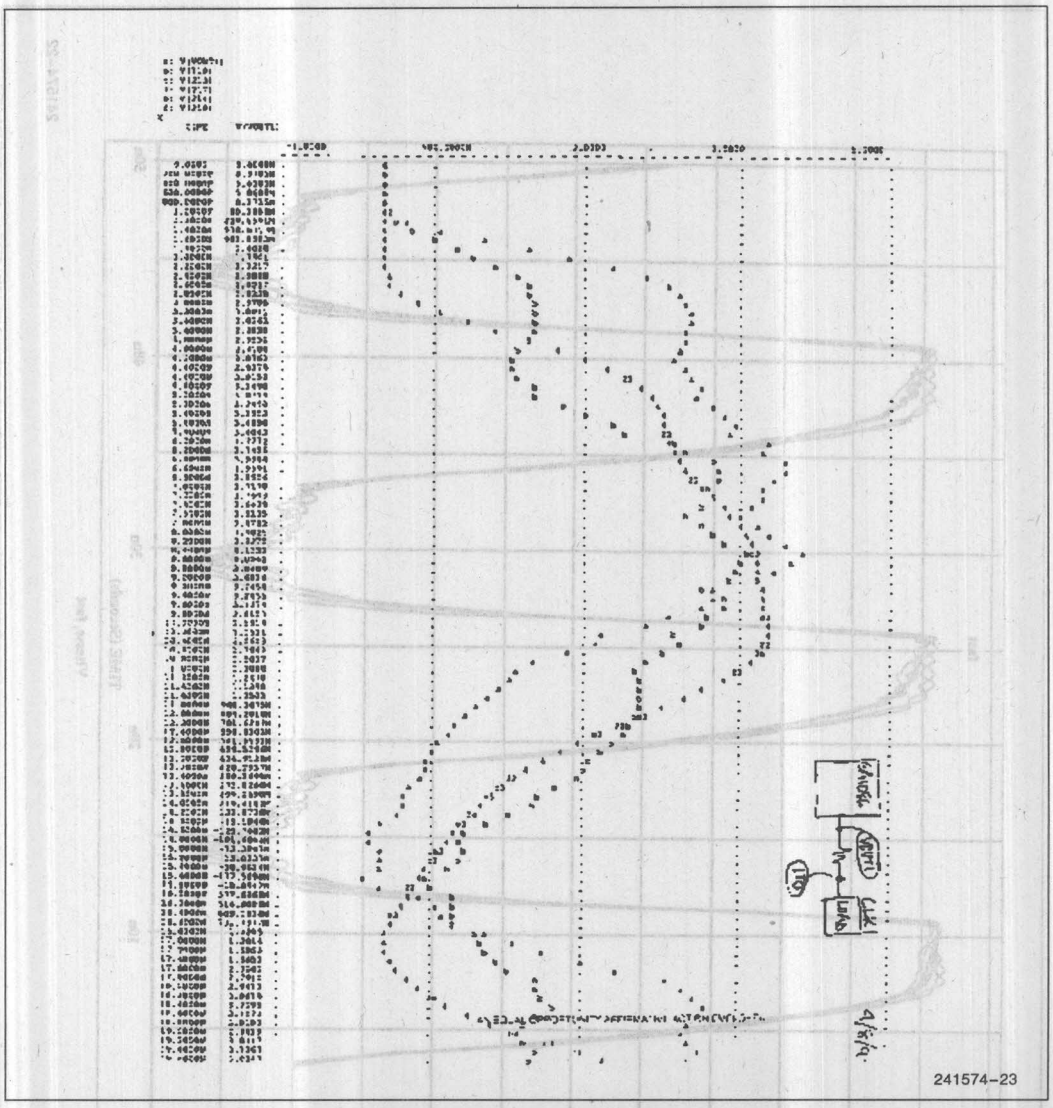


Figure 23. Triquint Waveform

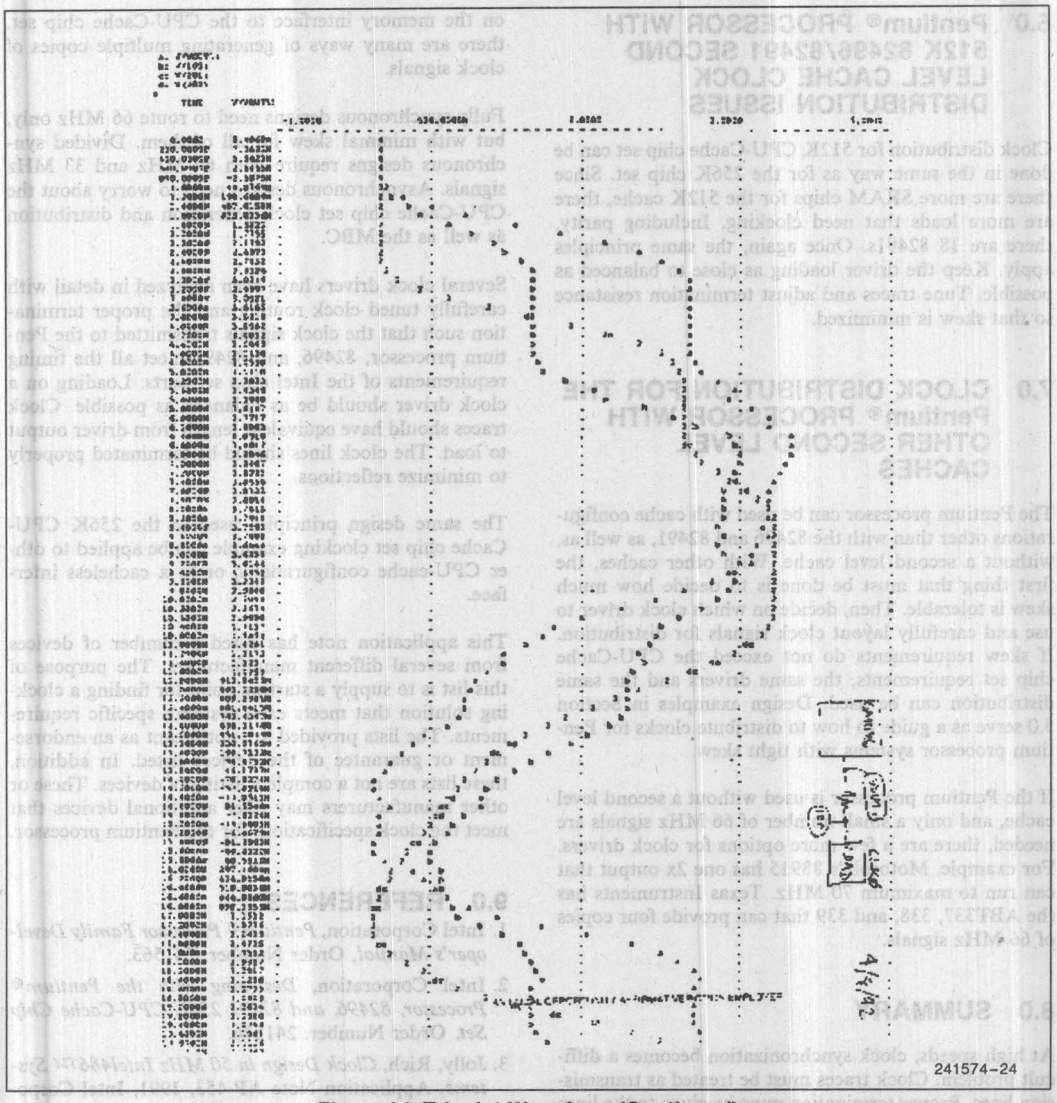


Figure 24. Triquint Waveform (Continued)

6.0 Pentium® PROCESSOR WITH 512K 82496/82491 SECOND LEVEL CACHE CLOCK DISTRIBUTION ISSUES

Clock distribution for 512K CPU-Cache chip set can be done in the same way as for the 256K chip set. Since there are more SRAM chips for the 512K cache, there are more loads that need clocking. Including parity, there are 18 82491s. Once again, the same principles apply. Keep the driver loading as close to balanced as possible. Tune traces and adjust termination resistance so that skew is minimized.

7.0 CLOCK DISTRIBUTION FOR THE Pentium® PROCESSOR WITH OTHER SECOND LEVEL CACHES

The Pentium processor can be used with cache configurations other than with the 82496 and 82491, as well as, without a second level cache. With other caches, the first thing that must be done is to decide how much skew is tolerable. Then, decide on which clock driver to use and carefully layout clock signals for distribution. If skew requirements do not exceed the CPU-Cache chip set requirements, the same drivers and the same distribution can be used. Design examples in Section 5.0 serve as a guide to how to distribute clocks for Pentium processor systems with tight skew.

If the Pentium processor is used without a second level cache, and only a small number of 66 MHz signals are needed, there are a few more options for clock drivers. For example, Motorola's 88915 has one 2x output that can run to maximum 70 MHz. Texas Instruments has the ABT337, 338, and 339 that can provide four copies of 66 MHz signals.

8.0 SUMMARY

At high speeds, clock synchronization becomes a difficult problem. Clock traces must be treated as transmission lines. Proper termination must be given to the lines to ensure good signal quality. The Pentium processor, with operating frequencies of 60 MHz and 66 MHz, has tight clock requirements. Together with the 82496 Cache Controller and 82491 Cache SRAM, the CPU-Cache chip set must be synchronized with minimal skew.

For the Pentium processor clocking, the most critical parameters are skew and rise and fall times. Depending on the memory interface to the CPU-Cache chip set, there are many ways of generating multiple copies of clock signals.

Fully synchronous designs need to route 66 MHz only, but with minimal skew for all of them. Divided synchronous designs require both 66 MHz and 33 MHz signals. Asynchronous designs need to worry about the CPU-Cache chip set clock generation and distribution as well as the MBC.

Several clock drivers have been analyzed in detail with carefully tuned clock routing and the proper termination such that the clock signals transmitted to the Pentium processor, 82496, and 82491 meet all the timing requirements of the Intel chip set parts. Loading on a clock driver should be as balanced as possible. Clock traces should have equivalent length from driver output to load. The clock lines should be terminated properly to minimize reflections.

The same design principles used in the 256K CPU-Cache chip set clocking example can be applied to other CPU-cache configurations, or to a cacheless interface.

This application note has listed a number of devices from several different manufacturers. The purpose of this list is to supply a starting point for finding a clocking solution that meets each system's specific requirements. The lists provided are not meant as an endorsement or guarantee of the devices listed. In addition, these lists are not a complete listing of devices. These or other manufacturers may offer additional devices that meet the clock specifications for the Pentium processor.

9.0 REFERENCES

1. Intel Corporation, *Pentium® Processor Family Developer's Manual*, Order Number: 241563.
2. Intel Corporation, *Designing with the Pentium® Processor, 82496, and 82491 256K CPU-Cache Chip Set,* Order Number: 241576.
3. Jolly, Rich, *Clock Design in 50 MHz Intel486™ Systems*, Application Note AP-453, 1991, Intel Corporation, Santa Clara, CA.
4. Blood, William R., Jr., *MECL System Design Handbook*, 1988, Motorola Inc.
5. Hanke, Chris and Tharalson, Gary, *Low Skew Clock Drivers and their System Design Considerations*, Application Note AP-1091, Motorola Inc., 1990.

APPENDIX A
CLOCK DRIVER MANUFACTURERS

The following is a list of contacts for the clock driver manufacturers listed in this application note. It is not meant to be an exhaustive list of all possible solutions. It is meant as a starting point for system designers to assist in finding a clock solution that meets their system requirements.

AMCC

United States:
Headquarters
6195 Lusk Boulevard
San Diego, CA 92121-2793
Ph: 619-450-9333 or 800-PLL-AMCC (755-2622)
FAX: 619-450-9885

Europe:

Amega Electronics
Basingstoke, RG24OPF, U.K.
Ph: 011/44-256-843166

Japan:

Teksel Co., Ltd.
Kawasaki 213
Tokyo, Japan
Ph: 011/81-448127430

Israel:

EIM
Petach Tiqva, Israel
Ph: 011/972-3-9233257

AT&T Microelectronics

AT&T Customer Response Center
Ph: 800-372-2447 x773

Danny George
555 Union Blvd.
Allentown, PA 18103
50N2G2100
Ph: 215-439-6697

Cypress

Sean Dingman
3901 N. 1st St.
San Jose, CA 95134
408-943-2743

ICS

Bruce Rogers
Technical Marketing Manager
2626 Van Buren Ave.
P.O. Box 968
Valley Forge, PA 19482
215-666-1900

Intel PLD BU International Contact List

United States:

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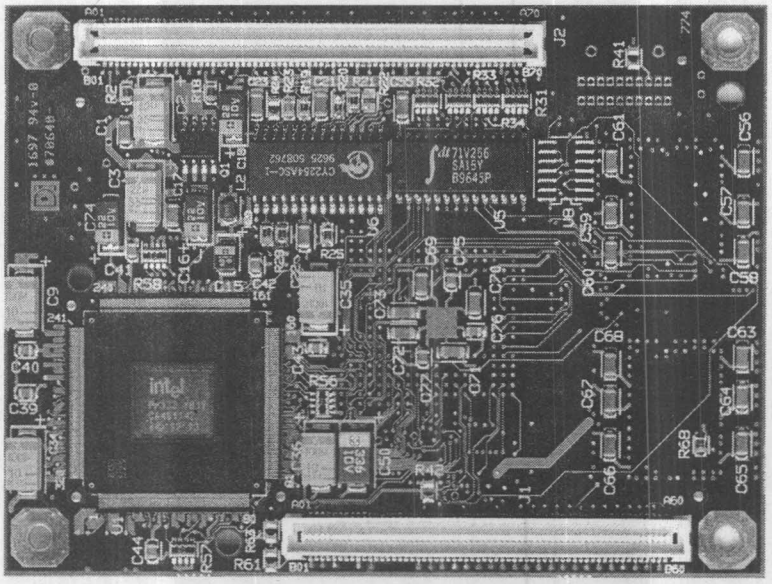
Chapter 3: Embedded Processor Modules

Chapter 3: Embedded Processor Modules

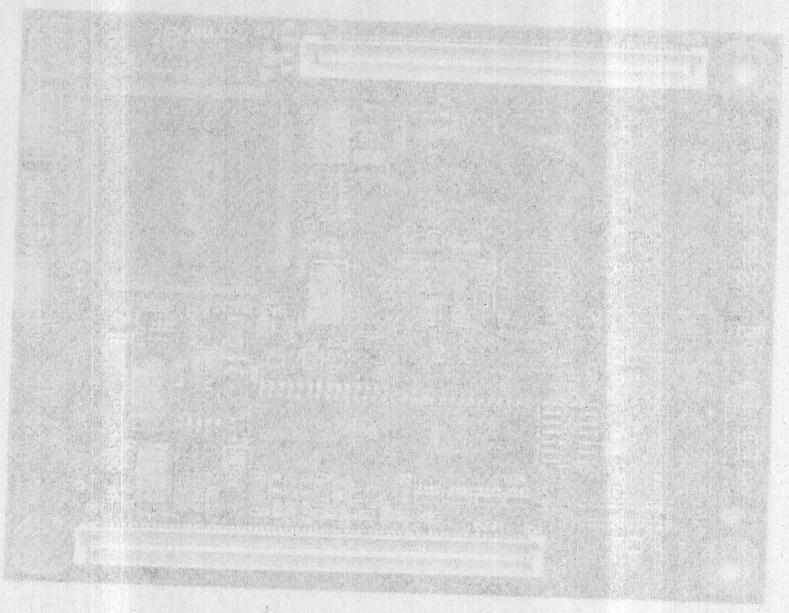
- **Technology with internal/bus frequency of 166/66 (EMBMOD166)**
- **Processor (host) reference and PCI clock generation**
- **Voltage regulation supports processor core input voltage of 2.9 V (EMBMOD133) or 2.45 V (EMBMOD166)**
- **PCI 2.1 compliant**
- **Integrated second-level cache controller**
- **Integrated DRAM controller**
- **Optional parity**
- **Optional error checking and correction**

The Intel Embedded Processor Module is a fundamental building block for the embedded system designer. The Intel Embedded Processor Module incorporates an Intel Pentium® processor, a 256-Kbyte (EMBMOD133) or 512-Kbyte (EMBMOD166) second-level cache, an Intel 430HX PCIset 82439HX System Controller (TXC), a clock generator and a voltage regulator on a single printed circuit board.

The Mobile Pentium® Processor with MMX™ Technology and the Pentium® Processor with Voltage Reduction Technology may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.



November 1997 **Order Number:** 273105-003



1.0 Introduction

The Intel Embedded Processor Module is a fundamental building block for the embedded system designer. The Intel Embedded Processor Module incorporates an Intel Pentium® processor, a 256-Kbyte or 512-Kbyte second level cache, an Intel 430HX PCIset 82439HX System Controller (TXC), a clock generator and a voltage regulator on a single printed circuit board.

Intel's PCIset architecture allows for physical partitioning at both the PCI and DRAM interface. Therefore the electrical interconnect defined for the Intel Embedded Processor Module includes the PCI bus, DRAM memory bus and some additional PCI sideband signals. An on-board voltage regulator provides the DC conversion from the system DC voltage to the processor's core voltage.

Building around the modular design gives the embedded system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards
- No requirement for manufacturing capabilities on the Tape Carrier Package (TCP) processors
- Faster Time to Market
- Future modules provide an upgrade path using a standard interface

The 430HX PCIset consists of two VLSI devices: the 82439HX System Controller (TXC), and the 82371SB PCI ISA IDE Xcelerator (PIIX3). The system manufacturer's motherboard which connects to the module must include the PIIX3 device.

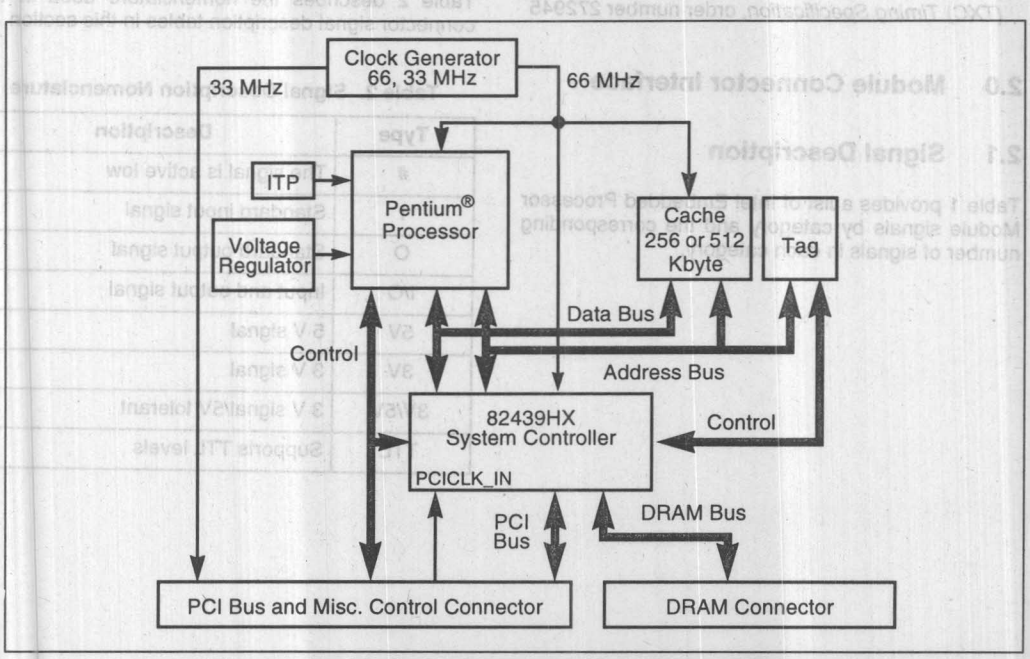


Figure 1. Intel Embedded Processor Module Block Diagram

1.1 Related Documents

- *Intel Packaging Handbook*, order number 240800
- *AP-757, Embedded Processor Module Design Guide*, order number 273120
- *AP-759, Embedded Processor Module Thermal Design Guide*, order number 273143
- *Pentium® Processor with Voltage Reduction Technology at 75/100/120/133/150 MHz* datasheet, order number 242557 (EMBMOD133)
- *Mobile Pentium® Processor with MMX™ Technology* datasheet, order number 243292 (EMBMOD166)
- *Pentium® Processor Family Developer's Manual*, order number 241428
- *Intel Architecture Software Developer's Manual* Vols. 1 and 2, order numbers 243190 and 243191
- *Intel 430HX PCIset 82439HX System Controller (TXC)* datasheet, order number 290551
- *Intel 430HX PCIset 82439HX System Controller (TXC) Timing Specification*, order number 272945

2.0 Module Connector Interface

2.1 Signal Description

Table 1 provides a list of Intel Embedded Processor Module signals by category and the corresponding number of signals in each category.

Table 1. Module Connector Signal Summary

Signal Group	Number
Memory	103
PCI Bus	56
Processor/PIIX3 sideband	10
Clocks	10
Voltage: 3.3 V	27
Voltage: 5.0 V	9
ITP/JTAG	1
Ground	30
Reserved/NC	14
Total	260

Table 2 describes the nomenclature used in the connector signal description tables in this section.

Table 2. Signal Description Nomenclature

Type	Description
#	The signal is active low
I	Standard input signal
O	Standard output signal
I/O	Input and output signal
5V	5 V signal
3V	3 V signal
3V/5V	3 V signal/5V tolerant
TTL	Supports TTL levels

2.2 J1 Connector Signal Description (120-Pin)

Table 3 lists the Intel Embedded Processor Module J1 interface signals. The 120-pin J1 connector contains the PCI, processor/PIIX3 sideband, Power, Ground, and Clock signals.

Table 3. J1 Connector Signal Description (Sheet 1 of 3)

Signal[1]	Type	Description
COREV_SENSE	O	**Power Good** on processor core.
3.3V	I	**3.3 Volt** supply voltage.
12MHZ	O	**12 MHz Clock Signal:** Keyboard Clock.
14.318MHZ	O	**14.318 MHz Reference Clock.**
24MHZ	O	**24 MHz Clock Signal:** I/O Clock.
A20M#	I	**Address Bit 20 Mask:** When enabled, this causes the processor to emulate the address wraparound at 1 Mbyte, which occurs on the Intel 8086 processor.
AD[31:0]	I/O 5V	**Address/Data** is the standard PCI address and data lines. An address is driven with FRAME# assertion. Data is driven or received in following clocks.
C/BE[3:0]#	I/O 5V	**Command/Byte Enable:** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
CPURST	I[2]	**CPU Reset:** The PIIX3 asserts CPURST to reset the CPU. The PIIX3 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven synchronously to the rising edge of PCICLK. When a hard reset is initiated through the RC register, the PIIX3 resets its internal registers to the default state.
DBRST	O	**Debugger Reset Output:** A debugger may assert DBRESET (high) while performing a "Reset All" or "Reset Target" debugger commands. Connect DBRESET to the system reset circuitry such that the system and processor are reset when DBRESET is asserted. This signal is asynchronous.
DEVSEL#	I/O 5V	**Device Select:** This signal is driven by the TXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
FERR#	O	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the CPU. IGNNE# is only used when the PIIX3 coprocessor error reporting function is enabled in the XBCSA Register. When FERR# is asserted, the PIIX3 generates an internal IRQ13 to its interrupt controller unit. The PIIX3 then asserts the INTR output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active. FERR# has a weak internal pull-up used to ensure a high level when the coprocessor error function is disabled.
FRAME#	I/O 5V	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GND	I	**Signal Ground.**

NOTES:

1. All signals in the PCI interface conform to the PCI Revision 2.1 specification.
2. Signals are open drain on the 82371SB and require an external pull-up resistor on the system manufacturer's motherboard which connects to the module.

Table 3. J1 Connector Signal Description (Sheet 2 of 3)

Signal[1]	Type	Description
GNT[3:0]#	O 5V	**PCI Grant:** Permission is given to the master to use PCI. Weak external pull-up resistors are required on these signals.
IGNNE#	I[2]	**Ignore Error:** This signal is connected to the ignore error pin on the CPU. IGNNE# is only used when the PIIX3 coprocessor error reporting function is enabled in the XBCSA Register. When FERR# is asserted, indicating a coprocessor error, a write to the Coprocessor Error Register (F0H) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. When FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted.
INIT	I[2]	**Initialization:** The PIIX3 asserts INIT when it detects a shutdown special cycle on the PCI Bus or when a soft reset is initiated via the RC Register.
INTR	I[2]	**CPU Interrupt:** INTR is driven by the PIIX3 to signal the CPU that an interrupt request is pending and needs to be serviced. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state.
IRDY#	I/O 5V	**Initiator Ready** is asserted when the initiator is ready for a data transfer.
LOCK#	I/O 5V	**Lock** is used to establish, maintain, and release resource locks on PCI.
N/C	—	**No Connect.**
NMI	I[2]	**Non-maskable Interrupt:** NMI is used to force a non-maskable interrupt to the CPU. The PIIX3 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed.
PAR	I/O 5V	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0].
PCI_CLK[0:5]	O	**33 MHz PCI Clock Outputs.**
PCICLK_IN	I	**Input 82439HX PCI Clock.**
PCIRST#	I	**PCI Reset:** This signal has two functions, depending on the programming of the APIC Chip Select bit (XBCS Register). See the APIC Signal Description for the APICACK# function. The PIIX3 asserts PCIRST# to reset devices that reside on the PCI Bus. The PIIX3 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven active for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK.
PHLD#	I 5V	**PCI Hold:** This signal comes from the expansion bridge. It is the bridge request for PCI. The PHLD# protocol supports passive release. A weak external pull-up resistor is required on this signal.
PHLDA#	O 5V	**PCI Hold Acknowledge:** This signal is driven by the TXC to grant PCI to the expansion bridge. The PHLDA# protocol supports passive release. A weak external pull-up resistor is required on this signal.

NOTES:

1. All signals in the PCI interface conform to the PCI Revision 2.1 specification.
2. Signals are open drain on the 82371SB and require an external pull-up resistor on the system manufacturer's mother-board which connects to the module.

	5V	action.
STPCLK#	I[2]	**Stop Clock:** STPCLK# is an active low synchronous output that is asserted by the PIIX3 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK.
TRDY#	I/O 5V	**Target Ready** is asserted when the target is ready for a data transfer.

NOTES:

1. All signals in the PCI interface conform to the PCI Revision 2.1 specification.
2. Signals are open drain on the 82371SB and require an external pull-up resistor on the system manufacturer's motherboard which connects to the module.

CAS[7:0]#	O 3V	**Column Address Strobe:** These pins select the DRAM column.
GND	I	**Signal Ground.**
MA[11:2]	O 3V	**Memory Address:** This is the row and column address for DRAM. These buffers include programmable size selection.
MAA[1:0]	O 3V	**Memory Address Copy A:** One copy of the memory addresses (MA[11:2]) that change during a burst read or write of DRAM. Size selection of the I/O buffers on these pins on the 82439HX is programmable.
MAB[1:0]	O 3V	**Memory Address Copy B:** A second copy of the memory addresses (MA[11:2]) that change during a burst read or write of DRAM. Size selection of the I/O buffers on these pins on the 82439HX is programmable.
MD[63:0]	I/O 3V/5V TTL	**Memory Data:** These signals are connected to the DRAM data bus.
MPD[7:0]	I/O 3V/5V TTL	**Memory Parity Data:** These signals connect to the DRAM parity or ECC bits. The MPD pins have similar timing and drive capability to the MD pins. ECC versus parity operation is determined by the PCI Control Register (PCON[DDIM] field) in the 82439HX. These signals have internal weak pull-down resistors, the same as the MD signals. These signals are always driven during write cycles, regardless of the existence of parity memory.
MWE#	O 3V	**Memory Write Enable:** Use MWE# as the write enable for the memory data bus. This signal has a programmable size selection, which is selected through the DRAM Extended Control Register (DRAMEC[MAD] field) in the 82439HX.
N/C	—	**No Connect.**
RAS[7:0]#	O 3V	**Row Address Strobe:** These pins select the DRAM row.

NOTE: All 3 V output signals can drive 5 V TTL inputs.

2.4 ITP/JTAG Connector Signal Description

Table 5 lists the Intel Embedded Processor Module Intel Test Port (ITP) interface signals. The 20-pin connector will *not* be populated on production modules. The ITP connector can be attached by the system integrator to gain access to the debug capabilities within the processor.

Table 5. Intel Test Port (ITP) Interface Signal Description

Signal Name	Dir	Description
DBRESET	I	**Debugger Reset Output:** A debugger may assert DBRESET (high) while performing "Reset All" or "Reset Target" debugger commands. DBRESET should be connected to the system reset circuitry so that the system and processor are reset when DBRESET is asserted. This signal is asynchronous.
GND		**Signal Ground.**
INIT	O	**Processor Initialization:** (Pentium processor signal) A debugger may use INIT to support emulating through the CPU INIT sequence while maintaining breakpoints or breaking on INIT.
N/C		**No Connect.** Leave this pin unconnected.
PRDY	O	**Probe Ready:** From the PRDY pin on the Pentium processor.
RESET	O	**Reset Signal:** (Pentium processor signal) A debugger may use RESET to support emulating through the reset while maintaining breaking on RESET.
R/S#	I	**Run/Stop:** Connect to the R/S# pin on the Pentium processor.
TCK	I	**Boundary scan clock.** (Pentium processor signal)
TDI	I	**Boundary scan data input:** (Pentium processor signal) This signal connects to TDI of the Pentium Processor.
TDO	O	**Boundary scan data output:** (Pentium processor signal) This signal connects to the TDO from the Pentium processor.
TMS	I	**Boundary scan mode select** (Pentium processor signal).
TRST#	I	**Boundary Scan Reset** (Pentium processor signal).
V_{CC}		**V_{CC}** from the Pentium processor system. A debugger uses this signal to sense that system power is on. Connect this signal to V_{CC} through a 1 KΩ (or smaller) resistor.

2.5 J1 Connector Pin Assignment (120-Pin)

Table 6 lists the signals for each pin of the 120-pin J1 connector. See Figure 6 for connector orientation.

Table 6. PCI Connector Pin Assignment (J1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	INIT	A31	GND	B01	3.3V	B31	AD22
A02	CPURST	A32	PHLDA#	B02	STPCLK#	B32	3.3V
A03	3.3V	A33	AD21	B03	SMI#	B33	LOCK#
A04	A20M#	A34	AD19	B04	GND	B34	AD20
A05	INTR	A35	3.3V	B05	NMI	B35	AD24
A06	IGNNE#	A36	FRAME#	B06	FERR#	B36	GND
A07	GND	A37	AD17	B07	N/C	B37	AD18
A08	24MHZ	A38	REQ0#	B08	3.3V	B38	AD16
A09	N/C	A39	GND	B09	COREV_SENSE	B39	IRDY#
A10	12MHZ	A40	CBE2#	B10	N/C	B40	3.3V
A11	3.3V	A41	AD15	B11	14.318MHZ	B41	CBE1#
A12	N/C	A42	TRDY#	B12	GND	B42	GNT0#
A13	PCICLK_1	A43	3.3V	B13	N/C	B43	AD14
A14	N/C	A44	AD13	B14	PCICLK_2	B44	GND
A15	GND	A45	REQ1#	B15	N/C	B45	AD12
A16	PCICLK_3	A46	AD11	B16	3.3V	B46	DEVSEL#
A17	N/C	A47	GND	B17	PCICLK_4	B47	AD10
A18	PCICLK_5	A48	AD9	B18	N/C	B48	3.3V
A19	3.3V	A49	AD8	B19	PCICLK_0	B49	GNT1#
A20	DBRST	A50	AD7	B20	GND	B50	CBE0#
A21	N/C	A51	3.3V	B21	PCICLK_IN	B51	REQ2#
A22	N/C	A52	STOP#	B22	N/C	B52	GND
A23	GND	A53	AD5	B23	PCIRST#	B53	AD6
A24	N/C	A54	GNT2#	B24	3.3V	B54	AD4
A25	AD30	A55	GND	B25	AD31	B55	PAR
A26	AD28	A56	AD3	B26	AD29	B56	3.3V
A27	3.3V	A57	REQ3#	B27	AD27	B57	AD2
A28	AD26	A58	AD1	B28	GND	B58	SERR#
A29	PHLD#	A59	3.3V	B29	AD25	B59	GNT3#
A30	AD23	A60	AD0	B30	CBE3#	B60	GND

					MA3	B40	MPD4
A06	MA4	A41	3.3V	B06	MA3	B41	MPD0
A07	MA2	A42	MPD6	B07	5.0V	B42	CAS6#
A08	MA8	A43	RAS0#	B08	MA11	B43	3.3V
A09	GND	A44	MPD7	B09	MA7	B44	MPD1
A10	MA10	A45	GND	B10	MA9	B45	MPD5
A11	MD0	A46	RAS2#	B11	5.0V	B46	RAS1#
A12	MD32	A47	MD08	B12	MD48	B47	GND
A13	5.0V	A48	MD40	B13	MD16	B48	MPD3
A14	MD33	A49	3.3V	B14	MD17	B49	RAS3#
A15	MD01	A50	MD25	B15	GND	B50	MD41
A16	MD49	A51	MD24	B16	MD02	B51	3.3V
A17	5.0V	A52	MD56	B17	MD34	B52	MD30
A18	MD35	A53	GND	B18	MD18	B53	MD44
A19	MD50	A54	MD26	B19	5.0V	B54	MD57
A20	MD03	A55	MD09	B20	MD19	B55	GND
A21	GND	A56	MD46	B21	MD36	B56	MD11
A22	MD04	A57	3.3V	B22	MD51	B57	MD10
A23	RAS7#	A58	MD42	B23	5.0V	B58	MD12
A24	RAS5#	A59	MD59	B24	MD05	B59	3.3V
A25	5.0V	A60	MD58	B25	MD52	B60	MD60
A26	MD20	A61	GND	B26	RAS6#	B61	MD27
A27	RAS4#	A62	MD43	B27	3.3V	B62	MD28
A28	MD53	A63	MD61	B28	MD21	B63	GND
A29	GND	A64	MD29	B29	MD37	B64	MD45
A30	CAS7#	A65	3.3V	B30	CAS3#	B65	MD13
A31	MD22	A66	MD62	B31	GND	B66	MD63
A32	MD38	A67	MD14	B32	MD06	B67	3.3V
A33	3.3V	A68	MD47	B33	CAS1#	B68	MD31
A34	MD39	A69	GND	B34	MD07	B69	MD15
A35	MD54	A70	N/C	B35	3.3V	B70	GND

2.7 ITP/JTAG Connector Pin Assignment

Table 8 lists the signals for each pin of the 20-pin ITP/JTAG connector. For connector orientation, refer to the ITP connector manufacturer's documentation.

Table 8. ITP Connector Pin Assignment (J3)

Pin	Signal	Pin	Signal
1	INIT	11	PRDY
2	DBRESET	12	TDI
3	RESET	13	TDO
4	GND	14	TMS
5	N/C	15	GND
6	3.3V	16	TCLK
7	R/S#	17	GND
8	GND	18	TRST#
9	N/C	19	N/C
10	GND	20	N/C

3.0 Functional Description

3.1 Embedded Processor Module

The Intel Embedded Processor Module uses the Pentium® Processor with Voltage Reduction Technology (EMBMOD133) or the Mobile Pentium® Processor with MMX™ Technology (EMBMOD166) with an internal frequency of 133 or 166 MHz (respectively) and a bus frequency of 66 MHz.

3.2 L2 Cache

The Pentium processor's internal cache is complemented by a second-level cache using 256 Kbytes (EMBMOD133) or 512 Kbytes (EMBMOD166) of high speed synchronous pipelined burst SRAM. The L2 cache can support up to 64 Mbytes of system memory. The L2 cache has a 3.3 V interface to the host system bus and the 82439HX System Controller (TXC). The L2 cache subsystem includes a 32 K x 8 cache tag RAM (provided on module). The upper address bits of the tag chip are disabled.

3.3 System Controller

Intel's 82439HX system controller is a highly integrated device that combines the Pentium processor bus controller, the DRAM controller, second-level cache controller and the PCI bus controller into one component. The 82439HX is PCI 2.1 compliant. The PCI bus for the Intel Embedded Processor Module operates at 33 MHz (one-half the host frequency) and is provided by the system baseboard. The system designer must take one of the six PCI clocks generated on the processor module, deskew the signal and route it back to the processor module. This ensures that the Host-to-PCI clock skew specification is met.

Refer to Intel's latest revision of the 430HX PCIset datasheets for complete details.

3.4 Clock Generation

A clock synthesizer circuit is provided on the Intel Embedded Processor Module. The clock generator accepts a 14.318 MHz input signal from a crystal oscillator. The clock generator provides the 66 MHz clock needed for the Pentium processor and the 82439HX, and the 33 MHz clocks needed for the

82439HX and the PCI interface. Additional outputs from the clock circuit are buffered 14.318 MHz, 24 MHz, and 12 MHz signals. Six buffered copies of the 33 MHz PCI clock signal are available.

3.5 Voltage Regulation

The Pentium processor with Voltage Reduction Technology requires 2.9 V for the core and 3.3 V for the I/O interface. The Pentium processor with MMX™ Technology requires 2.45 V for the core and 3.3 V for the I/O interface.The Intel Embedded Processor Module has an integrated voltage regulation circuit on-board to provide the 2.9 V or 2.45 V processor core requirement. The input to the voltage regulation circuit is 5.0 V and is provided by the system baseboard. The voltage regulator can supply a minimum of 3.0 A (on the 133 MHz module) or 4.1 A (on the 166 MHz module) to the Pentium processor. The voltage regulator is a switching regulator which increases the efficiency of the circuit as compared to a linear regulator.

3.6 Connectors

The Intel Embedded Processor Module interfaces to the I/O subsystem via two high density connectors. The 140-pin connector (J2) contains the DRAM interface, power and ground connections. The 120-pin connector (J1) contains the PCI interface, processor/PIIX3 sideband signals, clocks, power and ground connections. The connectors are low profile, with a 5 mm stacking height, and high density (0.8 mm pitch). The connectors minimize baseboard-to-module spacing.

The module also provides the ability to add an ITP connector to facilitate debug and software development. The ITP connector is not installed on production modules. The following components must be installed for the ITP to function correctly:

Table 9. Additional Components for ITP

Location	Component
U8	74LVQ04 Hex Inverter
R41	1.0 KΩ Resistor
R42	0Ω Resistor

All pins labeled N/C are "no connect" pins and are reserved for future use.

The connectors should not be used as the only mechanical connection to the system baseboard. Use the four mounting holes provided on the module as the mechanical interface to the system baseboard. The four mounting holes are electrically connected to ground.

3.7 Thermal Considerations

The Intel Embedded Processor Module (EMBMOD133) uses a passive heat sink as the thermal solution. The heat sink is mechanically attached to the topside of the module and uses an electrically and thermally conductive compound for the module-to-heat sink interface.

Figure 2 shows the orientation of the module in the 0 and 180 degree airflow rotation. Figure 3, Figure 4 and Table 10 contains the thermal characterization data showing the relationship between θ_{CA} and airflow required to ensure that the maximum case temperature is not exceeded. The maximum case temperature is 95° C for the Pentium processor and 85° C for the 82439HX System Controller and SRAM.

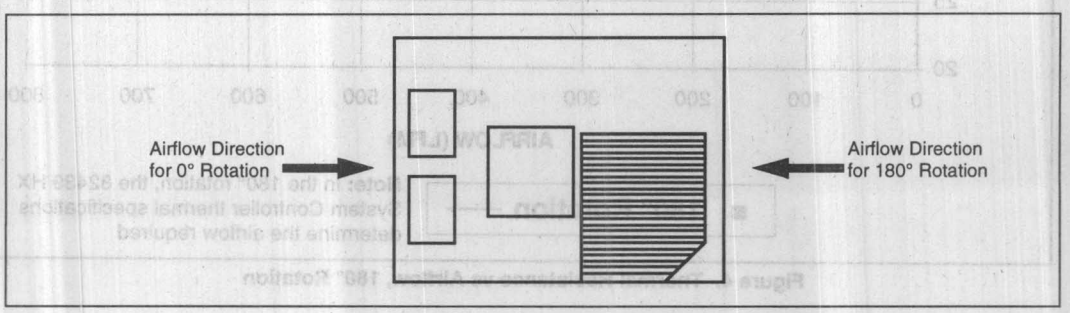


Figure 2. Airflow Direction

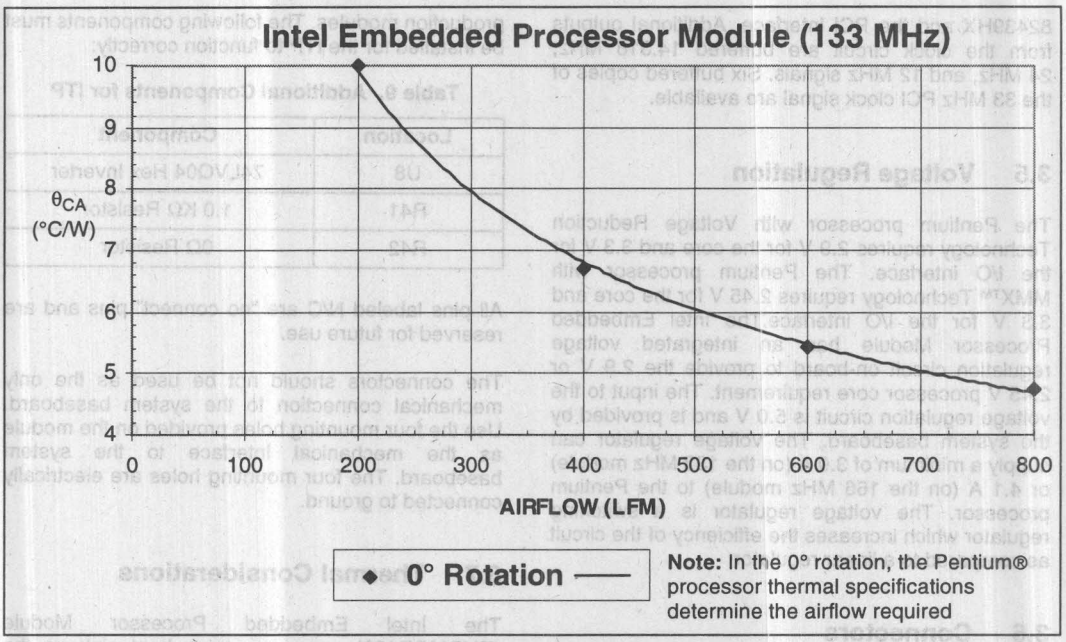


Figure 3. Thermal Resistance vs Airflow, 0° Rotation

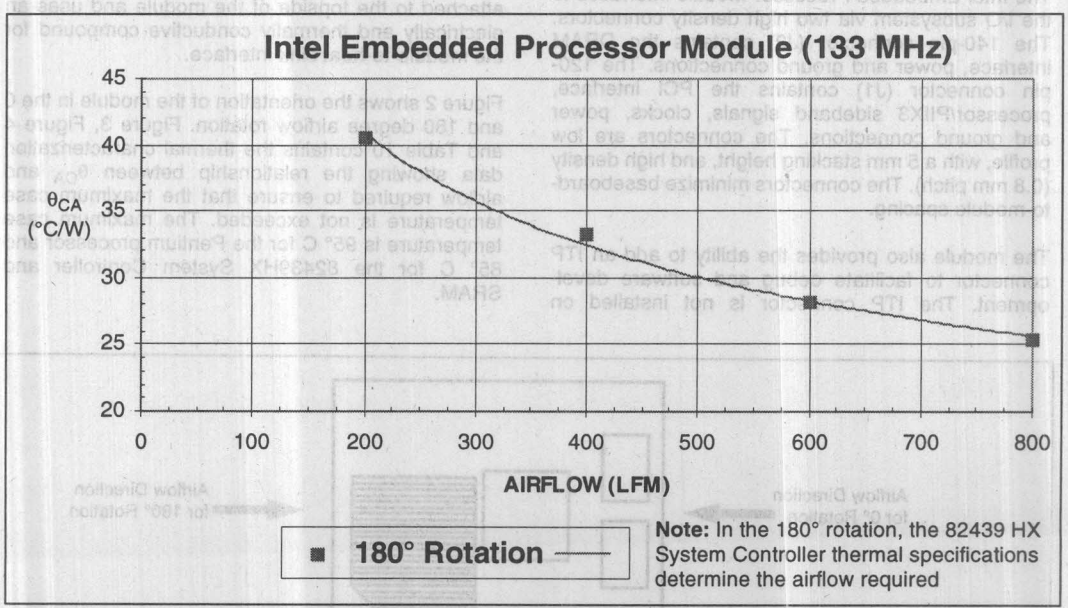


Figure 4. Thermal Resistance vs Airflow, 180° Rotation

Table 10. Tested Airflows and Rotation

Airflow	θ_{CA} (0° Rotation)	θ_{CA} (180° Rotation)
800	4.8	25.4
600	5.4	28.2
400	6.7	33.2
200	10.0	40.5

The test conditions were:

- All measurements were taken in an "open air" environment (no enclosure around the module); T_A = 50° C
- **0° rotation:** Airflow direction is from the 82439HX System Controller (BGA) to the Pentium processor (TCP); T_C = 95° C
- **180° rotation:** Airflow direction is from the Pentium processor (TCP) to the 82439HX System Controller (BGA); T_C = 85° C

The equation used to calculate θ_{CA}:

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

Where:

θ_{CA} = Case-to-Ambient Thermal Resistance (°C/ W)
T_C = Case Temperature
T_A = Ambient Temperature
P= Power in Watts

When considering the thermal requirements for the Embedded Processor Module in a specific application, always ensure that the maximum case temperature is not exceeded for any component on the module, regardless of the orientation of the module. Refer to the Intel Embedded Processor Module Thermal Design Guide (order number 273143).

The thermal solution for the EMBMOD166 is under development. The thermal characterization data for the EMBMOD166 will be published when it becomes available.

3.7.1 Maximum and Typical Power Design Examples

Below is an example of determining the airflow required during maximum power consumption:

T_C (TCP) = 95° C; T_C (BGA) = 85° C
TA = 50° C
P_{TCP} = 7.9 W, P_{BGA} = 1.2 W
θ_{CA} (TCP, 0° rotation) = 5.7 °C/W
θ_{CA} (BGA, 180° rotation) = 29.1 °C/W

Figure 3 and Figure 4 indicate that this example would require about 550 LFM in the 0° rotation, and about 550 LFM in the 180° rotation.

The next example shows the same calculation for typical power consumption:

T_C (TCP) = 95° C; T_C (BGA) = 85° C
TA = 50° C
P_{TCP} = 3.5 W, P_{BGA} = 1.0 W
θ_{CA} (TCP, 0° rotation) = 12.9 °C/W
θ_{CA} (BGA, 180° rotation) = 35.0 °C/W

Figure 3 and Figure 4 indicate that this example would require about 100 LFM in the 0° rotation, and about 325 LFM in the 180° rotation.

3.8 Electrical Design

Clock signals generated on the module are routed on impedance-controlled signal layers. To minimize clock skew, the 66 MHz clock lines are matched and have a length of 9.3 inches. Extra space was added between the clock lines and other signals to minimize signal crosstalk. The lengths of the 33 MHz clock lines are also matched. The 33 MHz clock input on the 82439HX comes from the external connector. Series termination resistors are provided

The design rules for the 430HX PCIset were followed on the module. Pentium processor signals that must be tied off are terminated on the module. PCI signals REQ[3:0]# and GNT[3:0]# are pulled up on the module. All other PCI signals must be terminated on the baseboard. The following signals have space for termination resistors on the module. These resistors are *not* populated on the production modules and must be provided by the host system.

INIT, RESET, A20M#, IGNNE#, SMI#, NMI, INTR, FERR#

A COREV_SENSE signal is provided to the baseboard for power-good sensing. The DBRESET signal from the ITP is provided on the PCI connector for baseboard use (with PWRGOOD). Power-good sensing is done on the baseboard. The baseboard must supply 2.0 A of 3.3 V and 3.5 A (EMBMOD133) or 4.1 A (EMBMOD166) of 5.0 V.

4.1.1 Dimensions and Connector Orientation

Figure 6 shows the board dimensions and the connector orientation for the Intel Embedded Processor Module.

4.1.2 Printed Circuit Board Thickness and Clearance

Figure 7 is a profile view of the Intel Embedded Processor Module showing the nominal thickness of the printed circuit board (0.058 inches) and the maximum module height (0.54 inches). The clearance from the motherboard to the underside of the Embedded Processor Module printed circuit board is fixed by the connector stacking height of 5 mm. Actual clearance varies depending on component thickness and location.

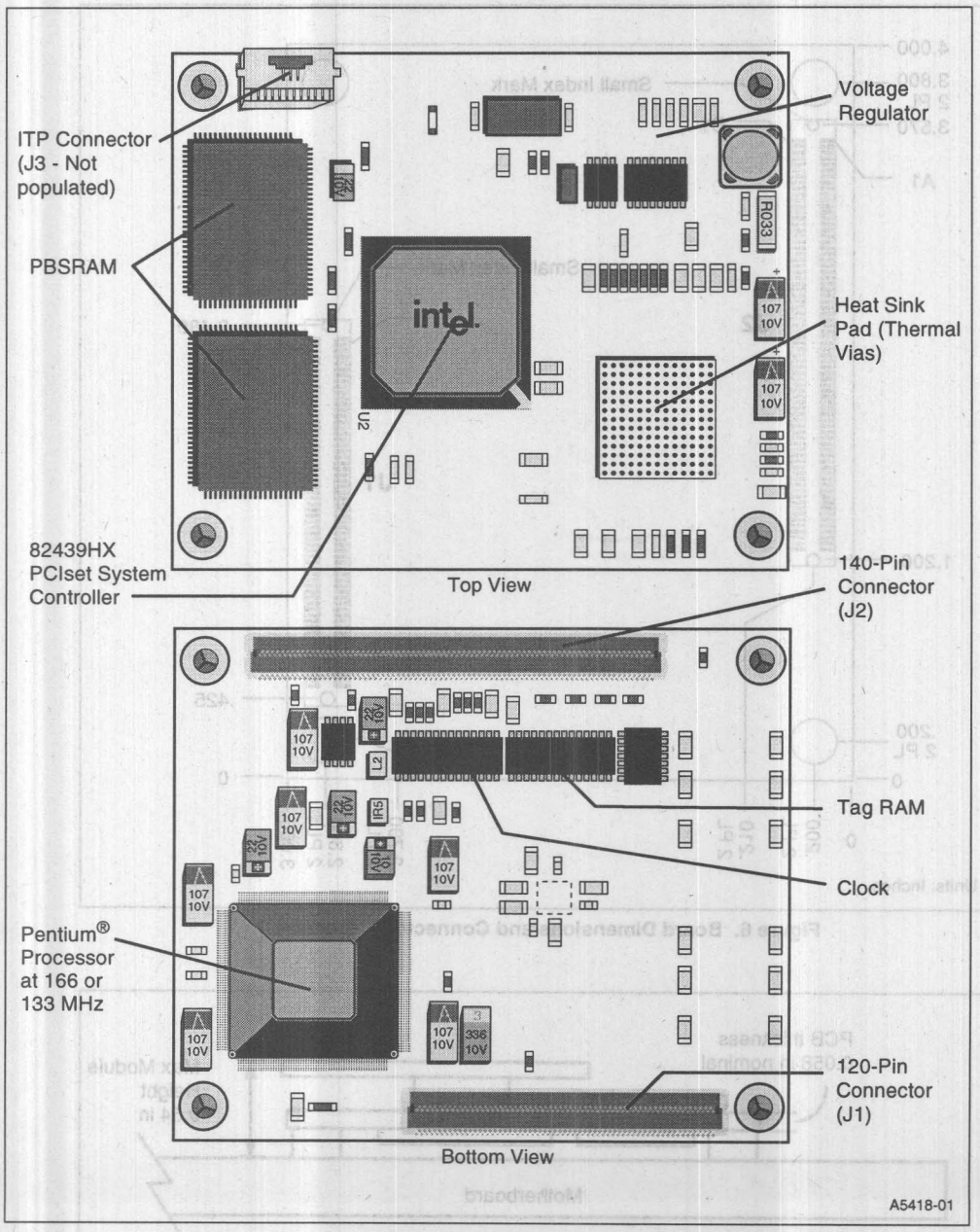


Figure 5. Intel Embedded Processor Module — Top and Bottom View

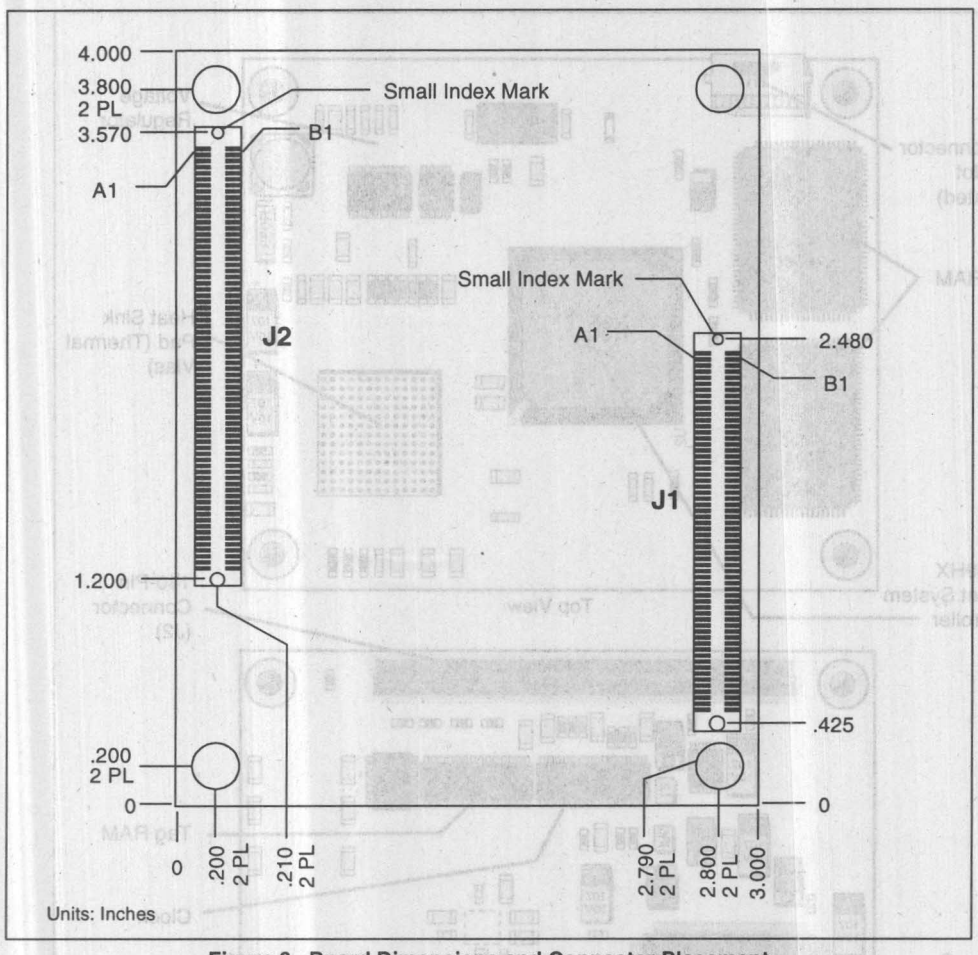


Figure 6. Board Dimensions and Connector Placement

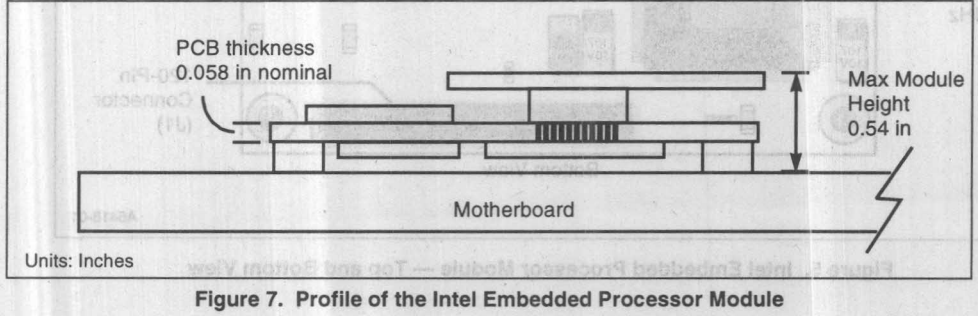


Figure 7. Profile of the Intel Embedded Processor Module

4.2 Connector Specifications

The Intel Embedded Processor Module connectors are surface mount, 0.8 mm pitch, 140-pin and 120-pin connectors. Table 11 summarizes some of the critical specifications for the connectors.

Table 11. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Beryllium Copper
	Housing	Thermoplastic Molded Compound LCP
Electrical	Current	0.5 A
	Voltage	100 VAC
	Termination Resistance	20 mΩ max. @20 mV open circuit with 10 mA
	Insulation Resistance	500 MΩ min. @ 500 VDC
Mechanical	Mating Cycles	100 cycles
	Connector Mating Force	0.9 N (90 gf) max. per contact
	Connector Un-mating Force	0.1 N (10 gf) min. per contact

5.0 Environmental Standards

The environmental standards for this product are being developed. Table 12 provides the parameter list to which specifications will be defined.

Table 12. Environmental Standards

Parameter	Condition	Specification
Temperature	Non-operating Operating	-25 ° C to 65° C 0 ° C to 50 ° C†
Shock	Unpackaged Packaged	Trapezoidal, 30 G, 11 ms Half Sine, 2 ms at 36" Simulated Free Fall
Vibration	Unpackaged Packaged Packaged	5 Hz to 500 Hz, 2.2 gRMS 10 Hz to 500 Hz, 1.0 gRMS 11,800 impacts, 2 Hz to 5 Hz (low frequency)
ESD	Air Discharge	0 to 2 kV (no detectable error)

† Requires minimum of 400 lfpm airflow.

intel®

AP-757
Application Note

Embedded Processor Module Design Guide

September, 1997

Order Number: 273120-001

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AP-757

Application Note

Embedded Processor Module Design Guide

September, 1997

Order Number: 272720-001

1.0 Introduction

The Intel Embedded Processor Module was developed to assist system designers with the challenges of high speed design by taking care of the high speed processor interface. This allows the system designer to concentrate on the I/O subsystems and PCI-bus interface.

This document is a supplement to the *Intel Embedded Processor Module* datasheet (Order No. 273105). The contents of this design guide assist in the development of a system-level platform that uses the Intel Embedded Processor Module.

In this document, the term "system board" refers to the system-level platform (baseboard or motherboard) that the Embedded Processor Module plugs into. Note that the 82371SB (PIIX3) must be used in the system board design.

1.1 Related Documents

Document	Intel Order Number
Intel 430HX PCIset Design Guide	297467
Intel Embedded Processor Module datasheet	273105
PCI Local Bus Specification, Revision 2.1	

2.0 Electrical Layout Considerations

Increasing bus frequencies with fast edge rates place additional demands on system designers. Designing a reliable system requires the use impedance-controlled boards, equalized clock trace lengths, optimized component layout and trace routing, and proper termination.

2.1 Clocks

The Embedded Processor Module contains a Cypress CY2254A* clock synthesizer. The clock synthesizer is fed by a 14.318 MHz crystal oscillator. The clock synthesizer generates four buffered copies of the 66 MHz processor clock, six buffered copies of the 33 MHz PCI clock, a 12 MHz clock, a 24 MHz clock, and two 14.318 MHz reference clocks.

The clocks lines are of matched length to minimize any skew between the processor, the system controller, and the pipeline-burst SRAMs (PBSRAMs). The host clocks are series terminated on the module with 66.5 Ω resistors. The 66 MHz clocks are not routed to the connector.

The six 33 MHz PCI clocks are routed to the 120-pin connector and are of equal length. The PCI clock traces are series terminated with 33.2 Ω resistors. One of the six PCI clocks must be routed back into the Embedded Processor Module through the PCICLK_IN pin on the 120-pin connector. The PCICLK_IN signal is used to drive the 82439HX System Controller PCI interface. The PCICLK_IN trace must be matched with the other PCI clocks on the system board to minimize skew between the Embedded Processor Module and the system board.

Clocks are series terminated on the Embedded Processor Module; the designer must ensure that the system board supports AC termination at the signal destination.

Table 1 lists trace lengths for the Embedded Processor Module clock signals.

Table 1. Clock Trace Lengths on the Intel Embedded Processor Module

Clock Trace	Length
CPU Host Clock	9.35"
PCI Onboard Clocks	2.60"
PCICLK_IN	1.60"

Based on the trace lengths provided in Table 1, the system board requirements are:

Minimum PCI trace length on system board
= CPU Host Clock – PCI Onboard Clock

PCI min = 9.35" – 2.60"
= 6.75"

All PCI Clock traces on the system board must be of equal length (± 250 mils) and at least 6.75" long to maintain the proper relationship between PCI devices and between PCI and host clocks.

The line length of the PCI clock routed back to the Embedded Processor Module must be 1.60" shorter than

- PCI Clock circuits are series terminated on the Embedded Processor Module. The system board must support AC termination.
- All PCI clocks routed on the system board must be at least 6.75"long.
- The trace length of the PCICLK_IN input to the Embedded Processor Module must be 1.60" shorter than the other PCI clocks on the system board. The minimum length required is 5.15".
- The impedance at the connector of the system board should be approximately 65 Ω to match the impedance on the Embedded Processor Module connector.
- Use point-to-point routing topologies whenever possible.
- To minimize EMI concerns, terminate unused PCI and system clocks on the system board.
- Future embedded modules may support higher processor clock frequencies, but the processor bus and PCI bus frequencies will remain the same:
  - Processor I/O bus = 66 MHz
  - PCI Bus = 33 MHz
  - Processor Core = Processor I/O × Ratio; Ratio= 2 (EMBMOD133) or 2.5 (EMBMOD166)

These frequencies are hardwired into the Embedded Processor Module and are not selectable.

2.2 Memory Bus

Follow the design guidelines for the 82439HX system controller when integrating the Embedded Processor Module into a system solution.

NOTE: The Embedded Processor Module supports both fast page mode (FPM) and extended data out (EDO) memory types. Synchronous DRAM is not supported by the Embedded Processor Module.

- Mixed EDO and FPM memory types are not allowed in the same bank. Mixing of memory types between banks is allowed.

For more information on the System Controller design, refer to the *Intel 430HX PCIset Design Guide* (Order No. 297467).

2.3 PCI Interface

The Embedded Processor Module communicates with the system board using a 32-bit PCI bus. The PCI bus conforms to the *PCI Local Bus Specification*, Revision 2.1. The module itself represents 1.5 electrical loads on the PCI bus.

The REQ[3:0]# signals are pulled up to 5 V by 2.7 KΩ resistors on the Embedded Processor Module. The following signals must be pulled to 5 V on the system board: PIRQ[A:D]#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, and SERR#. Pins REQ64# and ACK64# on the PCI connector must also be pulled to 5 V.

The GNT[3:0]# signals are pulled up to 3.3 V on the Embedded Processor Module by 2.7 KΩ resistors. The PHLDA# must be pulled up on the system board through a 2.7 KΩ resistor. These signals are outputs of the 82439HX system controller.

The 82439HX System Controller supports up to four PCI masters with its REQ[3:0]# and GNT[3:0]# signals.

For more information on the PCI interface design, see the *Intel 430HX PCIset Design Guide* (Order No. 297467).

2.4 Voltage Regulation

The Embedded Processor Module integrates a Linear Technology, Inc. LTC1435* voltage regulator on-board to provide the core voltage of the Pentium® Processor.

The input to the voltage regulator is the 5 V power plane on the Embedded Processor Module. Because the 5 V plane also supplies 5 V to the 82439HX system controller the tolerance on the power supply must be within ±5% (under a maximum current load). Refer to the applicable processor datasheet for maximum current requirements. The system board must supply a minimum voltage of 4.75 V.

Since the 3.3 V supply is not regulated on the Embedded Processor Module, the system board must provide a minimum of 3.135 V and a maximum of 3.6 V to meet the specifications for components integrated on the Embedded Processor Module.

The frequency of the switching regulator used on the Embedded Processor Module is approximately 165 KHz.

Bulk and high frequency decoupling capacitance is provided on the module; however, the system board should provide additional bulk and high frequency capacitance near the connectors of the Embedded Processor Module. The additional capacitors ensure that "clean" power is provided to the Embedded Processor Module. The amount of capacitance required on the system board depends on many factors, including power supply design, system board layout, and board impedance. Table 2 lists the minimum recommended configuration.

Table 2. Voltage Plane Capacitance Requirement

Voltage Plane	Location	Capacitance	Rating
V_5V	Connector	100 µF, 0.1 µF, 0.01 µF	35 V
V_3	Connector	100 µF, 0.1 µF	6 V

The Embedded Processor Module provides bulk decoupling for the processor, the 82439HX system controller, and the PBSRAMs. The bulk capacitance minimizes voltage drop when the power supply does not have time to react to a large current change in a relatively short period of time (50–300 ns). Table 3 lists the bulk capacitance for the processor on the Embedded Processor Module.

Table 3. Processor Bulk Decoupling Capacitance

2.9 V Core Decoupling	4 x 100 µF Low ESR/ESL Ceramic
3.3 V I/O Decoupling	1 x 33 µF Low ESR/ESL Ceramic

Additional bulk capacitance is implemented on the Embedded Processor Module for the System Controller and SRAM devices.

The Embedded Processor Module also provides high frequency decoupling capacitors to minimize the effects of high-frequency transient currents during device operation.

The Embedded Processor Module has a COREV_SENSE signal output to indicate that the core power supply is at the correct voltage. This signal should be used by the system designer to communicate the power good status to the overall system. The COREV_SENSE signal is detected by a comparison circuit, and the output is routed to the PWROK signal on the 82371SB (PIIX3). When this signal is received by the PIIX3, the system can be reset.

There is no overcurrent/overvoltage protection circuitry on the Embedded Processor Module, except for the input protection circuitry on the individual components. Never insert or remove the Embedded Processor Module while the power is on. Permanent damage to the module may result.

2.5 Embedded Processor Module Pullup/Pulldown Resistor Requirements

Table 4 lists the Embedded Processor Module signals that have pullup or pulldown resistors and the required resistor values:

Table 4. Signals with Pullups or Pulldowns

Signal	PU / PD	Resistor Values (Ω)	Voltage (V)
DP[7:0]	PU	4.7 K	3.3
STPCLK#	PU	8.2 K	3.3
AP	PU	8.2 K	3.3
WB/WT#	PU	8.2 K	3.3
FLUSH#	PU	1.0 K	3.3
PEN#	PU	4.7 K	3.3
R/S#	PU	8.2 K	3.3
REQ[3:0]#	PU	2.7 K	5.0
GNT[3:0]#	PU	2.7 K	3.3
EWBE#	PD	0	GND
HOLD	PD	0	GND
PHLD#	PU	10 K	5.0
PHLDA#	PU	10 K	3.3

2.6 System Board Pullup/Pulldown Resistor Requirements

The system designer must provide pullup resistors on the system board for the signals listed in Table 5.

Table 5. System Board Pullup/Pulldown Requirements

Signal	PU/PD	Resistor Value (Ω)	Strapping Voltage (V)
INTR	PU	4.7 K	3.3
FERR	PU	4.7 K	3.3
NMI	PU	4.7 K	3.3
SMI#	PU	4.7 K	3.3
IGNNE#	PU	4.7 K	3.3
CPURST	PU	3.3 K	3.3
PLOCK#	PU	2.7 K	5.0
DEVSEL#	PU	2.7 K	5.0
TRDY#	PU	2.7 K	5.0
IRDY#	PU	2.7 K	5.0
FRAME#	PU	2.7 K	5.0
SERR#	PU	2.7 K	5.0
STOP#	PU	2.7 K	5.0
PAR	PU	2.7 K	5.0
A20M#	PU	4.7 K	3.3
INIT	PU	330	3.3

3.0 Mechanical Considerations

3.1 Space Constraints

The Embedded Processor Module is designed to fit into a single CompactPCI* slot or into other space-constrained environments. The Embedded Processor Module integrates a thermal solution and provides adequate signal integrity at the connector interface.

The module does *not* provide a thermal solution that is adequate for *all* environmental conditions. The thermal characteristics of the Embedded Processor Module are currently being evaluated.

3.2 Reserved Areas

The area beneath the Embedded Processor Module module should be considered reserved, with the exception of 0805 footprint and smaller passive components. If the system board uses this area, the system designer must ensure that there is no interference between the Embedded Processor Module and the system board.

3.3 Module Mechanical Description

The following sections the physical characteristics of the Embedded Processor Module.

3.3.1 General Description

The Embedded Processor Module has components on both sides. Components on the bottom may extend to within 100 mils of the system board surface, except for the board-to-board connectors. The lead guard for the Tape Carrier Package (TCP) is not removable. Any attempt to remove it may result in damage to the TCP device. Components on the top side of the PCB (including the Heat sink) do not exceed 540 mils. Heights are relative to the PCB surface.

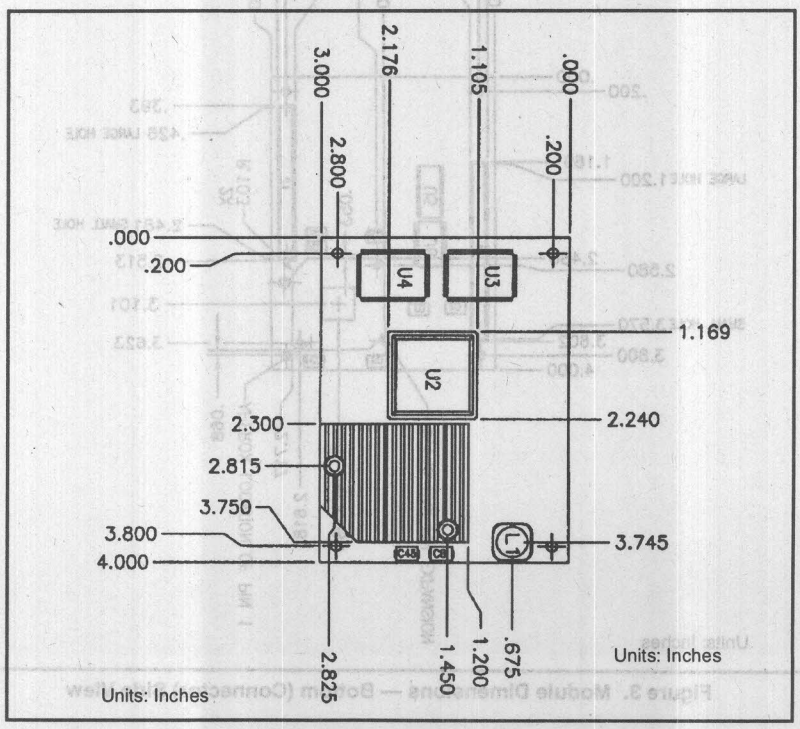


Figure 1. Module Dimensions — Top Side View

Figure 2. Module Dimensions — Side View

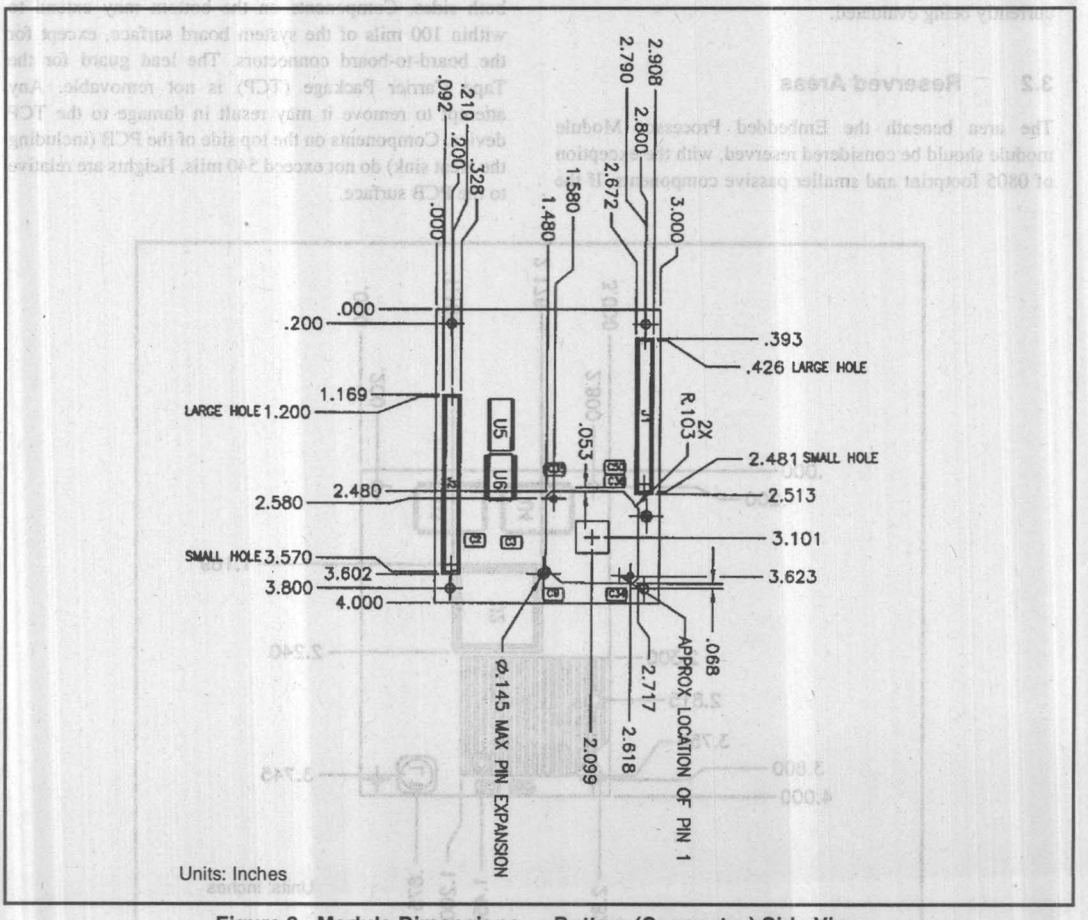


Figure 3. Module Dimensions — Bottom (Connector) Side View

3.3.2 Mounting Hole Locations and Size

There are four holes in the corners of the Embedded Processor Module for attachment to the system board. The diameter of the four mounting holes is 125 mils, nominal. The mounting holes accept a size 4 screw. Figure 4 shows the location of the holes from the edges of the PCB (all values are nominal).

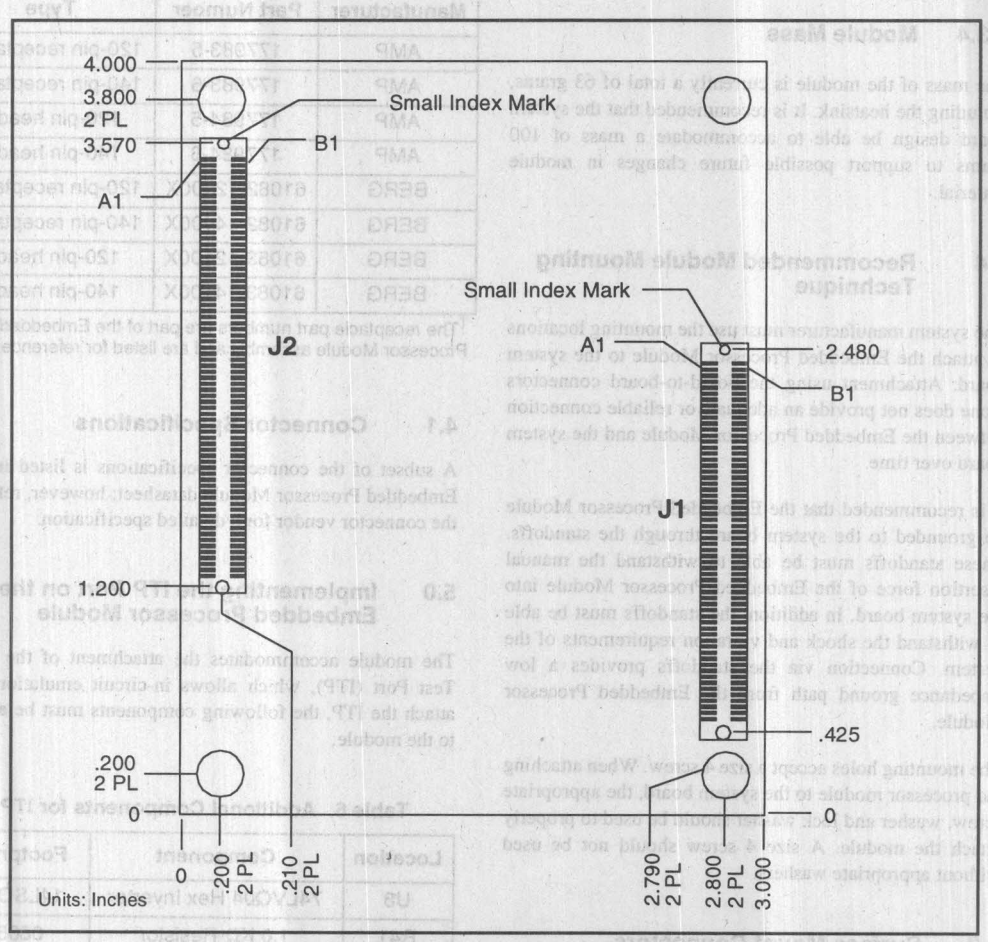


Figure 4. Mounting Hole Diagram

3.3.3 Ground Ring

The mounting holes are electrically tied to ground (GND) on the Embedded Processor Module. The ground ring around the mounting holes are 450 mils in diameter.

3.3.4 Module Mass

The mass of the module is currently a total of 63 grams, including the heatsink. It is recommended that the system board design be able to accommodate a mass of 100 grams to support possible future changes in module material.

3.4 Recommended Module Mounting Technique

The system manufacturer must use the mounting locations to attach the Embedded Processor Module to the system board. Attachment using the board-to-board connectors alone does not provide an adequate or reliable connection between the Embedded Processor Module and the system board over time.

It is recommended that the Embedded Processor Module be grounded to the system board through the standoffs. These standoffs must be able to withstand the manual insertion force of the Embedded Processor Module into the system board. In addition, the standoffs must be able to withstand the shock and vibration requirements of the system. Connection via the standoffs provides a low impedance ground path from the Embedded Processor Module.

The mounting holes accept a size 4 screw. When attaching the processor module to the system board, the appropriate screw, washer and lock washer should be used to properly attach the module. A size 4 screw should not be used without appropriate washers.

4.0 Surface Mount Connectors

The Embedded Processor Module connects to the system board via two low profile, high density connectors. The two connectors are segregated into functional categories: the PCI Bus interface and the DRAM interface. Refer to the *Intel Embedded Processor Module* datasheet for detailed information on the module pinout and signal descriptions. The connectors are available from multiple vendors with identical designs. The part numbers for two of the vendors are listed below. Mating pairs can be mixed between vendors.

Figure 5. Connector Part Numbers

Manufacturer	Part Number	Type
AMP	177983-5	120-pin receptacle†
AMP	177983-6	140-pin receptacle†
AMP	177984-5	120-pin header
AMP	177984-6	140-pin header
BERG	61082-12100X	120-pin receptacle†
BERG	61082-14100X	140-pin receptacle†
BERG	61083-12100X	120-pin header
BERG	61083-14100X	140-pin header

†The receptacle part numbers are part of the Embedded Processor Module assembly and are listed for reference only.

4.1 Connector Specifications

A subset of the connector specifications is listed in the Embedded Processor Module datasheet; however, refer to the connector vendor for a detailed specification.

5.0 Implementing the ITP Port on the Embedded Processor Module

The module accommodates the attachment of the Intel Test Port (ITP), which allows in-circuit emulation. To attach the ITP, the following components must be added to the module:

Table 6. Additional Components for ITP

Location	Component	Footprint
U8	74LVQ04 Hex Inverter	14LSOIC
R41	1.0 KΩ Resistor	0805
R42	0Ω Resistor	0805

See Figure 6 for the location of the test port. Figure 7 shows the location of the additional components required for the ITP to function.

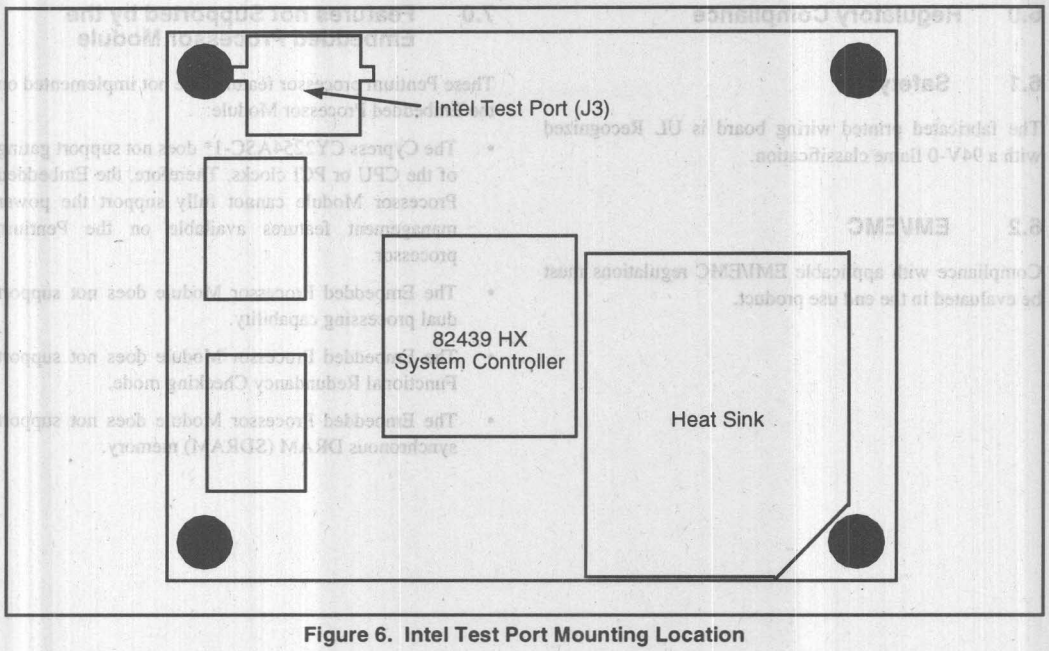


Figure 6. Intel Test Port Mounting Location

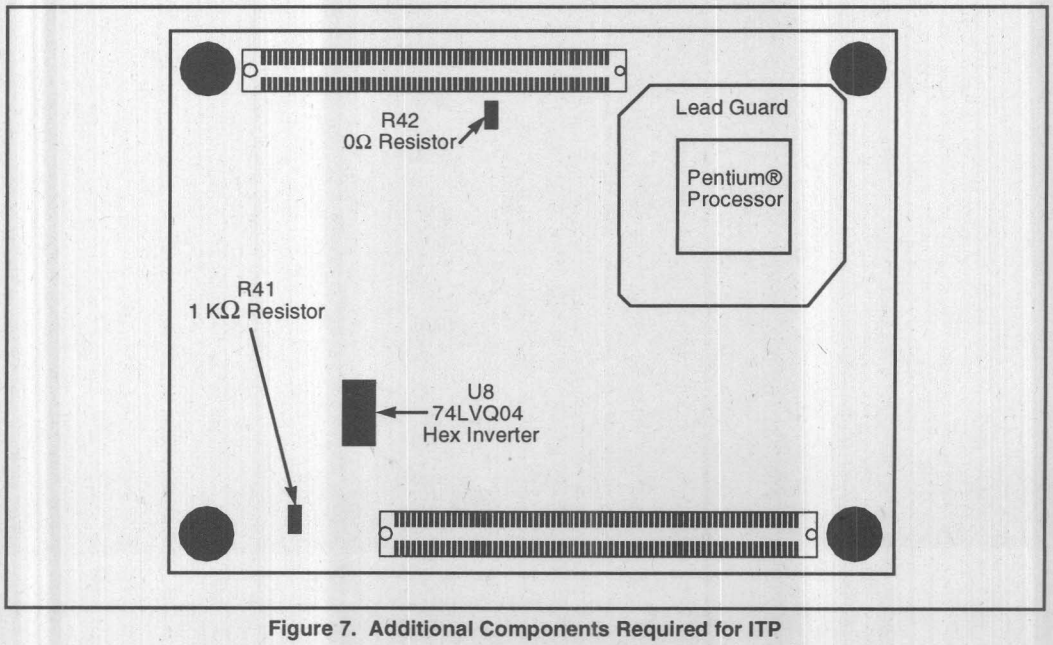
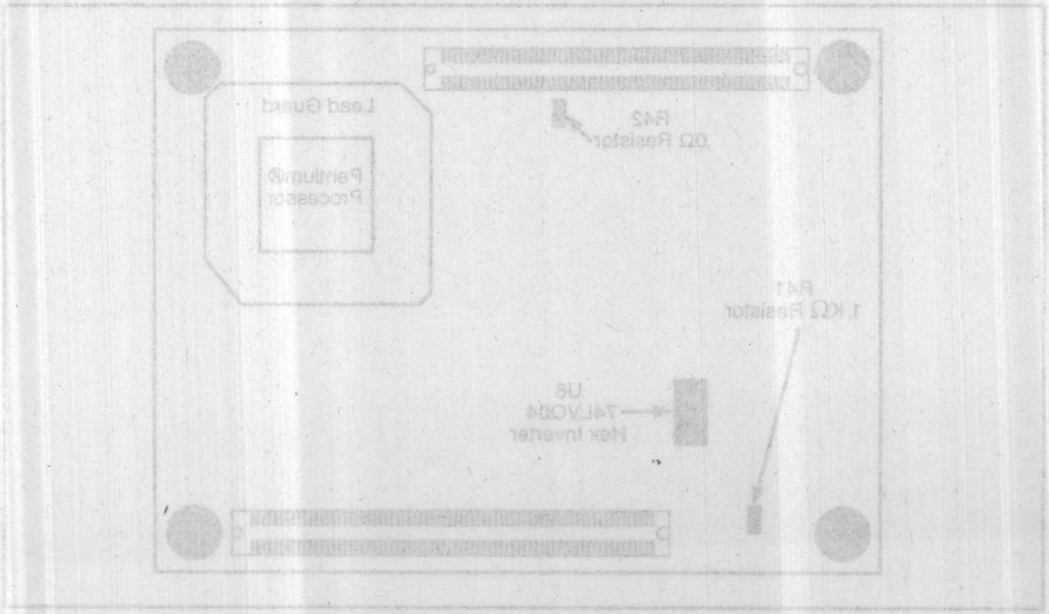


Figure 7. Additional Components Required for ITP

dual processing capability.

- The Embedded Processor Module does not support Functional Redundancy Checking mode.
- The Embedded Processor Module does not support synchronous DRAM (SDRAM) memory.



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AP-759

APPLICATION NOTE

Intel Embedded Processor Module (EMBMOD133) Thermal Design Guide

December, 1997

Order Number: 273143-001

intel

AP-759

APPLICATION
NOTE

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1.0 INTRODUCTION

The Embedded Processor Module is a high-performance subsystem for use in embedded, industrial and communication applications. Thermal management is important in these applications to achieve the necessary system performance.

This application note:

- Introduces the concepts and calculations used when designing a thermal solution
- Provides thermal performance data for the Intel Embedded Processor Module (EMBMOD133)
- Recommends methods for meeting the thermal requirements imposed on systems

Examples are also provided. Note that the thermal design information for the Intel Embedded Processor Module (EMBMOD166) which uses a 166 MHz processor is not covered in this application note.

2.0 IMPORTANCE OF THERMAL MANAGEMENT

The objective of thermal management is to ensure that the temperature of all components is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance and cause reliability issues.

The case temperature is the surface temperature of the package at its hottest point. Temperatures exceeding the case temperature limit can cause physical destruction or may result in irreversible changes in operating characteristics.

3.0 COMPONENT POWER AND CASE TEMPERATURE SPECIFICATIONS

The power dissipation and case temperature specifications are shown in Table 1 for the 133 MHz Pentium Processor in the Tape Carrier Package (TCP) and the Intel 82439HX System Controller (TXC) in a Ball Grid Array (BGA) package. The designer should collect similar data from the specific vendor for the 32Kx32 PBSRAM, Voltage Regulator, Clock Driver, 14.318 MHz Crystal, and 32Kx8 SRAM.

Table 1. Power Dissipation and Case Temperature Specifications for the Pentium® Processor and the Intel 82439HX System Controller (TXC)

IC Component	Package Type	Total Pins	Package Size (Max)	Typical Power (W)	Max Power (W)	Max Case Temp (°C)
Pentium® Processor (133 MHz)	TCP	320	24 mm x 24 mm	3.5	7.9	95
82439HX System Controller (TXC)	BGA	324	27.2 mm x 27.2 mm	1.0	1.2	85

NOTE: For more information, refer to the *Pentium® Processor with Voltage Reduction Technology* datasheet (order number 252557).

4.1 Ambient Temperature

Ambient temperature (T_A) is the temperature of the undistributed air surrounding the package. Ambient temperature is usually measured at a specified distance from the module. In a system environment, ambient temperature is the temperature of the air upstream to the module and in its close vicinity. In a typical laboratory test environment, ambient temperature is measured 12 inches (or as close to 12 inches as possible) upstream from the module to represent the ambient temperature with air flowing past the system. When natural convection is used in a system, the ambient temperature is measured directly underneath the board module.

4.3 Measuring Case Temperature

To verify that the proper T_C is maintained for the Pentium processor, it should be measured at the center of the top surface of the package. To minimize any measurement errors, the following techniques and materials are recommended:

- Use 36 AWG or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was performed using a thermocouple offered by Omega Engineering, Inc. (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center and top surface of the package using a cement or glue that is highly thermally conductive. Intel's laboratory testing was performed using Omega Bond* (Part number: OB-101).
- Attach the thermocouple at a 0° angle on the center of the top surface of the package as shown in Figure 1.

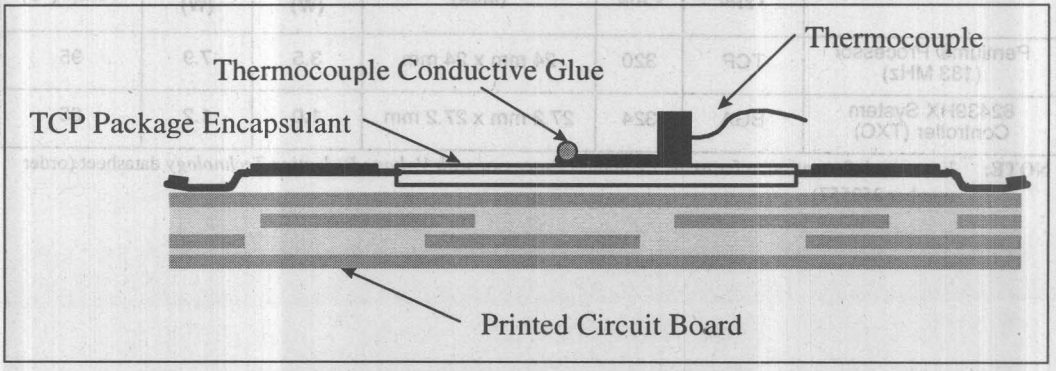


Figure 1. Thermocouple Attachment for Measuring the Case Temperature

4.4 Calculating Case-to-Ambient Thermal Resistance

For the Pentium processor with voltage reduction technology, an ambient temperature is not specified directly. The only requirement is that the case temperature is met. The thermal resistance can be calculated from the following equation:

$$\theta_{CA} = (T_C - T_A)/P \qquad (1)$$

where:

θ_{CA} = Case-to-Ambient thermal resistance (°C/W)

T_A = ambient temperature (°C)

T_C = case temperature (°C)

P = device power dissipation (Watts)

For example, assuming the case temperature is 95 °C, the ambient temperature is 50 °C, and the typical power dissipated by the Pentium processor is 3.5 W, the case-to-ambient thermal resistance (θ_{CA}) is 12.9 °C/W. Knowing the θ_{CA} value allows the system designer to determine the estimated airflow required to keep the TCP case temperature at 95 °C and helps the designer determine the best way to orient the board to obtain the minimum airflow requirement.

5.0 TCP PACKAGE THERMAL CHARACTERISTICS

The primary heat transfer path from the die of the TCP is through the back side of the die and into the printed circuit (PC) board. There are two thermal paths traveling from the PC board to the ambient air. One is the spread of heat within the board and the dissipation of heat by the board to the ambient air. The other is the transfer of heat through the board to the opposite side where thermal enhancements (heat sinks, fans, pipes, etc.) are attached.

6.0 PC BOARD THERMAL ENHANCEMENTS

Copper planes, thermal pads, and vias are design options that can improve heat transfer from the PC board to the ambient air. It should be noted that although thicker copper planes reduce the θ_{CA} of a system without any thermal enhancements, thicker planes have less effect on the θ_{CA} of a system with thermal enhancements. Placing vias under the die reduces the θ_{CA} of a system with and without thermal enhancements.

6.1 Thermal Test Board Configuration

The thermal measurements for the EMBMOD133 were taken with a Pentium processor in the TCP package soldered to a 4" x 3" test board outline. This six-layer board contains 10.0 mil drill holes on 50 mil pitch vias (underneath the die) in the die attach pad which are connected to a 1 oz. copper plane. The vias in the die attach pad are connected without thermal paths to the ground plane(s). The die is attached to the die attach pad using a thermally and electrically conductive adhesive as shown in Figure 2. A 13 X 13 array of thermal vias conducts the heat generated by the Pentium processor to the top side of the board where a heat sink is attached to assist in heat dissipation.

The test board was designed to optimize the heat spreading into the board and the heat transfer through to the opposite side of the board. Thermal die was used to represent each of the components with a power of 1W or greater. The test board included thermal die for the Pentium processor in a TCP package, Intel 82439HX System Controller (TXC) in a BGA package, and the 32Kx32 PBSRAM in a TQFP package.

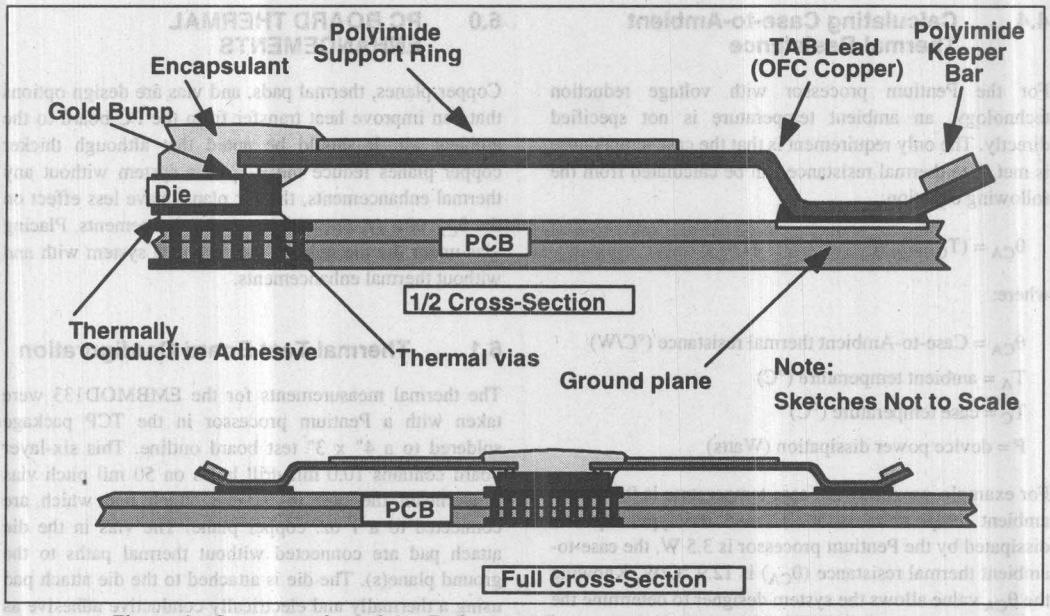


Figure 2. Cross-section of the Embedded Processor Module with TCP (Mounted)

7.0 DESIGNING FOR THERMAL PERFORMANCE

This section describes how to apply the thermal characteristics to a system thermal design. The goal of a thermal solution is to maintain the case temperatures of all the IC components on the board module. The main factors which determine the type of thermal solution to use are:

- Performance target
- Cost
- Amount and direction of airflow
- Available pressure drop
- Heat sink geometry
- Heat sink attachment to board

Three thermal solutions are available for the module which satisfy many broad-market requirements. At the time of this printing, Intel offers the Embedded Processor Module only with an extruded heat sink.

The three available solutions are a passive heat sink, active fan heat sink, and a liquid-cooled heat pipe and cooling device combination. A passive heat sink system is the simplest and most cost effective solution when the design can include ample airflow. The active fan heat sink solution should be used in designs without forced airflow that are operating at a typical ambient temperature of 50 °C. For designs operating at high ambient temperatures and restricted to only natural convection, a heat pipe with a cooling device may be the only solution.

The CompactPCI specification was used to determine the overall form factor of the Embedded Processor Module and the height allowed for the thermal solution. For a copy of the CompactPCI specification, contact Rogers Communication at the address listed in Appendix A.

7.1 Extruded Heat Sink Solution

The Intel Embedded Processor Module uses an extruded, unidirectional heat sink which meets the CompactPCI form-factor requirement with a height of 0.275 inches (6.98 mm), and can dissipate the Pentium processor's maximum power of 7.9 W. This cooling solution was demonstrated to meet the 95 °C case temperature and a 50 °C ambient temperature with a fixed airflow of 400 - 500 LFM with a typical processor power of 3.5 W when the airflow is directed first onto the TCP package without any preheating from other components (refer to the thermal characterization data in section 7.8). The amount of airflow required can change depending on where the system fan is located. The module's orientation in the system (Figure 3) determines how much airflow is needed.

All of the conditions for a particular application must be taken into consideration to determine if this particular heat sink is sufficient or if a new heat sink design is required. This design was targeted to meet the CompactPCI component height requirements as shown in Figure 4. If there is no need to meet this height requirement, a taller heat sink can be designed with a potential cost savings. The heat sink is shown in Figure 5 and the push pin is shown in Figure 6.

Although the extruded heat sink is the simplest solution, the design optimization is not trivial. The designer must consider the following parameters when designing a high-performance, low-cost heat sink or fan heat sink:

- Surrounding ICs
- Maximum power of all components
- Ambient and case temperatures
- Board/module orientation
- Direction of airflow
- Heat source area
- Top/bottom heat dissipation of component
- Manufacturability
- Tooling for testing and manufacturing
- Fin profile (round, oval, or square)
- Unidirectional vs. omnidirectional fins
- Fin geometry (height, thickness, and distance between fins)
- Base plate geometry (thickness and area)
- Material (aluminum, copper, and alloy)
- Heat sink attachment mechanism
- Heat sink attachment material (grease, dry-film, thermal tape)
- Heat sink attachment thickness and coverage area
- Heat sink surface treatment (e.g., anodizing)
- Safety/caution labels
- UL recognition (or equivalent)
- Available pressure drop

Appendix A lists heat sink vendors, vendors of heat sink attach/interface materials, the current PCB manufacturer, and the address for requests for copies of the CompactPCI Specification.

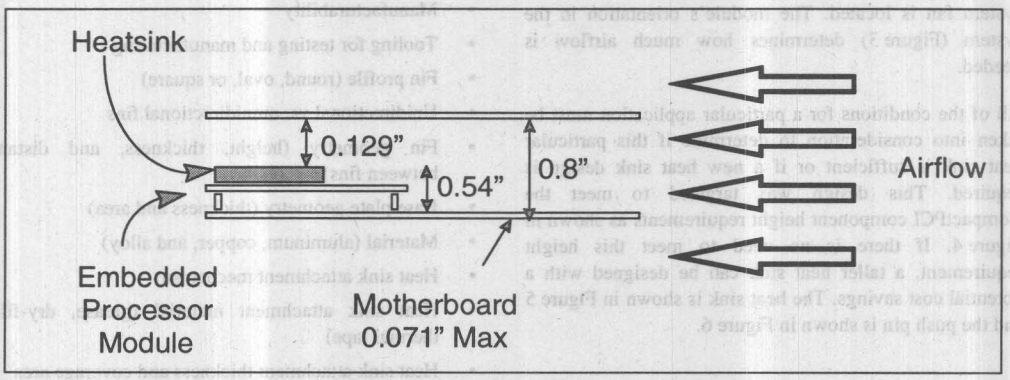


Figure 4. CompactPCI Configuration Requirements

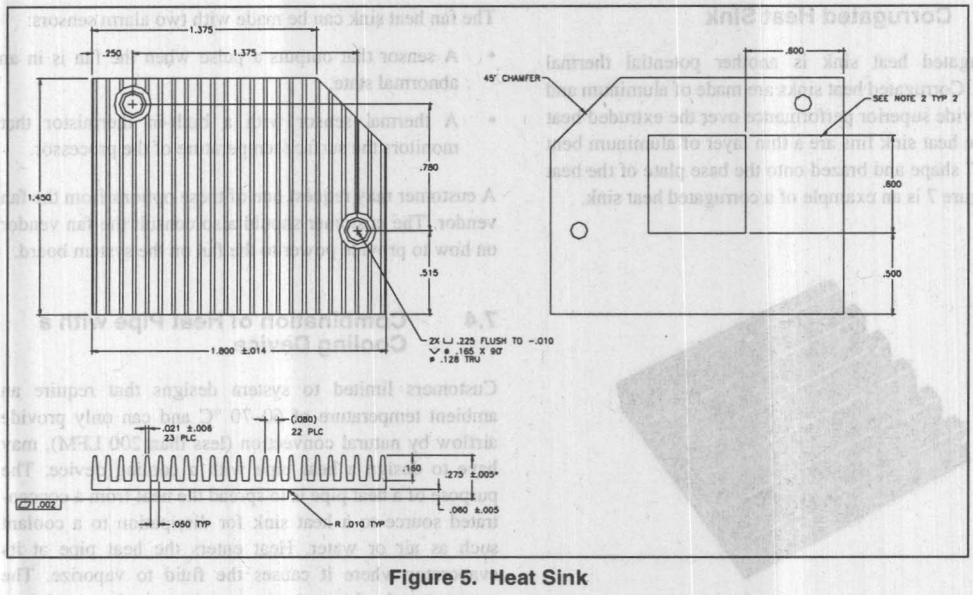


Figure 5. Heat Sink

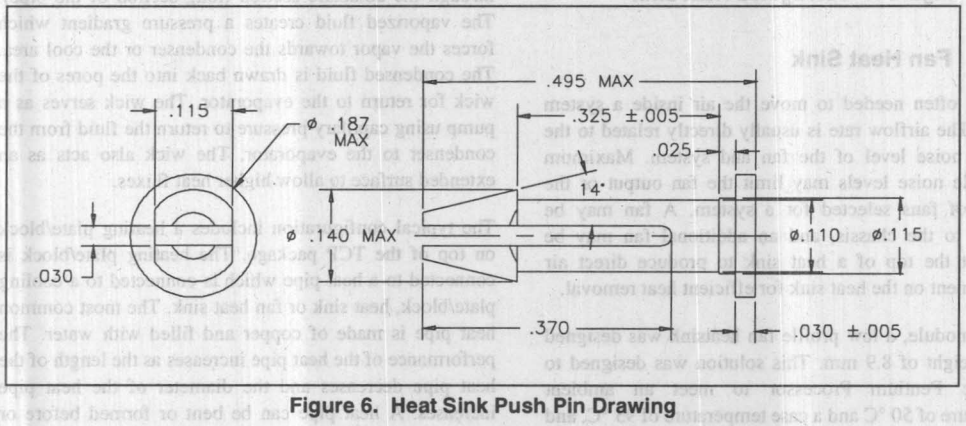


Figure 6. Heat Sink Push Pin Drawing

7.2 Corrugated Heat Sink

A corrugated heat sink is another potential thermal solution. Corrugated heat sinks are made of aluminum and may provide superior performance over the extruded heat sink. The heat sink fins are a thin layer of aluminum bent in an "S" shape and brazed onto the base plate of the heat sink. Figure 7 is an example of a corrugated heat sink.

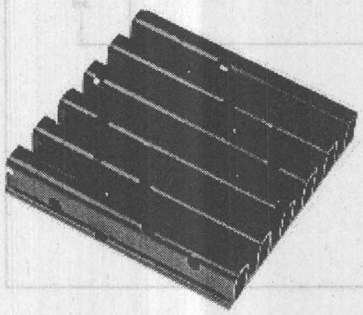


Figure 7. Corrugated Heat Sink

7.3 Fan Heat Sink

Fans are often needed to move the air inside a system chassis. The airflow rate is usually directly related to the acoustic noise level of the fan and system. Maximum acceptable noise levels may limit the fan output or the number of fans selected for a system. A fan may be attached to the chassis, and an additional fan may be placed at the top of a heat sink to produce direct air impingement on the heat sink for efficient heat removal.

For the module, a low profile fan heatsink was designed with a height of 8.9 mm. This solution was designed to cool the Pentium Processor to meet an ambient temperature of 50 °C and a case temperature of 95 °C, and to dissipate a maximum power of 7.9 W with no other airflow required by the system. The thermal characterization data for this design is provided in Section 7.8.

The height of this fan heatsink solution exceeds the CompactPCI height requirement of 7 mm or less. A fan heatsink design which will meet the CompactPCI specification is currently under evaluation. The module is not offered with a fan heatsink, but the fan heatsink design is available for customers.

The fan heat sink can be made with two alarm sensors:

- A sensor that outputs a pulse when the fan is in an abnormal state.
- A thermal sensor with a built-in thermistor that monitors the surface temperature of the processor.

A customer may request one of these options from the fan vendor. The customer should also consult the fan vendor on how to provide power to the fan on the system board.

7.4 Combination of Heat Pipe with a Cooling Device

Customers limited to system designs that require an ambient temperature of 60–70 °C and can only provide airflow by natural convection (less than 200 LFM), may have to design a heat pipe with a cooling device. The purpose of a heat pipe is to spread the heat from a concentrated source to a heat sink for dissipation to a coolant such as air or water. Heat enters the heat pipe at its evaporator where it causes the fluid to vaporize. The vapor travels from the evaporator to the condenser through the adiabatic section (long section of the pipe). The vaporized fluid creates a pressure gradient which forces the vapor towards the condenser or the cool area. The condensed fluid is drawn back into the pores of the wick for return to the evaporator. The wick serves as a pump using capillary pressure to return the fluid from the condenser to the evaporator. The wick also acts as an extended surface to allow higher heat fluxes.

The typical configuration includes a heating plate/block on top of the TCP package. The heating plate/block is connected to a heat pipe which is connected to a cooling plate/block, heat sink or fan heat sink. The most common heat pipe is made of copper and filled with water. The performance of the heat pipe increases as the length of the heat pipe decreases and the diameter of the heat pipe increases. A heat pipe can be bent or formed before or after fabrication to meet the system space requirements. Each bend lowers the performance of the heat pipe. Heat pipes can have a long life of 100,000 hours or more, depending on the design. Contact the vendor for reliability data.

The heat pipe thermal resistance is the sum of the conduction through the wall of the pipe, conduction through the wick, evaporation temperature difference, vapor pressure drop, condensation temperature difference (ΔT), conduction through the wick, and conduction

through the heat pipe wall on the opposite side of the pipe. The predominant thermal resistances are the evaporation (ΔT) and the vapor pressure drop.

A heat pipe solution is a unique, customer specific solution. The customer must provide the system environment, application and thermal requirements to the heat pipe vendors in order to generate an optimal design. Refer to Appendix A for a list of heat pipe vendors.

7.5 Thermally Conductive Interface Materials Information

The current heat sink attach material is a thermally and electrically conductive grease. Thermal grease is widely used as the interface material. Thermal grease typically provides the lowest thermal resistance of the available alternatives.

On the Embedded Processor Module, the thermal grease provides an effective interface between the heat sink and the processor package. Other thermally conductive materials such as film, tape, adhesives or gap fillers may be used to enhance the thermal characteristics of components which do not have a heat sink solution, such as the 82439HX System Controller, SRAMs, and the side of the Pentium processor package opposite the heat sink.

Several interface materials are currently being evaluated to determine which materials keep the components cooler. Refer to Appendix A for interface material vendors.

7.6 Heat Sink Removal and Attachment

It is not recommended to remove the heat sink once placed on the board. If you must remove the heat sink, be careful not to damage the module or components. Any damage to the board or the components voids the warranty of the module.

Follow this procedure when removing the heat sink:

CAUTION: Allow the heat sink to cool to room temperature before removing the heat sink from the module.

- Wear an ESD strap at all times when handling the modules to protect against electrostatic discharge.
- Use needle-nose pliers to gently squeeze the nose of each push pin (shown in Figure 8) together so that there is no gap and push the pins out of the board.

Follow this procedure to attach the heat sink:

- Add approximately 1/8 gram of thermally conductive grease evenly onto the pedestal of the heat sink.
- Align the heat sink holes to the plated holes on the module.
- Press push pins through the holes with approximately 6 lb. force until the nose of the pin latches onto the module.

If you require assistance or rework of the heat sink, contact the current board manufacturer listed in Appendix A.

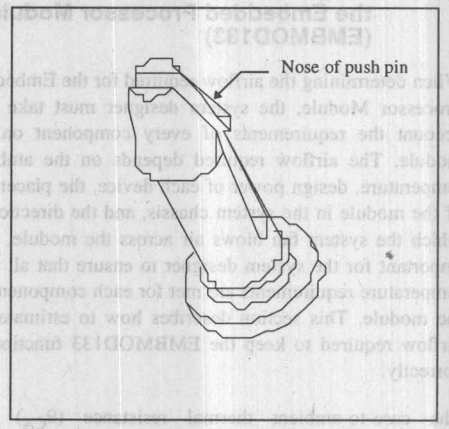


Figure 8. Heat Sink Push Pin

7.7 Heat Sink Handling Safety Precaution

The heat sink temperature should not rise above 95 °C at worst case power conditions. Intel requires a safety label or stamp to be placed on the heat sink as a warning to indicate that this part is hot. The safety label uses the caution/attention symbols (ISO 7000, # 0434 and IEC 417, # 5041) to provide this warning as shown in Figure 9.

CAUTION: Allow the heat sink to cool to room temperature before removing the heat sink from the module.

7.8 Thermal Characterization Data for the Embedded Processor Module (EMBMOD133)

When determining the airflow required for the Embedded Processor Module, the system designer must take into account the requirements of every component on the module. The airflow required depends on the ambient temperature, design power of each device, the placement of the module in the system chassis, and the direction in which the system fan blows air across the module. It is important for the system designer to ensure that all case temperature requirements are met for each component on the module. This section describes how to estimate the airflow required to keep the EMBMOD133 functioning correctly.

The case-to-ambient thermal resistance (θ_{CA}) was collected for these module components:

- Pentium processor in a TCP Package
- Intel 82439HX System Controller (TXC) in a BGA package
- 32Kx32 PB SRAM in a TQFP package

The other components were not considered in the characterization because of their low operating power conditions. The θ_{CA} values were gathered for the extruded heat sink, corrugated heat sink, and fan heat sink. All measurements were taken in an "open air" wind tunnel environment in which there was no enclosure around the module.

(EMBMOD133).

Two curves are shown in each figure:

0° rotation: This curve represents the thermal resistance vs. airflow when the module is in the 0° rotation. In the 0° rotation the airflow passes across the SRAMs, the 82439HX System Controller, and the Pentium processor in that order.

180° rotation: This curve represents the thermal resistance vs. airflow when the module is in the 180° rotation. In the 180° rotation the airflow passes across the Pentium processor, the 82439HX System Controller, and the SRAMs in that order.

Refer to Figure 3 for the airflow direction definitions.

The thermal characterization results show that the Pentium processor (TCP) thermal requirements determine the airflow required with the module in the 0° rotation. The TCP case temperature of 95 °C and the operating power range of the Pentium processor should be used to determine the thermal resistance and airflow in the 0° rotation.

The 82439HX System Controller thermal requirements determined the airflow required with the module in the 180° rotation of the board. The BGA case temperature of 85 °C and operating power range of the 82439HX System Controller should be used to determine the thermal resistance and airflow requirement in the 180° rotation.

The system designer can determine the approximate airflow required by calculating the θ_{CA} (refer to Section 4.4 on page 3) and charting this value onto the graphs in Figure 10 and Figure 11. For example, to determine the airflow required for maximum power consumption when the extruded heat sink exists on the module:

T_C (TCP) = 95 °C; T_C (BGA) = 85 °C

T_A = 50 °C T_A = 50 °C

P (TCP) = 7.9 W; P (BGA) = 1.2 W

θ_{CA} (TCP, 0° Rotation) = 5.7 °C/W

θ_{CA} (BGA, 180° Rotation) = 29.1 °C/W

Use equation (1) on page 3 to calculate θ_{CA} and then use the graphs of Figure 10 and Figure 11 to find the corresponding airflow required. Both graphs indicate that 550 LFM airflow is needed to meet maximum power conditions for both board rotations (0° and 180° rotation).

For typical power consumption when the extruded heat sink exists on the module:

T_C (TCP) = 95 °C; T_C (BGA) = 85 °C

T_A = 50 °C T_A = 50 °C

P (TCP) = 3.5 W; P (BGA) = 1.0 W

θ_{CA} (TCP, 0° Rotation) = 12.9 °C/W

θ_{CA} (BGA, 180° Rotation) = 35.0 °C/W

The graphs indicate that an airflow of 325 LFM is required in the 180° rotation of the module and less than 100 LFM in the 0° rotation for typical power conditions.

Figures 12, 13 and 14 and Tables 3, 4 and 5 represent the extruded heat sink characterization data. Figures 15 and 16 and Tables 6 and 7 represent the corrugated heat sink characterization data. Figures 17, 18 and 19 and Tables 8, 9 and 10 represent the fan heat sink characterization data.

Table 2. Intel Embedded Processor Module Thermal Resistance for various Airflows

Airflow (LFM)	0° Rotation θ_{CA} (°C/W)	180° Rotation θ_{CA} (°C/W)
800	4.8	25.4
600	5.4	28.2
400	6.7	33.2
200	10.0	40.5

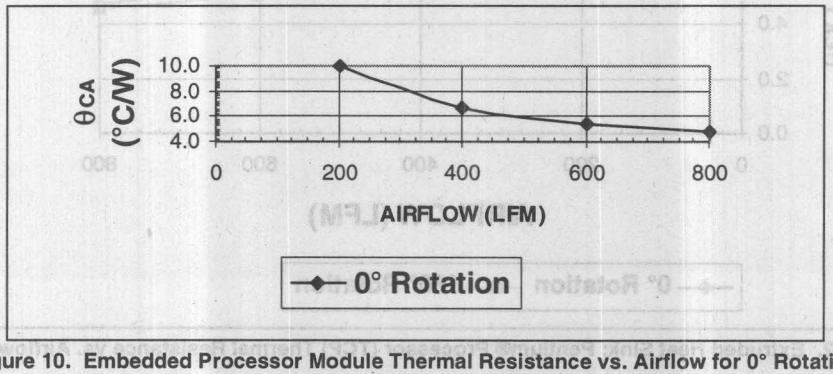


Figure 10. Embedded Processor Module Thermal Resistance vs. Airflow for 0° Rotation

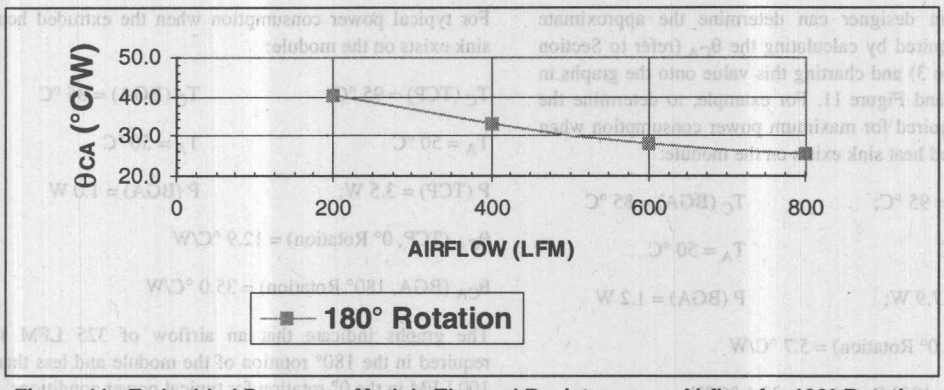


Figure 11. Embedded Processor Module Thermal Resistance vs. Airflow for 180° Rotation

Table 3. Extruded Heat Sink: Pentium® Processor (TCP) Thermal Resistance vs. Airflow

Airflow (LFM)	0° Rotation θ_{CA} (°C/W)	180° Rotation θ_{CA} (°C/W)
800	4.8	4.6
600	5.4	5.1
400	6.7	5.9
200	10.0	7.4

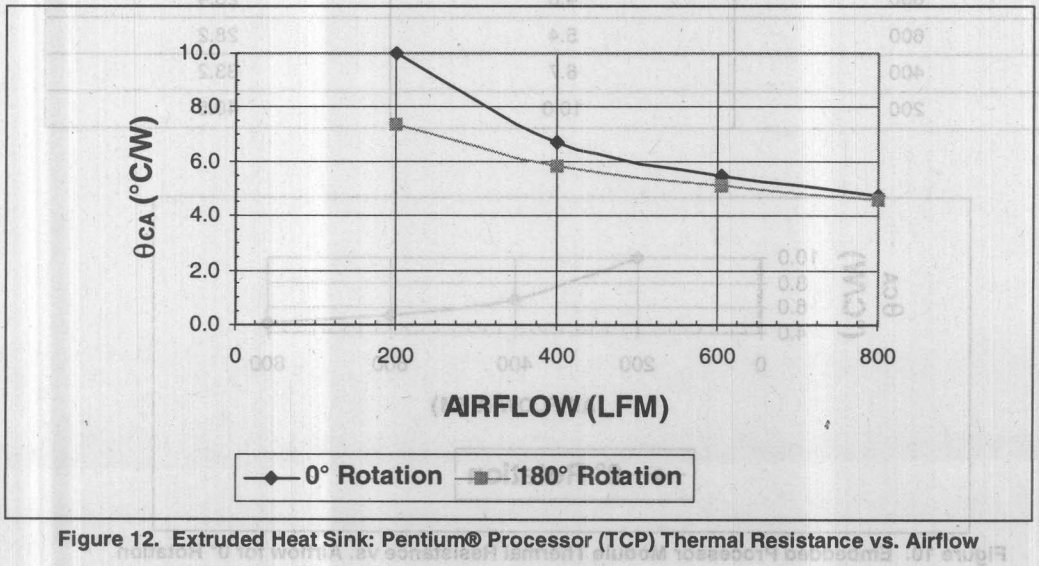


Figure 12. Extruded Heat Sink: Pentium® Processor (TCP) Thermal Resistance vs. Airflow

Table 4. Extruded Heat Sink: 82439HX System Controller (BGA) Thermal Resistance vs. Airflow

Airflow (LFM)	0° Rotation θ_{CA} (°C/W)	180° Rotation θ_{CA} (°C/W)
800	21.9	25.4
600	25.1	28.2
400	29.7	33.2
200	39.8	40.5

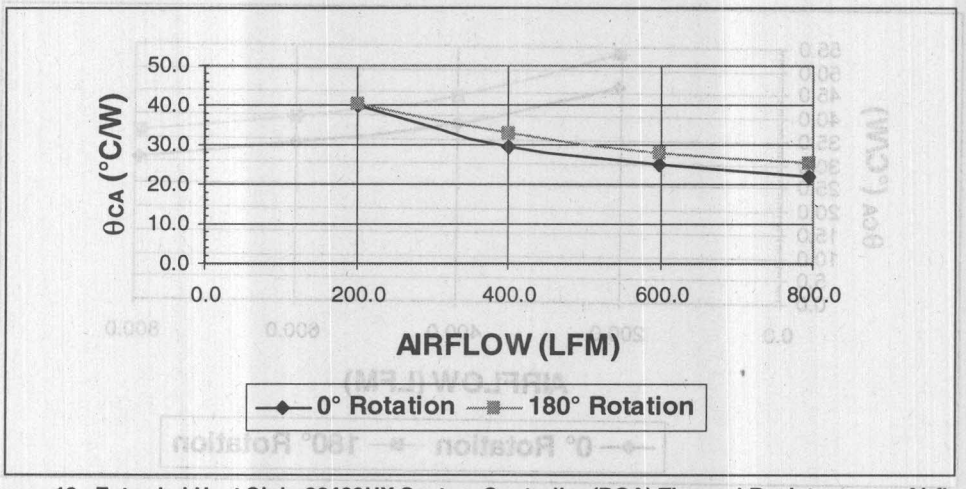


Figure 13. Extruded Heat Sink: 82439HX System Controller (BGA) Thermal Resistance vs. Airflow

Table 5. Extruded Heat Sink: SRAM (TQFP) Thermal Resistance vs. Airflow

Airflow (LFM)	0° Rotation θ_{CA} (°C/W)	180° Rotation θ_{CA} (°C/W)
800	30.6	36.8
600	34.0	39.6
400	38.4	44.4
200	46.4	53.8

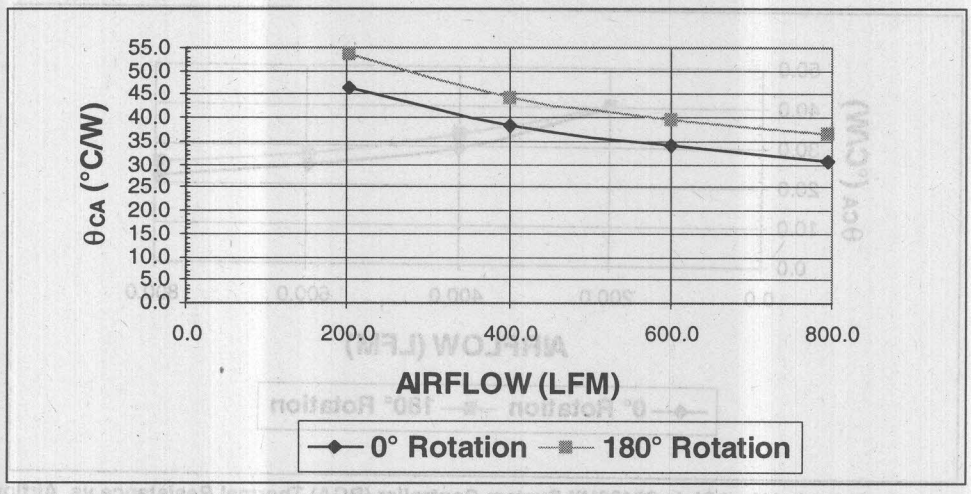


Figure 14. Extruded Heat Sink: SRAM (TQFP) Thermal Resistance vs. Airflow

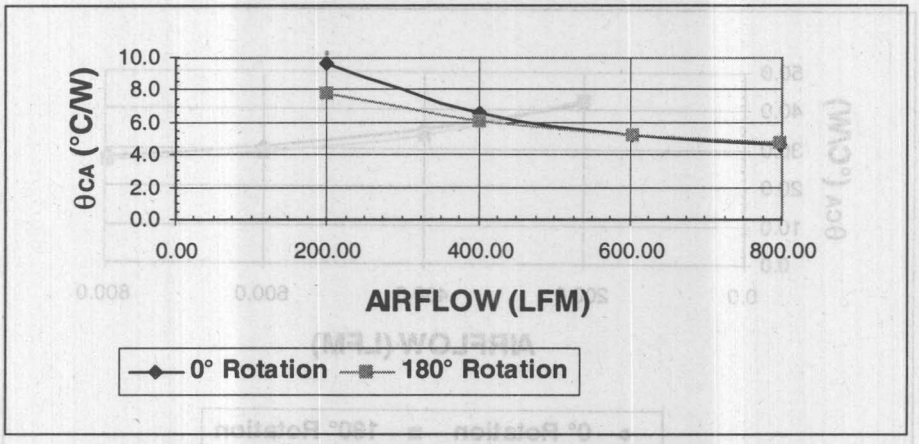


Figure 15. Corrugated Heat Sink: Pentium® Processor (TCP) Thermal Resistance vs. Airflow

Table 7. Corrugated Heat Sink: 82439HX System Controller (BGA) Thermal Resistance vs. Airflow

Airflow (LFM)	0° Rotation θ_{CA} (°C/W)	180° Rotation θ_{CA} (°C/W)
800	27.8	26.7
600	30.5	28.8
400	34.9	33.6
200	41.7	42.7

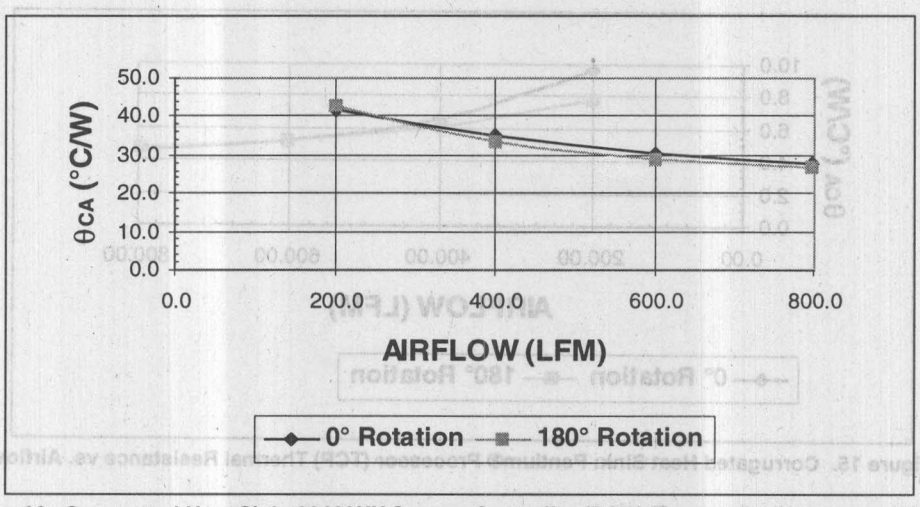


Figure 16. Corrugated Heat Sink: 82439HX System Controller (BGA) Thermal Resistance vs. Airflow

Table 8. Fan Heat Sink: Pentium® Processor (TCP) Thermal Resistance vs. Airflow

Airflow (LFM)	θ_{CA} (°C/W)
800	5.0
600	5.2
400	5.4
200	5.7
100	5.8

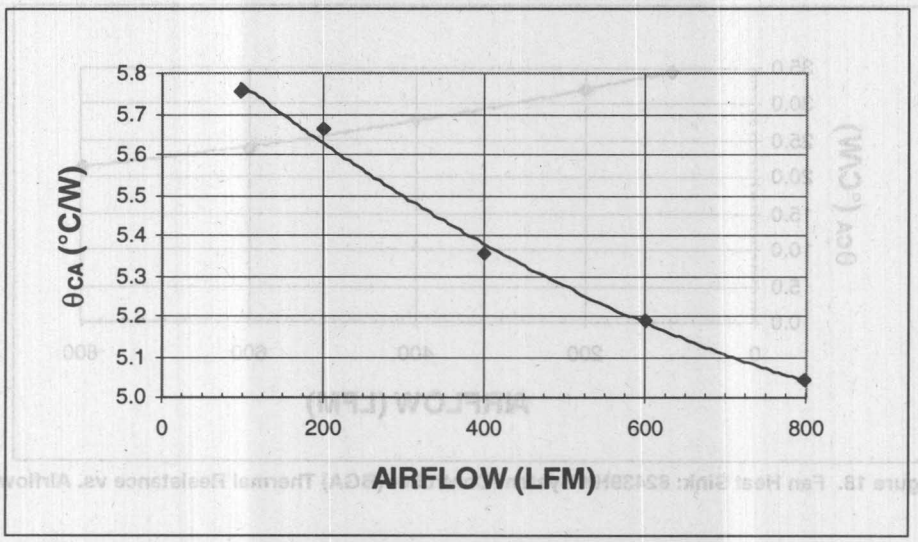


Figure 17. Fan Heat Sink: Pentium® Processor (TCP) Thermal Resistance vs. Airflow

Table 9. Fan Heat Sink: 82439HX System Controller (BGA) Thermal Resistance vs. Airflow

Airflow (LFM)	θ_{CA} (°C/W)
800	21.5
600	23.9
400	28.0
200	32.1
100	34.5

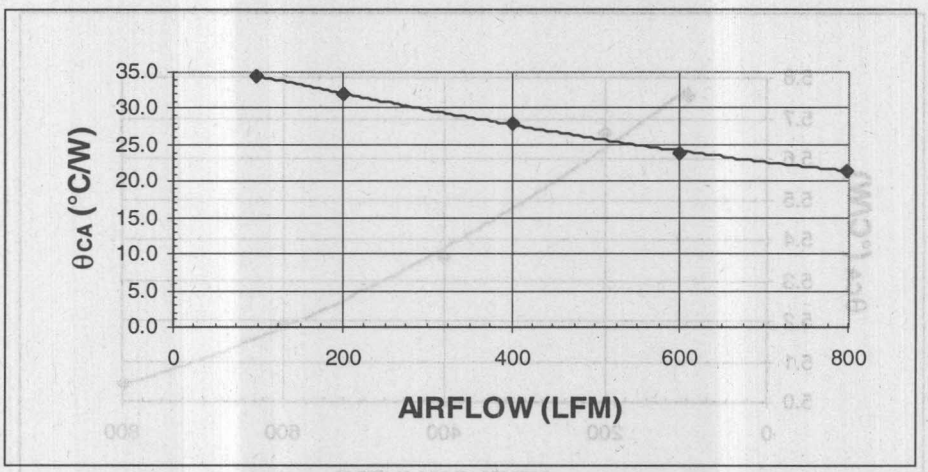


Figure 18. Fan Heat Sink: 82439HX System Controller (BGA) Thermal Resistance vs. Airflow

Table 10. Fan Heat Sink: SRAM (TQFP) Thermal Resistance vs. Airflow

Airflow (LFM)	θ_{CA} (°C/W)
800	30.9
600	33.6
400	37.9
200	42.9
100	45.9

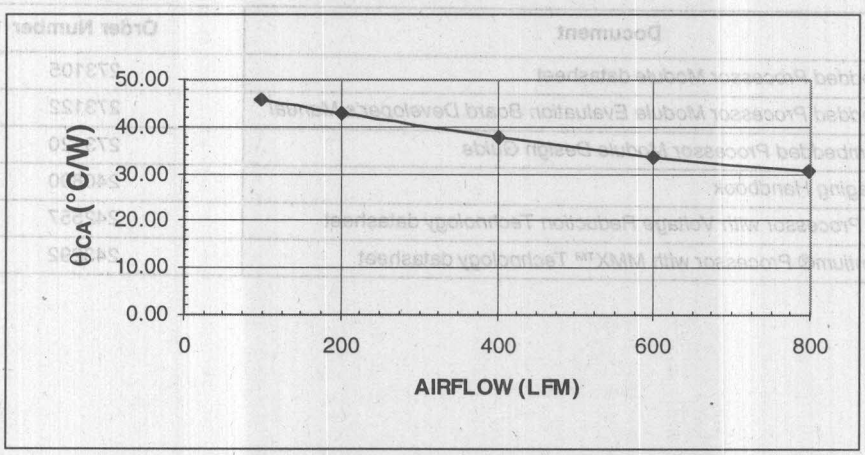


Figure 19. Fan Heat Sink: SRAM (TQFP) Thermal Resistance vs. Airflow

Table 11. Related Documents

Document	Order Number
Intel Embedded Processor Module datasheet	273105
Intel Embedded Processor Module Evaluation Board Developer's Manual	273122
AP-757, *Embedded Processor Module Design Guide*	273120
Intel Packaging Handbook	240800
Pentium® Processor with Voltage Reduction Technology datasheet	242557
Mobile Pentium® Processor with MMX™ Technology datasheet	243292

APPENDIX A

A.1 HEAT SINK VENDORS

Aavid Thermal Technologies, Inc.
One Kool Path
PO Box 400
Laconia, NH 03247
Phone: 603-528-3400
Fax: 603-525-1478

SMI Electronic Devices America, Inc.
4645 S. Lakeshore Drive
Suite # 11
Tempe, Arizona 85282
Phone: 602-820-9889

EG&G Wakefield Engineering, Inc.
60 Audubon Rd.
Wakefield, MA 01880
Phone: 617-246-0874
Fax: 617-224-3528

A.2 FAN HEAT SINK VENDORS

Sourceline, Inc. (Panasonic)
122 Charcot Ave.
San Jose, CA 95131
Phone: 408-727-5200
Fax: 408-727-3350

A.3 HEAT PIPE AND HEAT EXCHANGER VENDORS

Fujikara America, Inc.
3001 Oakmead Village Drive
Santa Clara, CA 95051
Phone: 408-988-7408 or 408-988-7415
Fax: 408-727-3515

Thermacore, Inc.
780 Eden Road
Lancaster, PA 17601
Phone: 717-569-6551
Fax: 717-569-4797

A.4 HEAT SINK ATTACHMENT VENDORS

MicroSi
1028 S 51st St.
Phoenix, AZ 85044
Phone: 602-893-8898
Fax: 602-893-8637

The Bergquist Company
5300 Edina Industrial Blvd.
Edina, MN 55439
Phone: 612-835-2322
Fax: 612-835-4156

A.5 BOARD MANUFACTURER

Avex Electronics Inc.
4807 Bradford Drive
Huntsville, Alabama 35805
Phone: 205-722-6000

A.6 COMPACTPCI SPECIFICATION

Rogers Communication
301 Edgewater Place, Suite 220
Wakefield, MA 01880
Phone: 617-224-1100
Fax: 617-224-1239

A.7 TEMPERATURE MEASUREMENT SUPPLIES

Omega Engineering, Inc.
One Omega Drive
P.O. Box 4047
Stamford, CT 06906
Phone: 1-800-622-2378

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intel®

AP-758

APPLICATION NOTE

Flash Memory PCI Add-In Card for Embedded Systems

September, 1997

Order Number: 273121-001

intel

AP-758

APPLICATION
NOTE

Flash Memory PCI Add-In Card for Embedded Systems

September, 1997

Order Number: 27121-001

1.0 Introduction

Embedded systems are typically designed to startup, operate, and store data to and from a type of non-volatile storage media. There are many types of non-volatile media, such as disc and tape drives. Silicon based, battery-backed volatile memory systems and non-volatile memory systems are also available. A typical embedded computing application does not require the vast amounts of storage space available from disk and tape drives. It is often impractical to use these media because of environmental limitations. Battery-backed semiconductor memory systems can provide suitable storage while the system is not operating, but reliability may be sacrificed because of limited battery lifetimes. Long term maintenance may also be an issue. For embedded systems, non-volatile semiconductor memory solutions can provide significant storage and robustness at an attractive price.

High performance embedded processors with their wide data buses and differing bus cycle protocols present a significant interface challenge to Flash memories. Three possible locations for the Flash memory interface can be considered when designing an embedded PC: the ISA bus, the PCI bus and the host bus.

Typically, the host bus cannot be heavily loaded due to speed considerations; this makes it impractical to add another host-to-Flash device to the host. Using current chipset technologies, placing the Flash on the DRAM bus would significantly reduce the bus speed and slow system performance.

Placing the Flash on the ISA bus would require dedicated logic to decode addresses, and to provide buffers and data steering. The ISA solution would be relatively slow and would limit the total amount of Flash memory to less than 16 Mbytes.

The PCI bus solution presents an easy to implement interface that can use current chipset technologies from the host processor bus. The PCI bus has good performance, industry standard protocols and provisions for system boot control.

Since typical chipsets do not directly support Flash memory interfaces, but commonly support host-to-PCI interfaces, a PCI-to-Flash solution was chosen for the proof of concept design.

The Flash Memory PCI Add-In Card was created to demonstrate the feasibility of interfacing Flash memory to the PCI bus in an embedded system. In such a system, Flash memory devices are used for high density and high performance mass storage for user code and data.

This application note describes a Flash Memory PCI Add-In Card design. This design is a proof-of-concept only. It is not a production product, nor is it being offered by Intel as such. This application note discusses design and software considerations specific to a prototype card assembled by Intel to demonstrate the feasibility of the PCI-to-Flash interface for various memory densities. This design and prototype can serve as a basis for customer designs. Several software utilities were developed for the prototype; these are described in this application note. Schematics of the prototype design and field programmable gate array (FPGA) are available for customers desiring to "copy exactly" the design presented here.

The PCI bus provides the interface between the microprocessor and the Flash memory. Since the PCI bus is widely accepted in the industry, the Flash Memory PCI Add-In Card can be easily integrated into existing systems that support the PCI bus, or it can be used in new PCI-bus-based designs. This easy integration can decrease time to market for new and retrofit designs.

An example of creating a new system with a shortened development time would be to use the Intel Embedded Processor Module (which supports PCI) and the Flash Memory PCI Add-In Card design. Designing a system using these components and appropriate baseboard support electronics saves considerable design time by eliminating the need to custom design the processor to Flash interface. For space sensitive systems without PCI connectors, the PCI-to-Flash interface can be designed to fit the system's form factor.

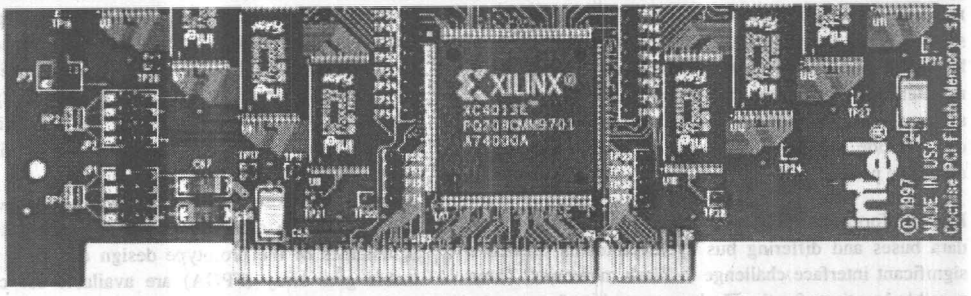


Figure 1. Flash Memory PCI Add-In Card

2.0 System Overview

The Flash Memory PCI Add-In Card Block diagram is shown in Figure 2.

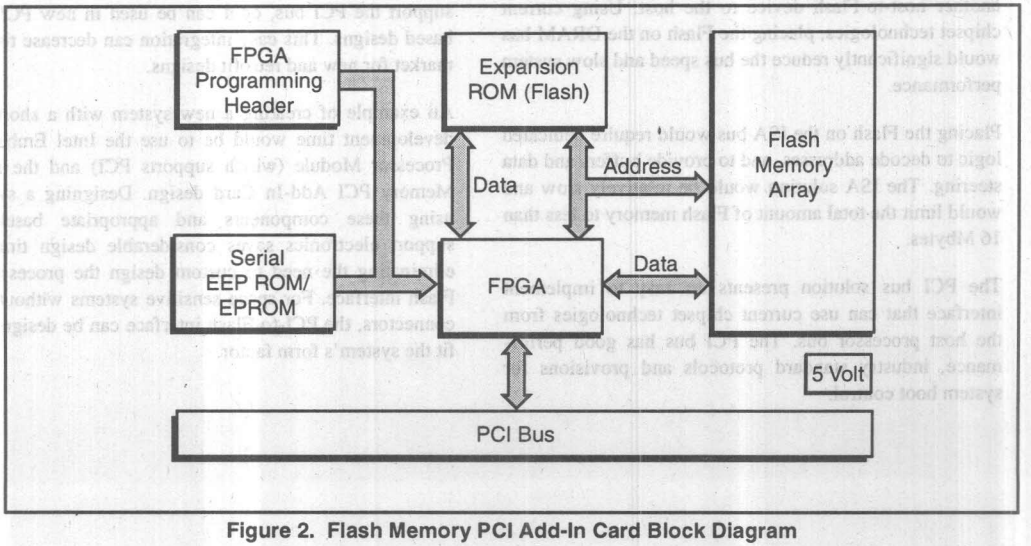


Figure 2. Flash Memory PCI Add-In Card Block Diagram

The Flash Memory PCI Add-In Card supports the PCI Local Bus Specification, revision 2.1, in both electrical characteristics and logical bus cycles. In accordance with allowable PCI protocols, it operates at 5 V on a standard 32-bit, 33 MHz bus. The card conforms to the specifications for a PCI Raw Variable Height Short Card as shown in Figure 5-3 of the PCI specification. This allows a maximum height of 4.2" and maximum length of 6.6". The card has a standard 32-bit PCI connector and operates on 5 V-only supply.

The card is designed around the Xilinx XC4000* family field programmable gate array (FPGA) with the PCI LogiCORE* interface. The PCI LogiCORE interfaces to the PCI bus and responds to all commands on the bus. The remaining FPGA logic responds to the commands from the PCI LogiCORE and generates appropriate address, data and control signals and sends them to the Flash array.

A programming header is available for FPGA programming alteration. You can write the program to the FPGA via a PC serial port. The serial ROM stores the FPGA program for configuration at power up. Once the ROM is downloaded to the FPGA, the card is ready to function.

The Flash Memory PCI Add-In Card supports the expansion ROM function. This function facilitates dead-start loads from the card at power up. The physical ROM is an Intel 2 Mbit (128 Kbit × 16 configuration) Boot Block Flash memory. This memory is set up in a ×16 mode to speed up data transfers.

The Flash Memory PCI Add-In Card supports plug-and-play operation and non-plug-and-play operation. The FPGA contains all necessary header information.

The Flash memory array is divided into four banks, with four devices in each bank. This banked array is supported by four memory density modes within the FPGA: 2 Mbyte, 8 Mbyte, 16 Mbyte and 32 Mbyte. Figure 3 shows the Flash memory array block diagram.

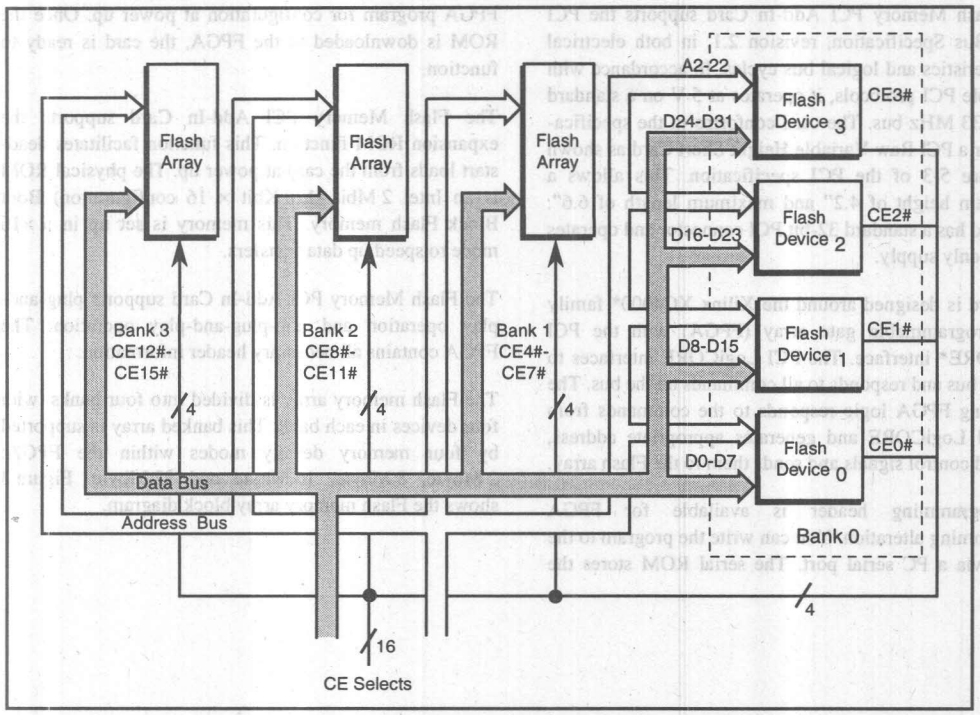


Figure 3. Flash Memory Array Block Diagram

The arrangement of the Flash devices represents a double word aligned memory array. This means that for a given 4 byte read/write starting on a double word boundary (address x00H) within bank 0, the 4 bytes reside in the Flash devices selected by CE0# through CE3# respectively. This is an important system consideration when defining software utilities and when programming and erasing the Flash. Refer to "Software Design Considerations" on page 9 for more information.

Intel's High-Density FlashFile™ Memory components are recommended for the memory array. These are symmetrically-blocked FlashFile architecture devices. They allow selective block locking and are pin compatible with other families of Intel Flash memory. This compatibility allows for upgrades to higher performance devices.

The card is operated using standard software routines that write and read Flash devices. Standard software may need to be modified to account for the following:

- The FPGA does *not* contain algorithms that automatically perform the multiple operations necessary to program and erase the Flash devices.
- The card does *not* support burst PCI transfers.

Table 1 describes the commands used to read, write, and erase the Flash, and the commands used to determine Flash status. Consult the applicable Flash device specification and user guide to fully understand the operation of Flash devices.

Table 1. Flash Command User Interface

Command[1]	Bus Cycles Required	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[2]	Addr[3]	Data[4]	Oper[2]	Addr[3]	Data[4]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	5	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	6	Write	BA	20H	Write	BA	D0H
Program	2	6,7	Write	PA	40H or 10H	Write	PA	PD
Block Erase and Program Suspend	1	5	Write	X	B0H			
Block Erase and Program Resume	1	5	Write	X	D0H			
Set Block Lock Bit	2	7	Write	BA	60H	Write	BA	01H
Set Master Lock Bit	2	7	Write	X	60H	Write	X	F1H
Clear Block Lock Bit	2	8	Write	X	60H	Write	X	D0H

NOTES:

1. Commands not listed in this table are reserved by Intel for future device implementations; use only the signals listed.
2. Bus operations are defined in the Flash datasheet.
3. X= Any valid address within the device
   IA= Identifier Code Address
   BA= Address within the block being erased or locked
   PA= Address of memory location to be programmed
4. SRD= Data read from status register.
   PD= Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE#, whichever goes high first
   ID= Data read from identifier codes
5. Following the Read Identifier codes command, read operations access manufacturer, device, lock block, and master lock codes.
6. When the block is locked, RP# must be at V_{HH} to enable block erase or program operations. Attempts to issue a block erase or program to a locked block while RP# is V_{IH} will fail.
7. Either 40H or 10H are recognized by the WSM as the program setup.
8. When the master lock bit is set, RP# must be at V_{HH} to clear lock-bits. The clear lock-bits operation simultaneously clears all block lock bits. When the master lock bit is not set, the Clear Lock Bits command can be done while RP# is V_{IH}.

3.0 System Operations and Performance

The next few sections provide a general description of reading, writing and erasing the Flash. See the datasheet for your Flash devices for specific instructions and programming flow diagrams.

3.1 Reading the Flash

PCI-to-Flash read transactions are handled by the FPGA. DEVSEL# is asserted back to the bus master during the fourth PCI clock cycle (slow DEVSEL# timing). Wait-state timing occurs during clock cycles 5-9; on cycle 10 the Flash data is valid and TRDY# and STOP# are asserted. This forces a target disconnect because burst transfers are not supported in this design. With this read timing, assuming 4 byte transfers, this design supports up to 12 Mbyte/s transfers. The host must recognize the PCI disconnect and keep track of addressing during what normally would be a burst transfer.

3.2 Writing the Flash

PCI-to-Flash write operations are similar to read operations (slow DEVSEL# timing) but complete in five PCI clock cycles; the assertion of STOP# signals that burst transactions are not supported. The maximum write rate to the Flash is 11 Mbyte/s, assuming 4 byte writes that are double-word aligned. The write performance is slightly less than the read performance because it takes two write cycles to complete the write operation (12 PCI cycles total, including the turnaround cycles per write transaction).

Execute a read command to return to reading the array.

3.3 Erasing the Flash

Erasing the Flash is accomplished by sending appropriate commands to the Flash array. This is no different than writing to the array, except that the first write to the array indicates a command to erase; the second write command confirms the erase command and indicates the block address to be erased. Similarly, commands to the array to determine Flash status are sent via writes, and status is read through normal read operations. Table 1 lists the transactions necessary to perform all Flash operations.

Execute a read command to return to reading the array.

3.4 Scaling Memory Size

The Flash Memory PCI Add-In Card supports four different memory sizes. Table 2 describes the devices and banks used in each of the memory size types.

Table 2. Memory Size versus Layout and Device Selection

Total Size	Device Layout	Flash Density	Product number	Access Time
2 Mbyte	4 × 1	4 Mbit	28F004S5	85 ns
8 Mbyte	4 × 1	16 Mbit	28F016S5	95 ns
16 Mbyte	4 × 2	16 Mbit	28F016S5	95 ns
32 Mbyte	4 × 4	16 Mbit	28F016S5	95 ns

For size-sensitive applications, the 4 × 1 bank option provides memory densities of 2 Mbyte and 8 Mbyte simply by changing out memory types. This can result in considerable cost savings over the life of a product, since no redesign is necessary for the memory upgrade. In applications for which larger amounts of memory are required and physical size limitations are not an issue, the designer may opt for the 2 or 4 bank solution.

The proof of concept design and FPGA support up to the full 4x4 memory configuration. In a custom design based on the proof of concept, the designer may opt to use only 1 or 2 banks when there are physical size limitations in the design.

3.5 Banked Memory Configuration Considerations

The memory system employed uses four separately selectable Flash memory devices connected to a 32-bit data bus. This presents a number of considerations that must be accounted for in system development, especially software.

It is possible to write single bytes to the Flash array, and there are no restrictions on addressing. However, when writing words or double words, the double-word boundaries must not be crossed in a single transaction. This causes unpredictable results.

For contiguous address read and writes, the user must be aware that the bytes are being stored across four separate Flash devices and not in one device. For instance, four byte writes to address (x)00H are written to Flash devices 0-3 at address represented by the (x) decoded value. Therefore, from a system standpoint, the Flash memory "block" is not 64 Kbytes as defined by each device, but rather 256 Kbytes as defined for the bank of memory. Similarly when it is desired to lock the first "block" of 256 Kbytes, the command must be available across all 32 bits of the write data to indicate to each Flash device that a block lock is requested.

Table 3. Flash Programming Code Example

```
MOV     EAX, 77777777H      ;Place lock block command across all 4
                            ;bytes to signal all 4 devices to lock the
                            ;block
MOV     [address], EAX      ;Write lock block command
MOV     EAX, D0D0D0D0H      ;Place confirm command across all 4
                            ;bytes to signal all 4 devices to confirm
                            ;lock block command
MOV     [address], EAX      ;Confirm lock block
MOV     EAX, FFFFFFFFH      ;Place read array command across all 4
                            ;bytes to signal all 4 devices to go to
                            ;read mode
MOV     [address], EAX      ;return to read mode for all of bank
```

The system programmer can overcome this addressing system and use a single Flash block (64 Kbytes) for code or data by offsetting each of the byte writes/reads by 4. This ensures that the data is assigned to a single Flash device as long as the bank boundary is not crossed. The user must decide which system suits the application best. The penalty for such a system is decreased throughput performance, since only 1 byte at a time can be read or written per PCI cycle. This reduces the performance to 3 Mbyte/s for reads and 2.75 Mbyte/s for writes.

The system designer/programmer should consider Flash wear leveling. If sections of the Flash are going to be erased and programmed many times over the life of the product, and others not used at all, some provision should be made to spread the program/erase cycles evenly between devices. This increases system data retention reliability and life.

3.6 Expansion ROM Operation

An Intel Boot Block Flash memory device is recommended as the PCI expansion ROM. This device operates in ×16 bit mode to speed boot load operations. The expansion ROM is accessed at power-up through the system BIOS. The ROM PCI cycle can provide the 4 bytes in 12 PCI clock cycles for a maximum read performance of 11 Mbytes/s.

During initialization the system BIOS checks the Expansion ROM header. The BIOS verifies that the header is correct (using signatures and checksums). Depending upon the capabilities of the BIOS and the data contained within the ROM header, the BIOS shadows the expansion ROM contents to shadow RAM and calls the initialization routine. The initialization routine is responsible for card specific initialization functions. Once the initialization is complete, the ROM initialization code returns to the BIOS for completion of the system initialization.

4.0 Hardware Considerations

4.1 Address Line Buffering

Since the address lines on the Flash side of the FPGA connect to as many as 17 devices, additional buffering is needed to accommodate the load. Each address line from the FPGA goes to two buffers and is distributed to memory. Address lines are routed through the address pins to minimize load reflections. Series resistors are employed to reduce reflections in the long lines connected to the memory arrays.

4.2 Choosing Memory Size

The Flash Memory to PCI Add-In Card has two sets of jumpers that select the configuration.

JP1: This block selects the Flash memory array size. This size is selectable from 64 Kbytes to 2 Gbytes. Only four sizes are currently supported by the chip-enable code within the FPGA: 2 Mbyte, 8 Mbyte, 16 Mbyte, and 32 Mbyte. Refer to the schematics for these jumper settings. (Schematics are available from the Intel World Wide Web site; see "Downloadable Files" on page 13 for more information.)

JP2: This configures the expansion ROM size. By default (all jumpers open) the expansion ROM is set at 64 Kbytes. The FPGA supports all sizes up to 2 Gbytes, although the PCI specification limits the Expansion ROM size to 16 Mbytes. Since there is only one socket for the expansion ROM, this size is really limited by the size of available Flash memory.

Jumpers or hardwired through-holes provide a cost effective configuration change mechanism for designs that support more than one memory size.

4.3 FPGA Options

The FPGA is programmed by a bitstream from either the serial ROM or from a PC. This bitstream was created by compiling the VHDL code and the LogiCORE netlist with the FPGA software tools from Xilinx. Once the FPGA is programmed with this bitstream it acts as the bridge between the PCI bus and the Flash memory array by converting the PCI bus transactions into Flash memory control signals.

The FPGA supports master and slave modes. The mode is selectable through jumper JP3. When the jumper block is open, the FPGA is in slave mode. In slave mode, the FPGA must be programmed through the header connection on the board using a PC and the appropriate tools. When the jumper is installed, the FPGA is in master mode and automatically downloads its configuration from the serial ROM.

The critical signals on the PCB are the traces between the PCI connector and the FPGA, and between the FPGA and the Flash memory devices. The traces between the FPGA and the PCI bus connector must be less than 1.5" long, except the PCI clock signal which must be 2.5" (+/- 0.1") long. This is a requirement of the PCI Local Bus Specification, revision 2.1.

To minimize the length of the address line traces, they are routed *through* the pins (rather than having stubs connecting the pins to the trace) of the Flash memory array devices which were laid out in an angular fashion.

Decoupling capacitors are located next to power pins on the devices and between the power and ground planes of the PCB to act as filters and reduce noise in the power signals. Refer to the schematics for information on the placement of decoupling capacitors. Decoupling consistent with published datasheets should always be employed.

The resistors placed on the address lines between the outputs of the buffers and the address lines of the Flash in Card. Instead, proprietary applications were used to demonstrate card functionality.

It is advisable for the card to begin executing after system start. An expansion ROM serves this function.

5.1 Software Design Considerations

The memory system uses four separately selectable Flash memory devices connected to a 32-bit data bus. This presents several software design considerations when programming the card.

5.1.1 Erasing/Programming Algorithms

Standard Flash implementations provide contiguous address space for each chip implemented. Since the card implements a 32-bit data bus, the algorithms used to erase and program devices must change.

Figure 4 shows the address map for a 16-byte block within the 32-bit data bus implementation.

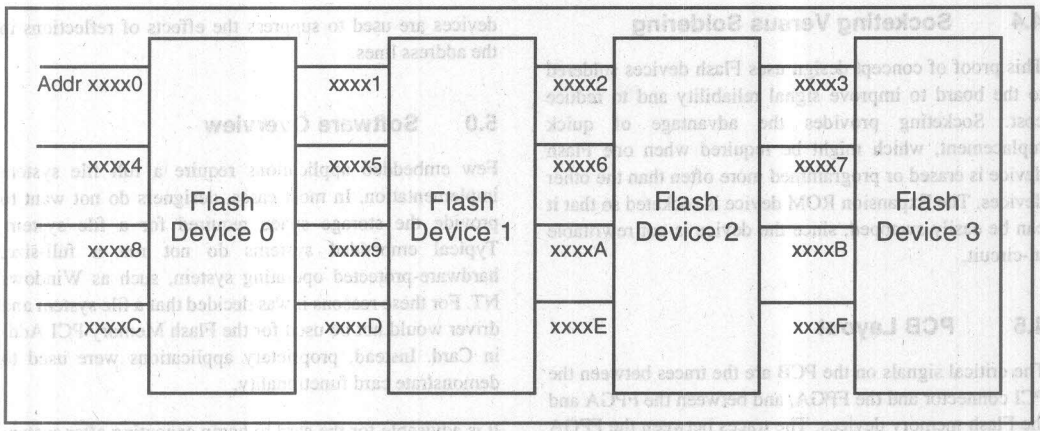


Figure 4. Memory Block Address Map

The erase/programming algorithms must take this into account since the contiguous address space spans multiple devices.

Two methods can be used to address this issue.

- The first method is to create an algorithm that accounts for the fact that consecutive addresses within the same device differ by 4 instead of 1. This method is useful only when the programmer is running diagnostic routines on a specific device.
- The second method involves taking advantage of the 32-bit data bus. When programming/erasing is initiated, the command code byte sent to the devices is replicated four times within a 32-bit command/data word. This invokes the program/erase operation on all four devices within that address line. When using this method, the programmer must verify that accesses are done on double-word boundaries. Once the command code is written, double-word accesses must then be performed to retrieve status from all four devices. A ready condition should not be acknowledged until ready is returned from all devices.

5.2 Applications

Several applications were created for the Flash Memory PCI Add-in Card. These are available for download from Intel's World Wide Web site (http://www.intel.com; see "Downloadable Files" on page 13 for more information). The following sections describe these applications.

5.2.1 COCHISE.EXE

COCHISE.EXE is a DOS executable that provides the following high-level functions:

- Plug and Play identification of device
- Flash part detection and identification
- Erase/Write/Read testing of entire Flash space
- Device erase capability
- Download of DOS file to Flash
- Upload of Flash contents and storage in file

The application is a menu based system that allows the user to choose which actions should take place.

5.2.2 CUPLOAD.EXE

CUPLOAD.EXE is a DOS executable that transfers a file from the system (motherboard) to the Flash. The executable verifies that the card exists in the system using Plug and Play (PnP) BIOS calls, gets the configuration information for the PCI device and the Flash devices, and then copies the file from the system to the Flash. The executable supports other functions. To determine the available options, type /? on the command line.

5.2.3 CDNLOAD.EXE

CDNLOAD.EXE is a DOS executable that transfers the contents of the Flash devices on the card to a specified DOS binary file. The executable verifies the existence of the card within the system (through the Plug and Play BIOS), retrieves the Flash device information, and copies the data from the Flash device to the specified file. To determine available options for the executable, use the /? Option on the command line.

5.3 Software Alternatives

The card could be used by an operating system as a nonvolatile storage device. To do this, the user must write a device driver that enables the operating system to format, write and read the Flash devices on the card. Several Flash file system alternatives exist that could be used once the driver is written. This option is not addressed within this application note.

5.4 Boot Execution

Typical embedded applications do not require user interaction before they begin execution. Possible solutions to execute the code stored in the card upon system start are dependent upon the capabilities of the system BIOS. The following sections describe the options based upon the capabilities of the BIOS.

5.4.1 BIOS Boot Specification 1.01

The BIOS Boot Specification as defined by Compaq, Phoenix Technologies and Intel provides the means for any device in a system to be identified as an Initial Program Load (IPL) device. If the system BIOS supports this specification, the expansion ROM within the card can indicate that it is an available IPL device.

The BIOS maintains a list of available IPL devices and assigns a priority to the devices. The user can change to the IPL order/priority of the available devices. If the expansion ROM is used as an IPL device, the IPL code must be contained within the expansion ROM space of the card. The system BIOS calls the Bootstrap Entry Vector (BEV) to boot the operating system. The expansion ROM either copies the OS to DRAM for execution or jumps directly to the entry point of the image contained in Flash. Example ROM code is available which provides an example of how to implement a Plug and Play IPL device. Please see the BIOS Boot Specification for a complete description of all required tables and actions to support this capability.

5.4.2 Expansion ROM Initialization

If the system BIOS does not support the PnP Boot Process, the expansion ROM can take advantage of the expansion ROM initialization. During the POST process, the system BIOS shadows all valid expansion ROMs and calls the initialization routines. The card can determine if the BIOS supports the PnP installation and boot process by checking input parameters provided to the unitization routine.

If the system BIOS does not support the BIOS boot specification (as determined at run time by the expansion ROM), the expansion ROM can perform any necessary initialization, and prior to returning control to the system BIOS can perform one of the following actions:

- Provide a option screen for the user to select available boot options
- Automatically load the image to DRAM from Flash and execute
- Jump to the entry point in the Flash image to provide eXecute In Place (XIP) for the image

When this method is used, it is recommended to use the first option. If the other options are chosen, the flexibility of the system to boot from alternate devices upon request and recover from boot failure is limited.

6.0 VHDL Code

Figure 5 shows the functional block diagram of the VHDL code used for the Flash Memory PCI Add-In Card design. VHDL code is available from Intel's World Wide Web site (http://www.intel.com; see "Downloadable Files" on page 13 for more information).

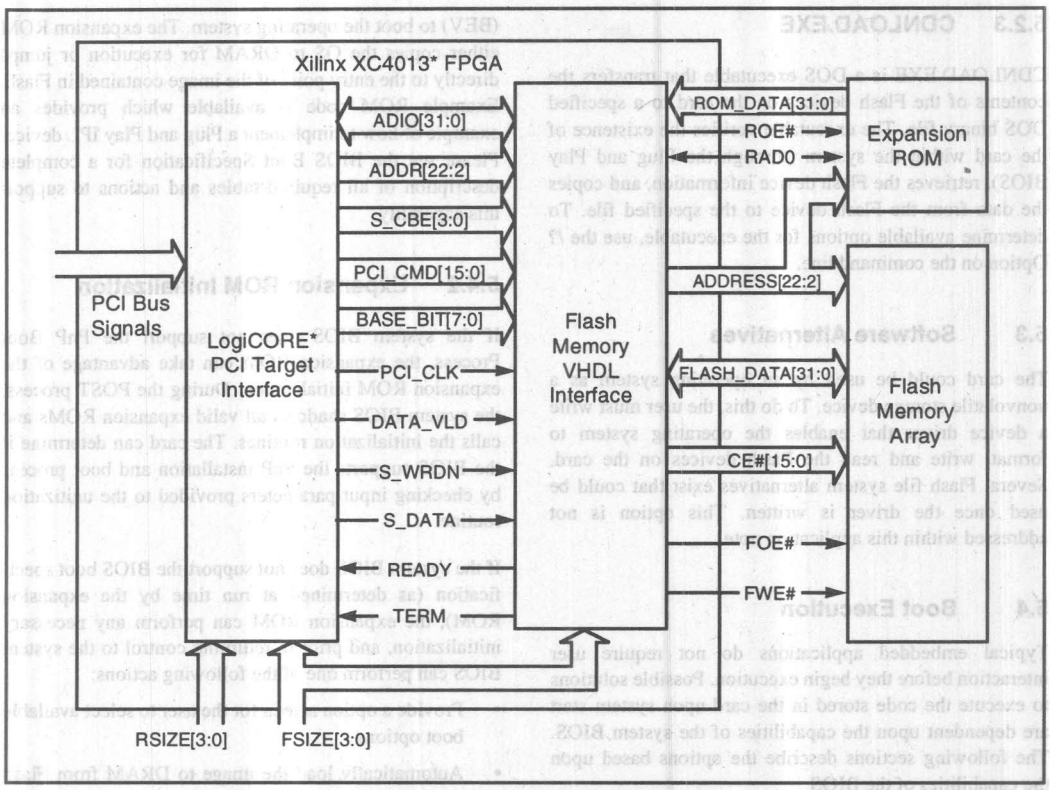


Figure 5. VHDL Code Block Diagram

7.0 Schematic and Material List

Schematics and the material list are available from Intel's World Wide Web site (http://www.intel.com; see "Downloadable Files" on page 13 for more information).

8.0 Vendor Contact List

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
(408)559-7778

Intel Corporation
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(408) 765-8080

9.0 Specification Summary

PCI compatibility:	Revision 2.1
Logical PCI Interface:	Xilinx LogiCORE PCI Slave Interface (LC-DI-PCIS-C)
Programmable Logic:	Xilinx XC4013E-2PQ208C
Configuration PROM:	XC17256DPD8C, 256 Kbit Serial PROM
Development Software:	Synopsys* VHDL FPGA-Compiler, Xilinx Foundation Series 6.0.2, XACT* 6.0 for PC
Flash Array Devices:	Intel FlashFile™ Memory Architecture 28F004S5, 28F016S5
Flash access time:	85 ns (28F004S5), 95 ns (28F016S5)
Expansion ROM:	Intel Boot Block Flash Memory (E28F200-B5-B60)
Electrical voltage:	5 V_{cc}, 5 V_{pp}
Operating Frequency:	33 MHz
Data Path:	32 bits

10.0 Related Documents

These documents are available for download from Intel's World Wide Web site at http://www.intel.com.

Table 4. Related Documents

Document	Order Number
Byte-Wide Smart 5 FlashFile™ Memory Family datasheet	290597
2-Mbit Boot Block Flash Memory Family datasheet	290448
Intel Embedded Processor Module datasheet	273105
Intel Embedded Processor Module Evaluation Board Developer's Manual	273122
PCI Local Bus Specification, Revision 2.1	This document can be ordered from the PCI Special Interest group at: http://www.pcisig.com

10.1 Downloadable Files

Files mentioned in this document are available for download from the Intel World Wide Web site at http://www.intel.com. Search for FL_AIC.EXE to find the following information related to the Flash Memory PCI Add-In Card proof of concept design:

- Bill of Materials for the card
- VHDL source code and description
- FPGA Serial ROM code used on the card
- Software executables discussed in this application note
- Schematics for the card

Chapter 4: Mobile Pentium® Processors

PENTIUM® PROCESSORS FOR MOBILE SYSTEMS

INTRODUCTION

Intel manufactures a reduced power version of the Pentium® processors, including the Pentium processor with voltage reduction technology, the mobile Pentium processor with MMX™ technology (0.35 Micron), and the latest mobile Pentium processor with MMX technology on 0.25 Micron, targeting the mobile market. The Pentium processor for mobile systems is offered in the Tape Carrier Package (TCP), the Plastic Pin Grid Array (PPGA) package, and Intel Mobile Module. It has all the advanced features of the Pentium processor for desktop systems.

The mobile Pentium processor with MMX technology on 0.25 Micron has several features which allow high-performance notebooks to be designed, including the following:

- TCP dimensions are ideal for small form-factor designs.
- TCP has superior thermal resistance characteristics.
- 1.8V (166/200/233MHz)/2.0V (266MHz) core and 2.5V I/O buffer V_{CC} inputs reduce power consumption significantly.
- The SL Enhanced feature set, which was initially implemented in the Intel386™ CPU.

The architecture and internal features of the mobile version of the Pentium processor are identical to the desktop processor specifications provided in this document, except several features not used in mobile applications which have been eliminated to streamline it for mobile applications. The mobile Pentium processor family now consists of the following products:

- Mobile Pentium® processor with MMX™ technology on 0.25 micron at 266 MHz
- Mobile Pentium processor with MMX technology on 0.25 micron at 233 MHz
- Mobile Pentium processor with MMX technology on 0.25 micron at 200 MHz
- Mobile Pentium processor with MMX technology on 0.25 micron at 166 MHz
- Mobile Pentium processor with MMX technology at 166 MHz
- Mobile Pentium processor with MMX technology at 150 MHz
- Mobile Pentium processor with MMX technology at 133 MHz
- Mobile Pentium processor with MMX technology at 120 MHz
- Mobile Pentium processor at 150 MHz
- Mobile Pentium processor at 133 MHz
- Mobile Pentium processor at 120 MHz

DOCUMENT REFERENCE LIST

For information regarding Pentium processors for mobile systems, you may obtain documents listed in the table below by calling our toll-free Literature Distribution Center at 800-548-4725 in the U.S. and Canada. For all other geographies, please contact your local sales office or distributor.

Document Reference List

Document Title	Document Type	Document Number
Pentium® Processor with MMX™ Technology on 0.25 Micron Mobile Module	Datasheet	243515[2]
Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron	Datasheet	243468[2]
Intel Pentium® Processor with MMX™ Technology Mobile Module	Datasheet	243328[2]
Mobile Pentium® Processor with MMX™ Technology	Datasheet	243292[2]
Pentium® Processor at iCOMP® Index 815\100 MHz Pentium Processor at iCOMP Index 735\90 MHz Pentium Processor at iCOMP Index 610\75 MHz with Voltage Reduction Technology	Datasheet	242973[2]
Pentium® Processor at iCOMP® Index 610\75	Datasheet	242323[2]
Pentium® Processors with Voltage Reduction Technology at 75/100/120/133/150 MHz	Datasheet	242557[2]
Mobile Pentium® Processor with MMX™ Technology Performance Brief	Performance Brief	243302[2]
Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron System Design Considerations	Design Guide	243571[2]
Notebook Power Computing: Power and Performance Analysis	Application Note	243308[2]
AP-577 An Introduction to Plastic Pin Grid Array (PPGA) Packaging	Application Note	243103[2]
Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems	Application Note	242558[1]
Pentium® Processor (610\75) Design Considerations for Mobile Systems	Application Note	242417[1]
Pentium® Processor (610\75) Power Supply Considerations for Mobile Systems	Application Note	242415[1]
Packaging	Databook	240800[2]

NOTE:

1. These documents may be obtained by contacting your local sales office.
2. These documents may also be obtained by visiting Intel's web site at http://www.intel.com/design/mobile

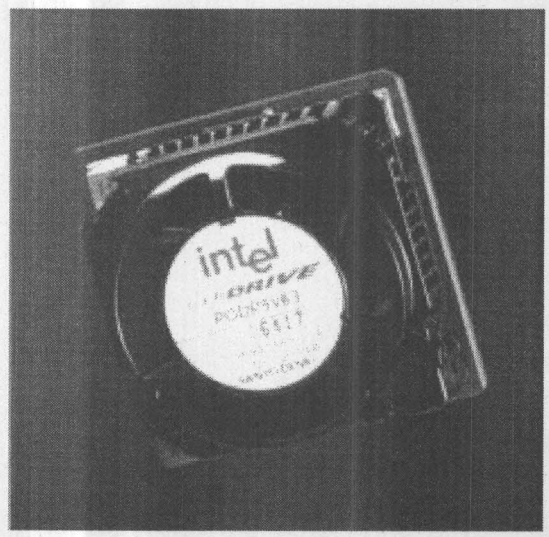
Chapter 5: Pentium® OverDrive® Processors

Chapter 5: Pentium® OverDrive® Processors

INTEL Pentium® OverDrive® PROCESSOR

- **Powerful CPU Upgrade for Intel486™ CPU-Based Systems**
  - **— Makes Intel Procesor-Based Systems Run Faster**
  - **— Significantly Accelerates All Software Applications**
- **Designed for Systems Based on:**
  - **— Intel486™ SX Processors**
  - **— Intel486™ DX Processors**
  - **— IntelSX2™ Processors**
  - **— IntelDX2™ Processors**
- **Compatible with Installed Base of Thousands of Applications**
- **Based on Advanced Intel Pentium® Processor Technology**
- **Incorporates SMM Power Saving Features**

The Pentium® OverDrive® processor upgrades Intel486™ processor-based systems to Pentium processor technology. It features a true Pentium processor core (Superscalar Architecture, Branch Prediction, and faster floating point unit), silicon enhancements (separate code and data caches, 16 KB each, and 32-bit bus interface), and package innovations (on-package voltage regulation and fan heat sink).



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June 1995 **Order Number: 290544-001**

INTEL Pentium® OverDrive® PROCESSOR

- Powerful CPU Upgrade for Intel486™ CPU-Based Systems
  - Makes Intel Processor-Based Systems Run Faster
  - Significantly Accelerates All Software Applications
- Designed for Systems Based on:
  - Intel486™ SX Processors
  - Intel486™ DX Processors
  - Intel SX2™ Processors
  - Intel DX2™ Processors
- Compatible with Installed Base of Thousands of Applications
- Based on Advanced Intel Pentium® Processor Technology
- Incorporates 3 Mil Power Saving Features

The Pentium® OverDrive® processor upgrades Intel486™ processor-based systems to Pentium processor technology. It features a true Pentium processor core (Superscalar Architecture, Branch Prediction, and Pentium floating point unit), silicon enhancements (separate code and data caches, 16 KB each, and 32-bit bus interface), and package innovations (on-package voltage regulation and fan heat sink).

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June 1995 Order Number 290544-007

1.0 INTRODUCTION

This data sheet describes the Intel Pentium OverDrive processor, a CPU upgrade for most Intel486 SX, Intel486 DX, IntelSX2, and IntelDX2 processor-based systems. This processor upgrade will significantly accelerate all software applications run on your existing system, thereby increasing the overall performance of your PC.

It is important to note that this data sheet is intended to be used in conjunction with the *Intel486 Microprocessor Family Databook* (242202-002). Only information which is not in the databook will be included in this datasheet.

1.1 Pentium® OverDrive® Processor Product Overview

The Pentium OverDrive processor is the highest performance CPU upgrade available for systems based on the Intel486 family of CPUs. It brings Pentium processor technology (including Superscalar Architecture, Branch Prediction, faster floating-point unit, and separate data and code caches) to Intel486 processor-based systems.

Inclusion of the Pentium OverDrive processor socket in systems based on the Intel486 family of microprocessors provides the end user with an easy and cost-effective way to increase system performance. The majority of upgrade installations which take advantage of the Pentium OverDrive processor socket will be performed by end users and resellers. Therefore, it is important that the design be "end user easy", and that the amount of training and technical expertise required to install the OverDrive processors be minimized. Upgrade installation instructions should be clearly described in the system user's manual. In addition, by making installation simple and foolproof, PC manufacturers can reduce the risk of system damage, warranty claims and service calls. Feedback from Intel's upgrade customers highlight three main characteristics of end user easy designs: accessible socket location, clear indication of upgrade component orientation, and minimization of insertion force. Recommendations regarding designing for easy upgradability appear in Section 9.

1.2 Product Description

The Pentium OverDrive processor is designed to upgrade systems based on Intel486 SX, Intel486 DX, IntelSX2, and IntelDX2 processor-based systems and is based on Intel's Pentium processor technology. It is 100% binary compatible with the 8086/88, 80286, Intel386 DX, Intel386 SX, Intel486 DX, Intel486 SX, IntelSX2, and the IntelDX2 processor family.

The Pentium OverDrive processor provides significant improvements over the Intel486 CPU including:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Separate 16K Code and 16K Data Caches
- Improved Instruction Execution Times
- Write back MESI Protocol implemented in Data Cache
- System Management Mode

The Pentium OverDrive processor significantly increases the integer performance, and can attain up to 2x floating-point performance relative to an equivalent frequency IntelDX2 processor. The initial target bus frequencies for the Pentium OverDrive processor are 25 MHz and 33 MHz.

Figure 1-1 shows the Pentium OverDrive processor's two pipelines and floating-point unit that are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, 2 floating point instructions) in one clock.

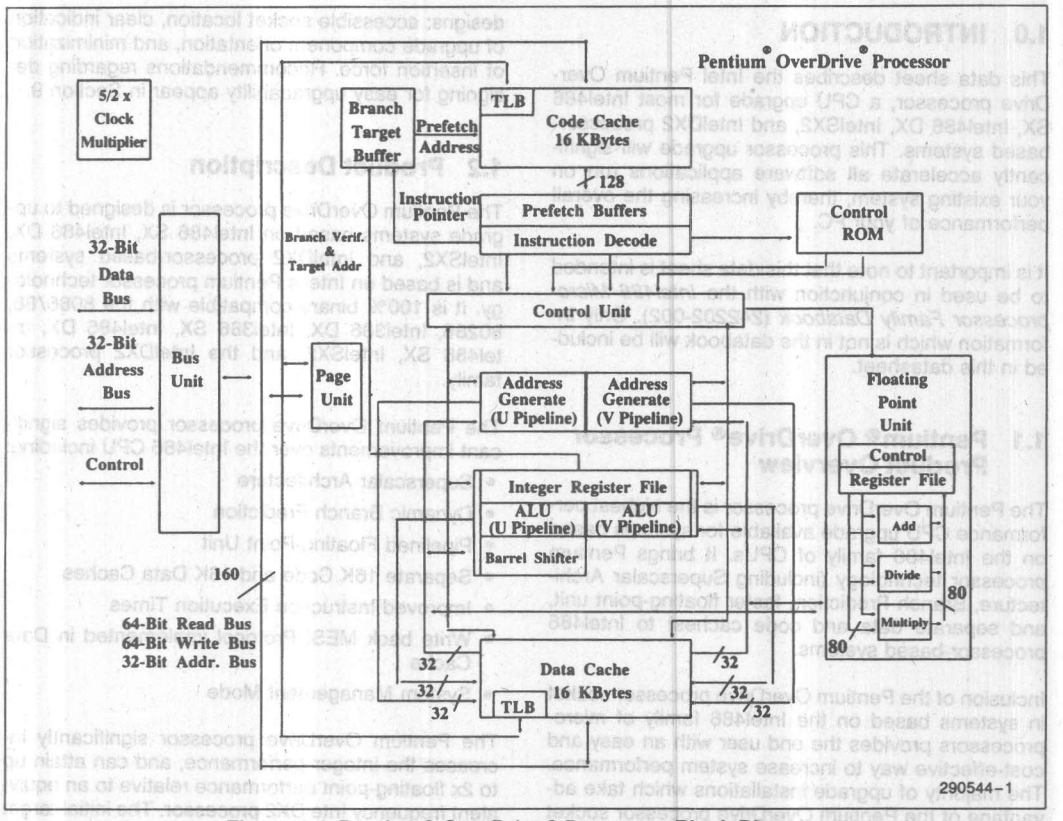


Figure 1-1. Pentium® OverDrive® Processor Block Diagram

The floating-point unit has been completely redesigned over the IntelDX2 processor. Faster algorithms provide at least 3X internal speed-up for common floating point operations including ADD, MUL, and LOAD. With instruction scheduling and overlapped (pipelined) execution, these three performance enhancements can allow many math intensive applications to achieve a 2X performance boost.

The Pentium OverDrive processor implements 32-bit address and data busses.

The block diagram shows that the Pentium OverDrive processor contains two instruction pipelines, the "u" pipe and the "v" pipe. Both the u- and the v-pipes execute integer instructions, while only the u-pipe executes floating point instructions. The one exception is the FXCH instruction which may also be executed in the v-pipe. Therefore, the Pentium OverDrive processor is capable of executing two integer instructions in each clock, or one floating point instruction in each clock. Floating point instructions can be paired in certain conditions(1). Each pipeline has its own address generation logic, arithmetic logic unit and data cache interface.

NOTE:

1. Refer to the *Pentium Processor Data Book* for more information on instruction execution timing and pairing.

Note that there are two separate caches, a code cache and a data cache. The data cache has three tag ports, one for each of the two pipes and one dedicated to handle snoops from other processors. It has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

Pentium OverDrive processor architecture. The control ROM unit has direct control over both pipelines.

1.3 Purpose of this Document

This document describes the system architecture and physical environment of the Pentium OverDrive processor. It also outlines differences between the Intel486 Family of processors and the Pentium OverDrive processor.

1.4 Compatibility Note

In this document, some register bits are shown as "Intel Reserved" (RES) and some pins are marked as "No Connects" (NC) or "Reserved" (RES). When reserved bits are called out, treat them as fully undefined. This is essential for software compatibility with future processors. When a pin is marked as a "NC" or "RES" it is important to not connect any other signals to such pins to ensure proper operation. Intel strongly recommends that you follow the guidelines below:

1) Do not depend on the states of any undefined bits when testing the values of defined register bits. Mask them out when testing.
2) Do not depend on the states of any undefined bits when storing them to memory or another register.

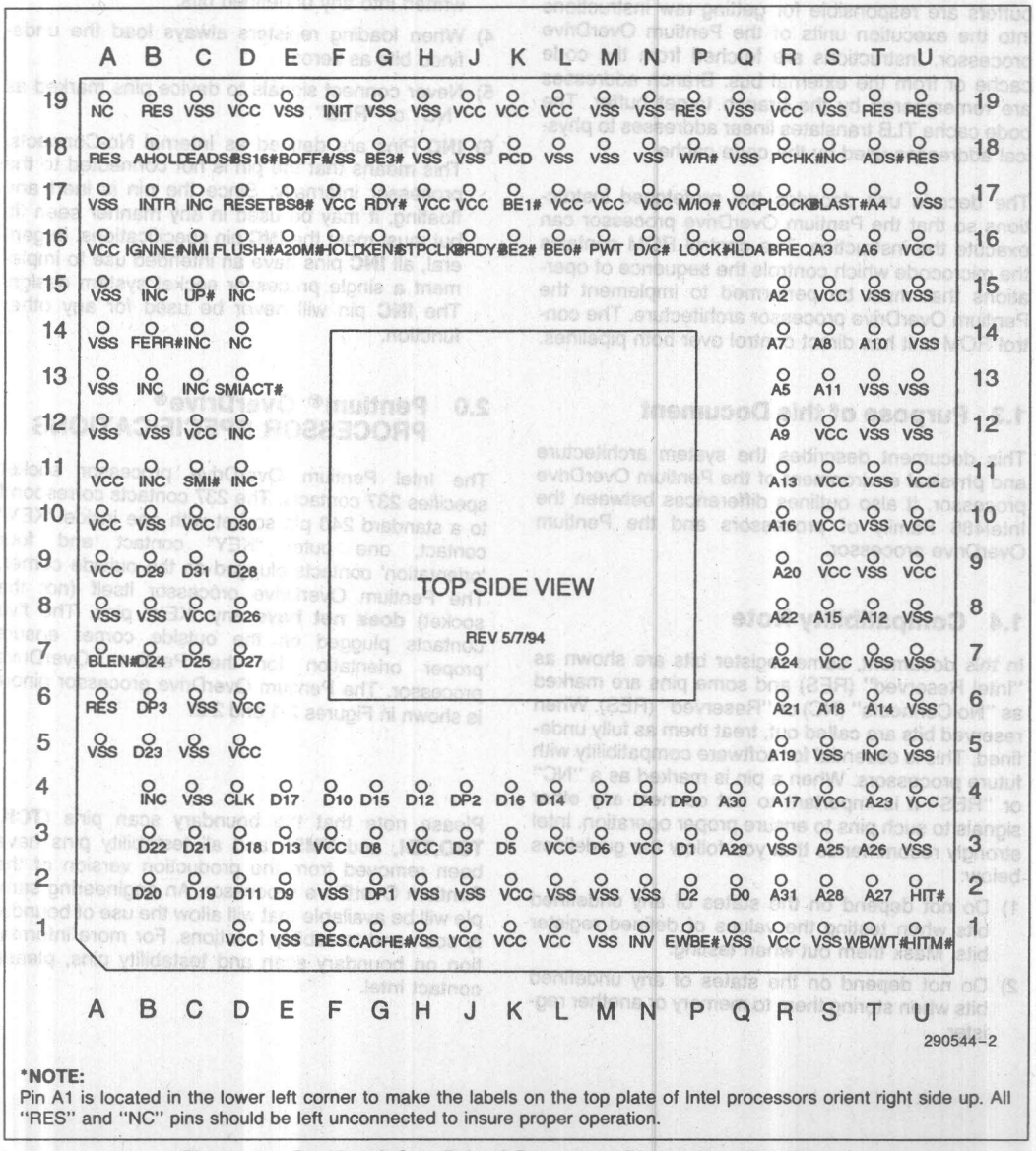
The **INC** pin will never be used for any other function.

2.0 Pentium® OverDrive® PROCESSOR SPECIFICATIONS

The Intel Pentium OverDrive processor socket specifies 237 contacts. The 237 contacts correspond to a standard 240 pin socket with one inside "KEY" contact, one outer "KEY" contact and four 'orientation' contacts plugged on the outside corner. The Pentium OverDrive processor itself (not the socket) **does not have** any "KEY" pins. The five contacts plugged on the outside corner ensure proper orientation for the Pentium OverDrive processor. The Pentium OverDrive processor pinout is shown in Figures 2-1 and 2-2.

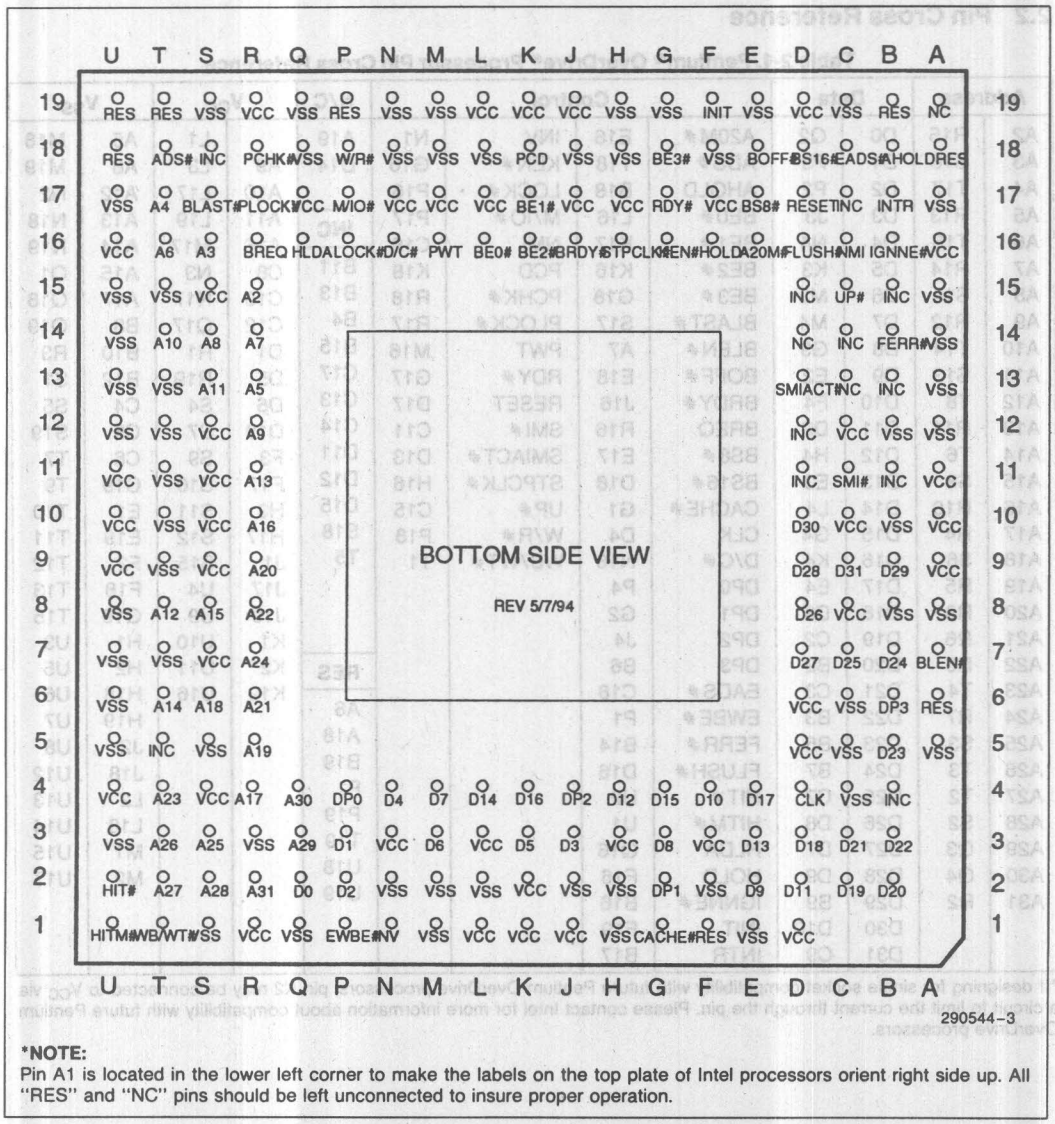
Please note that the boundary scan pins (**TCK, TDO,TDI,** and **TMS**), and all testability pins have been removed from the production version of the Pentium OverDrive processor. An engineering sample will be available that will allow the use of boundary scan and testability functions. For more information on boundary scan and testability pins, please contact Intel.

2.1 Pentium® OverDrive® Processor Pinout



***NOTE:**
Pin A1 is located in the lower left corner to make the labels on the top plate of Intel processors orient right side up. All "RES" and "NC" pins should be left unconnected to insure proper operation.

Figure 2-1. Pentium® OverDrive® Processor Pinout (Top Side View)



***NOTE:**
Pin A1 is located in the lower left corner to make the labels on the top plate of Intel processors orient right side up. All "RES" and "NC" pins should be left unconnected to insure proper operation.

Figure 2-2. Pentium® OverDrive® Processor Pinout (Bottom Side View)

2.2 Pin Cross Reference

Table 2-1. Pentium® OverDrive® Processor Pin Cross Reference

Address		Data		Control				N/C	V_{CC}		V_{SS}	
A2	R15	D0	Q2	A20M#	E16	INV	N1	A19		L1	A5	M18
A3	S16	D1	P3	ADS#	T18	KEN#	G16	D14	A9	L3	A8	M19
A4	T17	D2	P2	AHOLD	B18	LOCK#	P16		A10	L17	A12	N2
A5	R13	D3	J3	BE0#	L16	M/IO#	P17	INC	A11	L19	A13	N18
A6	T16	D4	N4	BE1#	K17	NMI	C16		A16	M17	A14	N19
A7	R14	D5	K3	BE2#	K16	PCD	K18	B11	C8	N3	A15	Q1
A8	S14	D6	M3	BE3#	G18	PCHK#	R18	B13	C10	N17	A17	Q18
A9	R12	D7	M4	BLAST#	S17	PLOCK#	R17	B4	C12	Q17	B8	Q19
A10	T14	D8	G3	BLEN#	A7	PWT	M16	B15	D1	R1	B10	R3
A11	S13	D9	E2	BOFF#	E18	RDY#	G17	C17	D5	R19	B12	S1
A12	T8	D10	F4	BRDY#	J16	RESET	D17	C13	D6	S4	C4	S5
A13	R11	D11	D2	BREQ	R16	SMI#	C11	C14	D19	S7	C5	S19
A14	T6	D12	H4	BS8#	E17	SMIACT#	D13	D11	F3	S9	C6	T7
A15	S8	D13	E3	BS16#	D18	STPCLK#	H16	D12	F17	S10	C19	T9
A16	R10	D14	L4	CACHE#	G1	UP#	C15	D15	H3	S11	E1	T10
A17	R4	D15	G4	CLK	D4	W/R#	P18	S18	H17	S12	E19	T11
A18	S6	D16	K4	D/C#	N16	WB/WT#	T1	T5	J1	S15	F2	T12
A19	R5	D17	E4	DP0	P4				J17	U4	F18	T13
A20	R9	D18	D3	DP1	G2				J19	U9	G19	T15
A21	R6	D19	C2	DP2	J4				K1	U10	H1	U3
A22	R8	D20	B2	DP3	B6			RES	K2*	U11	H2	U5
A23	T4	D21	C3	EADS#	C18				K19	U16	H18	U6
A24	R7	D22	B3	EWBE#	P1			A6			H19	U7
A25	S3	D23	B5	FERR#	B14			A18			J2	U8
A26	T3	D24	B7	FLUSH#	D16			B19			J18	U12
A27	T2	D25	C7	HIT#	U2			F1			L2	U13
A28	S2	D26	D8	HITM#	U1			P19			L18	U14
A29	Q3	D27	D7	HLDA	Q16			T19			M1	U15
A30	Q4	D28	D9	HOLD	F16			U18			M2	U17
A31	R2	D29	B9	IGNNE#	B16			U19				
		D30	D10	INIT	F19							
		D31	C9	INTR	B17							

*If designing for single socket compatibility with future Pentium OverDrive processors, pin K2 may be connected to V_{CC} via a circuit to limit the current through the pin. Please contact Intel for more information about compatibility with future Pentium OverDrive processors.

2.3 Pentium® OverDrive® Processor Pin Descriptions

This section provides a summary of the Pentium OverDrive processor pins and how they function. For more information on the pinout differences between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor, please see Section 10.

2.3.1 SIGNAL DESCRIPTIONS

Table 2-2 provides a brief pin description.

Table 2-2. Signal Description

Symbol	Type	Name and Function
INTERRUPTS		
INIT	I	The **INIT** pin is the Pentium OverDrive processor initialization pin. Since the SL-enhanced Intel486 processors implement this functionality on the **SRESET** pin, the corresponding pin (D11) on the Pentium OverDrive Processor is defined as an **INC** pin so that pin F19 and pin D11 may be tied together on the motherboard. **INIT** will force the Pentium OverDrive Processor to begin execution in a known state. The processor state after **INIT** is the same as the state after **RESET** except that the internal caches, floating point registers, and the SMM base register retain whatever values they had prior to **INIT. INIT** may NOT be used in lieu of **RESET** after power-up. **INIT** can not be used to cause the processor to enter BIST or Tri-State Test Mode. INIT is an edge triggered interrupt and is processed at instruction boundaries. Since **INIT** is an interrupt, **ADS#** may be driven even if **INIT** is active. Recognition of **INIT** is guaranteed in a specific clock if it is asserted synchronously and meets setup and hold times. To guarantee recognition if **INIT** is asserted asynchronously, it must have been deasserted for a minimum of two clocks before being returned active to the processor and remain asserted for a minimum pulse width of two clocks. **INIT** must remain active for three clocks prior to the **BRDY#** or **RDY#** of I/O write cycle to guarantee the processor recognizes and performs **INIT** right after I/O write instruction. **INIT** is asynchronous but must meet setup and hold times t_{20} and t_{21} to be recognized on any one clock. **INIT** is supplied with an internal pull-down.
CACHE CONTROL		
WB/WT#	I	This pin allows a cache line to be defined as *write back or write through* on a line by line basis. As a result, it controls the MESI state that the line is saved in. This pin is sampled in the clock in which the first **BRDY#** or **RDY#** is returned for a read cycle or a write through cycle. However, it must the meet setup and hold times at every clock. Cache lines are not allocated on write through cycles. This pin is also used as a configuration pin at the falling edge of **RESET** only. If **WB/WT#** is driven low, or left unconnected, the processor will operate in a **standard bus (write through only)** mode. This means that the Pentium OverDrive processor will run in an IntelDX2 processor compatible write through only cache mode. If **WB/WT#** is driven high, the processor will operate in enhanced bus **(write back)** mode. **INIT** can not be used to change the mode of the processor with **WB/WT#.** During **RESET, WB/WT#** should be held at its desired value for two clocks before and after the falling edge of **RESET. WB/WT#** is ignored when the processor is in **standard bus** mode. Please see Section 3 for a detailed description of the two modes of operation. **WB/WT#** has an internal pull down resistor to force the processor into the **standard bus** mode if left unconnected. The pin timings must meet setup and hold times t_{38} and t_{39} on every clock edge.

Table 2-2. Signal Description (Continued)

Symbol	Type	Name and Function
CACHE INQUIRE		
EWBE#	I	The *External Write Buffer Empty* pin, when inactive (HIGH), indicates that a write through cycle is pending in the external system. When the processor generates a non-write back cycle, and **EWBE#** is sampled inactive, the processor will hold off all subsequent writes to all E- or M- state lines until all write-through cycles have completed, as indicated by **EWBE#** going active. This ensures that writes are visible from outside the processor in the same order as they were generated by software. When the Pentium OverDrive processor serializes instruction execution through the use of a serializing instruction, it waits for **EWBE#** to go active before fetching and executing the next instruction. **EWBE#** is sampled with each **BRDY#** or **RDY#** of a write through cycle. If sampled inactive, the processor will repeatedly sample **EWBE#** in each clock until it is found active. Once sampled active, it will ignore **EWBE#** until the next **BRDY#** or **RDY#** of a write cycle. **EWBE#** is not sampled and has no effect on processor operation while the processor is in standard bus mode. If unused, **EWBE#** should be tied LOW or left unconnected. **EWBE#** is active low and must meet setup and hold times t_{38} and t_{39} and is supplied with an internal pull-down.
HIT#	O	This pin participates in an inquire cycle. If an inquire cycle hits a valid line in the processor, this pin is asserted two clocks after **EADS#** has been driven to the processor. If the inquire cycle misses in the processor cache, this pin is negated two clocks after **EADS#.** This pin changes its value only as a result of inquire cycle as described above and retains its value between any two inquire cycles.
HITM#	O	**HITM#** is asserted when an inquire cycle hits a modified line in the Pentium OverDrive processor. It can be used to inhibit another bus master from accessing the data until the line is completely written back. **HITM#** is asserted two clocks after an **EADS#** assertion hits a modified line in the processor cache and deasserts after the last **BRDY#** or **RDY#** of the corresponding write back is returned. **HITM#** is guaranteed to be deasserted before the **ADS#** following a write back cycle. If an INVD instruction occurs at the same time as an external snoop, **HITM#** may be asserted and deasserted without a corresponding **ADS#** for a write back cycle.
CACHE BURST CONTROL		
BLEN#	I	**BLEN#** controls if write back cycles will be attempted to run as burst cycles. When **BLEN#** is HIGH, the processor will write out a dirty line as four separate writes, each with its own **ADS#** and **BLAST#.** When **BLEN#** is LOW, a write back is done as a 16 byte burst. Since **BLEN#** is a constant input, meaning that it will have to be tied HIGH or LOW. As a result, it does not have setup and hold time specifications. **BLEN#** is has no effect and is not sampled when the processor is in **standard bus** mode. **BLEN#** is supplied with an internal pull-up resistor.
CACHE#	O	The **CACHE#** pin is used to indicate a cache operation. **CACHE#** will be active along with the first **ADS#** until the first **RDY#/BRDY#** and is undefined during any other time period. On cacheable read accesses, **CACHE#** will be asserted when **PCD** is low, except on locked cycles. **CACHE#** will always be asserted in the beginning of cacheable reads (line fills and code prefetches) and can be used as an indication that the processor intends to perform a linefill. For write cycles, **CACHE#** is active for write backs only. The beginning of a replacement write back can be uniquely identified by the presence of **ADS#, W/R#** and **CACHE#** together. The beginning of a snoop write back is marked by **ADS#, W/R#, CACHE#** and **HITM#** being active together.

Table 2-2. Signal Description (Continued)

Symbol	Type	Name and Function
OEM CPU INTERFACE		
UP#	O	The *upgrade present* pin is used to signal the system OEM microprocessor to float its outputs and stop driving the bus. It is active low and is never floated. **UP#** is driven low at power-up and remains active for the entire duration of the Pentium OverDrive processor operation.
INC PINS		
INC		The **INC** pin is defined to be an *internal no-connect*. This means that the pin is not connected internally, and may be used for the routing of external signals. It will never be used for any other function, and is guaranteed to remain an **INC** pin. Any voltage level applied to an **INC** pin must remain within the processor V_{CC} specifications. Most **INC** pins have a specified use in creating a design that supports multiple processors in one socket. For more information, please see Section 9.

2.3.2 OUTPUT PINS

Table 2-3 lists all the output pins, indicating their active level, and when they are floated.

Table 2-3. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE3#–BE0#	LOW	Bus Hold, Backoff
PWT, PCD	HIGH	Bus Hold, Backoff
W/R#, D/C#, M/IO#	LOW	Bus Hold, Backoff
LOCK#	LOW	Bus Hold, Backoff
PLOCK#	LOW	Bus Hold, Backoff
ADS#	LOW	Bus Hold, Backoff
BLAST#	LOW	Bus Hold, Backoff
PCHK#	LOW	
FERR#	LOW	
SMIACT#	LOW	
A3–A2	HIGH	Bus Hold, Address Hold and Backoff
HIT#, HITM#	LOW	
CACHE#	LOW	Bus Hold, Backoff
UP#	LOW	

2.3.3 INPUT PINS

Table 2-4 lists all input pins, indicating their active level, and whether they are synchronous or asynchronous inputs.

Table 2-4. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
CLK				
RESET	HIGH	Asynchronous		
HOLD	HIGH	Synchronous		
AHOLD	HIGH	Synchronous	PULLDOWN	
EADS#	LOW	Synchronous	PULLUP	
BOFF#	LOW	Synchronous	PULLUP	
FLUSH#	LOW	Asynchronous	PULLUP	
A20M#	LOW	Asynchronous	PULLUP	
BS16#, BS8#	LOW	Synchronous	PULLUP	
KEN#	LOW	Synchronous	PULLUP	
RDY#	LOW	Synchronous		
BRDY#	LOW	Synchronous	PULLUP	
INTR	HIGH	Asynchronous		
NMI	HIGH	Asynchronous		
IGNNE#	LOW	Asynchronous	PULLUP	
BLEN#	LOW	Tie High or Low	PULLUP	
EWBE#	LOW	Synchronous	PULLDOWN	BRDY#/RDY#
INIT	HIGH	Asynchronous	PULLDOWN	
INV	HIGH	Synchronous	PULLUP	EADS#
STPCLK#	LOW	Asynchronous	PULLUP	
SMI#	LOW	Asynchronous	PULLUP	
WB/WT#	BOTH	Synchronous	PULLDOWN	FIRST RDY#/RDY#

2.3.4 INPUT/OUTPUT PINS

Table 2-5 lists all the input/output pins, indicating their active level, and when they are floated.

Table 2-5. Input/Output Pins

Name	Active Level	When Floated
D31–D0	HIGH	Bus Hold, Backoff
DP3–DP0	HIGH	Bus Hold, Backoff
A31–A4	HIGH	Bus, Address Hold, Backoff

3.0 CACHE FUNCTIONALITY

3.1 Cache Introduction

Special hooks are provided to support the Pentium OverDrive processor on-chip write back cache and to maintain cache consistency. The external environment can dynamically change the caching policy of the Pentium OverDrive processor on a line by line basis.

The Pentium OverDrive processor has separate code and data caches. Each of the caches are 16 Kbytes in size and each is organized as a 4-way set associative cache. The data cache follows the MESI cache consistency protocol while the code cache follows a subset of that protocol. For a complete description of the cache see the *Intel486 Microprocessor Family Data Book*(2).

NOTE:

2. A generic discussion on the operation of cache memories can be found in the Intel Cache Tutorial available from your Intel sales representative or from Intel's Literature department, order #296543-002.

3.2 Cache Organization

The Pentium OverDrive processor includes separate code and data caches on chip to meet its performance goals. The code and data caches can be accessed simultaneously. The code cache can provide up to 16 bytes of raw opcodes and the data cache can provide data for two data references all in the same clock. Each of the caches are accessed with physical addresses and each cache has its own TLB (translation look aside buffer) to translate linear addresses to physical addresses. A cache consistency protocol called the **MESI** protocol is implemented in the data cache to ensure data consistency in a multiprocessor environment.

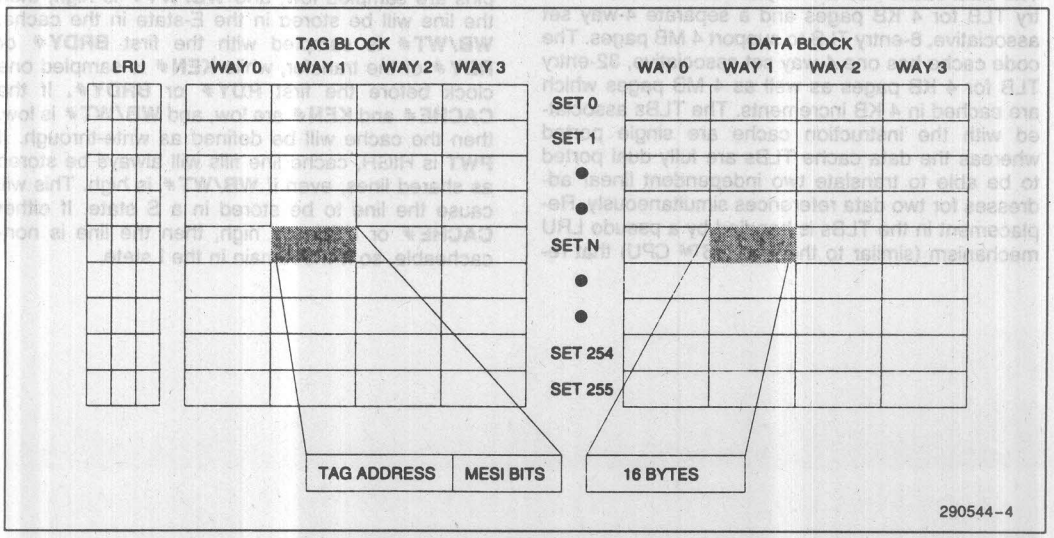


Figure 3-1. Conceptual Organization of Data Cache

Each of the caches are 16 Kbytes in size and each is organized as a 4-way set associative cache. There are 256 sets in each cache, each set containing 4 lines. Each cache line is 16 bytes wide. Replacement in both the data and instruction caches is handled by a pseudo LRU mechanism which requires three bits per set in each of the caches. A conceptual diagram of the organization of the data cache is shown below in Figure 3-1.

The data cache can support two data references simultaneously in one clock, one from each of the two pipelines. It is a write back cache with full support for data consistency in a multimaster environment. This is implemented with two status bits associated with each cache line. The data cache can optionally be configured in write through mode on a line by line basis when in write back cache mode. The storage array in the data cache is single ported but interleaved on 4 byte boundaries to be able to provide data for two simultaneous accesses to the same cache line. The tags in the data cache are triple ported. One of the ports is dedicated to snooping while the other two are used to lookup two independent addresses corresponding to data references from each of the pipelines. The code cache tags are also triple ported. Again, one port is dedicated to support snooping and other two ports facilitate split line accesses (simultaneously accessing upper half of one line and lower half of the next line).

The data cache has a 4-way set associative, 64-entry TLB for 4 KB pages and a separate 4-way set associative, 8-entry TLB to support 4 MB pages. The code cache has one 4-way set associative, 32-entry TLB for 4 KB pages as well as 4 MB pages which are cached in 4 KB increments. The TLBs associated with the instruction cache are single ported whereas the data cache TLBs are fully dual ported to be able to translate two independent linear addresses for two data references simultaneously. Replacement in the TLBs is handled by a pseudo LRU mechanism (similar to the Intel486™ CPU) that requires 3 bits per set. The tag and data arrays of the TLBs are parity protected with a parity bit associated with each of the tag and data entries in the TLBs.

3.3 State Transition Tables

Lines cached in the Pentium OverDrive processor can change state because of Pentium OverDrive processor generated activity or as a result of activity on the Pentium OverDrive processor bus generated by other bus masters (snooping). As shown in the following tables, state transitions occur because of Pentium OverDrive processor generated transactions (memory reads/writes) and snooping by the external system. This protocol has minor differences from the MES1 protocol of the Write-Back Enhanced IntelDX2 processor as detailed in Section 10.2.

3.3.1 READ CYCLE

The state transitions for the data cache during reads are shown in Table 3-1. For a cache line that is in the M (Modified), E (Exclusive) or S (Shared) states, the data is transferred from the cache to the core, with no bus cycle generated.

Three different cases can occur when a cache read occurs for an I-state (Invalid) line. An access to an invalid line indicates a miss in the cache, so a read cycle will be generated. If the **CACHE#** and **KEN#** pins are sampled low, and **WB/WT#** is high, then the line will be stored in the E-state in the cache. **WB/WT#** is sampled with the first **BRDY#** or **RDY#** of the transfer, while **KEN#** is sampled one clock before the first **RDY#** or **BRDY#.** If the **CACHE#** and **KEN#** are low, and **WB/WT#** is low, then the cache will be defined as write-through. If **PWT** is HIGH, cache line fills will always be stored as shared lines, even if **WB/WT#** is high. This will cause the line to be stored in a S state. If either **CACHE#** or **KEN#** is high, then the line is non-cacheable, so it will remain in the I state.

Table 3-1. Data Cache State Transitions for Pentium® OverDrive® Processor Initiated Unlocked Read Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Read hit; data is provided to the Pentium OverDrive processor core by cache. No bus cycle is generated.
E	n/a	E	Read hit; data is provided to the Pentium OverDrive processor core by cache. No bus cycle is generated.
S	n/a	S	Read hit; Data is provided to the Pentium OverDrive processor by the cache. No bus cycle is generated.
I	**CACHE#** low AND **KEN#** low AND **WB/WT#** high AND **PWT** low	E	Data item does not exist in cache (MISS). A bus cycle (read) will be generated by the Pentium OverDrive processor. This state transition will happen if **WB/WT#** is sampled high with first **BRDY#** or **RDY#**.
I	**CACHE#** low AND **KEN#** low AND (**WB/WT#** low OR **PWT** high)	S	Same as previous read miss case except that **WB/WT#** is sampled low with first **BRDY#** or **RDY#**. If **PWT** is high, **WB/WT#** is ignored and the resulting line state is always "S".
I	**CACHE#** high OR **KEN#** high	I	**KEN#** pin inactive; the line is not intended to be cached in the Pentium OverDrive processor.

NOTE:
The transition from I to E or S-states (based on **WB/WT#**) happens only if the line is cacheable. If **KEN#** is sampled high, the line is not cached and remains in the I-state.

3.3.2 WRITE CYCLE

The state transitions of data cache lines during Pentium OverDrive processor generated write cycles are illustrated in Table 3-2. Writes to SHARED lines in the data cache are always sent out on the bus along with updating the cache with the write item. The status of the **PWT** and **WB/WT#** pins during these write cycles on the bus determines the state transitions in the data cache during writes to S-state lines.

A write to a SHARED line in the data cache will generate a write cycle on the Pentium OverDrive processor bus to update memory and/or invalidate the contents of other caches. If the **PWT** pin is driven high when the write cycle is run on the bus, the line will be updated, and will stay in the S- state regardless of the status of the **WB/WT#** pin that is sampled with the first **BRDY#** or **RDY#**. If **PWT** is driven low, the status of the **WB/WT#** pin sampled along with the first **BRDY#** or **RDY#** for the write cycle determines what state (E or S) the line transitions to.

The state transition from S to E is the only transition in which the data and the status bits are not updated at the same time. The data will be updated when the cycle is written to the Pentium OverDrive processor write buffers. The state transition does not occur until the write has completed on the bus (last **BRDY#** or **RDY#** has been returned). Writes to the line after the transition to the E-state will not generate bus cycles. However, it is possible that writes to the same line that were buffered before the transition to the E-state will generate bus cycles after the transition to E-state.

An inactive **EWBE#** input will stall subsequent writes to an E- or an M- state line until **EWBE#** is returned active.

Table 3-2. Data Cache State Transitions for Pentium® OverDrive® Processor Initiated Write Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Write hit; update data cache. No bus cycle generated to update memory.
E	n/a	M	Write hit; update cache only. No bus cycle generated; line is now MODIFIED.
S	**PWT** low AND **WB/WT#** high	E	Write hit; data cache updated with write data item. A write through cycle is generated on bus to update memory and/or invalidate contents of other caches. All subsequent writes to E- or M-state lines are held off until completion of write cycle is known and state transition happens.
S	**PWT** low AND **WB/WT#** low	S	Same as above case of write to S-state line except that **WB/WT#** is sampled low.
S	**PWT** high	S	Same as above cases of writes to S-state lines except that this is a write hit to a line in a write-through page; status of **WB/WT#** pin is ignored.
I	n/a	I	Write MISS; a write through cycle is generated on the bus to update external memory. No allocation is done.

NOTE:
Memory writes are buffered while I/O writes are not. There is no guarantee of synchronization between completion of memory writes on the bus and instruction execution after the write.

3.3.3 INQUIRE CYCLES (SNOOPING)

The purpose of inquire cycles is to check whether the address being presented is contained within the caches in the Pentium OverDrive processor. Inquire cycles may be initiated with or without an invalidation request (**INV** = 1 or 0). The processor samples the snoop address during the clock that **EADS#** is active. An inquire cycle is run through the data and code caches through a dedicated snoop port to determine if the address is contained in one of the Pentium OverDrive processor caches. If the address is in a Pentium OverDrive processor cache, the **HIT#** pin is asserted. If the address hits a modified line in the processor , the **HITM#** pin is also asserted and the modified line is then written back to external memory.

Table 3-3 shows the state transitions for inquire cycles.

3.4 Processor Code Cache Consistency Protocol

The Pentium OverDrive processor code cache follows a subset of the MESI protocol. Access to lines in the code cache are either a Hit (Shared) or a Miss (Invalid). In the case of a read hit, the cycle is serviced internally to the Pentium OverDrive processor and no bus activity is generated. In the case of a read miss, the read is sent to the external bus and may be converted to a line fill.

Lines are never overwritten in the code cache. Writes generated by the Pentium OverDrive processor are snooped by the code cache. If there is a hit, the line is invalidated. If there is a miss, no action is taken by the code cache.

3.5 Warm Reset Cache Behavior

The **INIT** pin can be used to reset the Pentium OverDrive processor without invalidating the on-chip cache. The Pentium OverDrive processor state after **INIT** is the same as the state after **RESET** except that the internal caches, floating point registers, and SMM Base Register retain whatever values they had prior to recognition of **INIT**. The **INIT** signal can be used instead of **RESET** for warm resets when the cache contents need to be maintained. However, **INIT** cannot be used in lieu of **RESET** after power up. For more information on the INIT and the Pentium OverDrive processor, please see Section 5.

Table 3-3. Cache State Transitions during Inquire Cycles

Present State	Next State INV = 1	Next State INV = 0	Description
M	I	S	Snoop hit to a MODIFIED line indicated by **HIT#** and **HITM#** pins low. Pentium OverDrive processor schedules the writing back of the modified line to memory.
E	I	S	Snoop hit indicated by **HIT#** pin low; no bus cycle generated.
S	I	S	Snoop hit indicated by **HIT#** pin low; no bus cycle generated.
I	I	I	Address not in cache; **HIT#** pin high.

4.0 HARDWARE DESIGN CONSIDERATIONS

4.1 Introduction

This section describes the organization of the Translation Lookaside Buffers (TLBs), write buffers and the buffering scheme used in the Pentium OverDrive processor. Other important Pentium OverDrive Processor design specific details are also included as well as the use of the **WB/WT#** pin as an input to determine the fundamental cache operation mode of the processor.

4.1.1 CACHE CONSISTENCY CYCLES

The external system can check and invalidate cache lines in the internal processor cache using inquire cycles (snooping). Snooping allows the external system to keep cache coherency throughout the system. Snoop cycles may be performed using **AHOLD**, **BOFF#**, or **HLDA** and then asserting **EADS#** to inform the processor that the snoop address is available on the bus. The following table summarizes the snoop mechanism initiated by any of these three control signals.

The snoop cycle begins by checking whether a particular cache line has been "cached" and invalidates the line based on the state of the **INV** pin. If the Pentium OverDrive processor is configured in the Standard Bus Mode, the processor will always invalidate the cache line on snoop hits. If the processor is configured in the Enhanced Bus Mode, the system must drive **INV** high to invalidate a particular cache line. The Pentium OverDrive processor will invalidate the line and write back an E-state line if the system snoop hits either S-state, E-state, or M-state line, provided **INV** was driven high during **EADS#** assertion. If **INV** is driven low, a modified line will be written back to memory and will remain in the cache as a write-back line. If **INV** is driven low, a shared line also will continue to remain in the cache as a shared line.

After asserting **AHOLD** or **BOFF#**, the external master driving a snoop cycle must wait at least two clocks before asserting **EADS#**. If snooping is done after **HLDA** assertion, then the master performing a snoop must wait for at least one clock cycle before driving the snoop addresses and asserting **EADS#**. **INV** should be driven low during bus master read operations to minimize invalidations. **INV** should be driven high to invalidate a cache line during bus master write operations. The Pentium OverDrive processor asserts **HIT#** and **HITM#** if the cycle hits an M state line in the cache or **HIT#** only if the cycle

Table 4-1. Snoop Cycles under AHOLD, BOFF#, or HLDA

AHOLD	Tri-states the address bus. **ADS#** will be asserted under **AHOLD** only to initiate a snoop writeback cycle. An ongoing burst cycle will complete under an **AHOLD.** For non-burst cycles, a specific non-burst transfer (**ADS#-RDY#** transfer) will complete under **AHOLD** and will be fractured (interrupted) before the next assertion of **ADS#**. A snoop writeback cycle will be reordered ahead of a fractured non-burst cycle. Should an **ADS#** be required to start the next cycle while **AHOLD** is asserted, the processor will only perform snoop write back cycles. If the processor issues and **ADS#** while **AHOLD** is asserted, it is the responsibility of the system to determine the address of the snoop write back from the snoop address driven with **EADS#**. An interrupted non-burst cycle will be completed only after the snoop writeback cycle is completed, provided there are no other snoop writeback cycles scheduled and **AHOLD** is deasserted. If **BLEN#** is driven inactive (disabling bursted writes), the processor will drive four individual **ADS#-RDY#** cycles to complete the cycle while **AHOLD** is active.
BOFF#	Overrides **AHOLD;** takes effect in the next clock. Ongoing bus cycles will stop in the clock following **BOFF#** being asserted and resumes when **BOFF#** is deasserted, in the same manner as the standard Intel486 processor bus. A snoop writeback will be reordered ahead of the backed off cycle. The snoop writeback cycle begins after **BOFF#** is deasserted followed by any backed off cycle.
HOLD	**HOLD** will be acknowledged only between bus cycles, except for a non-cacheable, non-bursted code prefetch cycle. In a non-cacheable, non-bursted code prefetch cycle, **HOLD** is acknowledged after the system returns **RDY#** or if **BOFF#** is asserted. Once **HLDA** is active, the processor blocks all bus activities until the system releases the bus (by de-asserting **HOLD**).

hits an E or S state line. These output signals become valid two clock periods after **EADS#** is valid on the bus. **HITM#** will remain asserted at least until the last **RDY#** or **BRDY#** of the snoop writeback cycle is returned. The **HIT#** signal will continue to drive the result of the last snoop until the next external snoop occurs. Most timing diagrams in the following sections do not include the **HIT#** signal since it is not necessary for single processor system designs. Snoop operations may interrupt an ongoing bus operation in both the Standard Bus Mode and Enhanced Bus Mode.

The Pentium OverDrive processor can accept EADS# in every clock period while in the Standard Bus Mode. In the Enhanced Bus Mode, the processor can accept EADS# every other clock period until the external snoop hits an M-state line. Any **EADS#** assertion after the **EADS#** that hit a modified line will be ignored. The processor will not accept any further **EADS#** assertions until the snoop writeback operation is completed and **HITM#** is deasserted. Figure 4-1 shows the allowable **EADS#** window for the different snooping mechanisms (**AHOLD, HOLD, BOFF#**). **For the Enhanced bus mode, EADS# must not be asserted outside the windows presented in the diagrams below.**

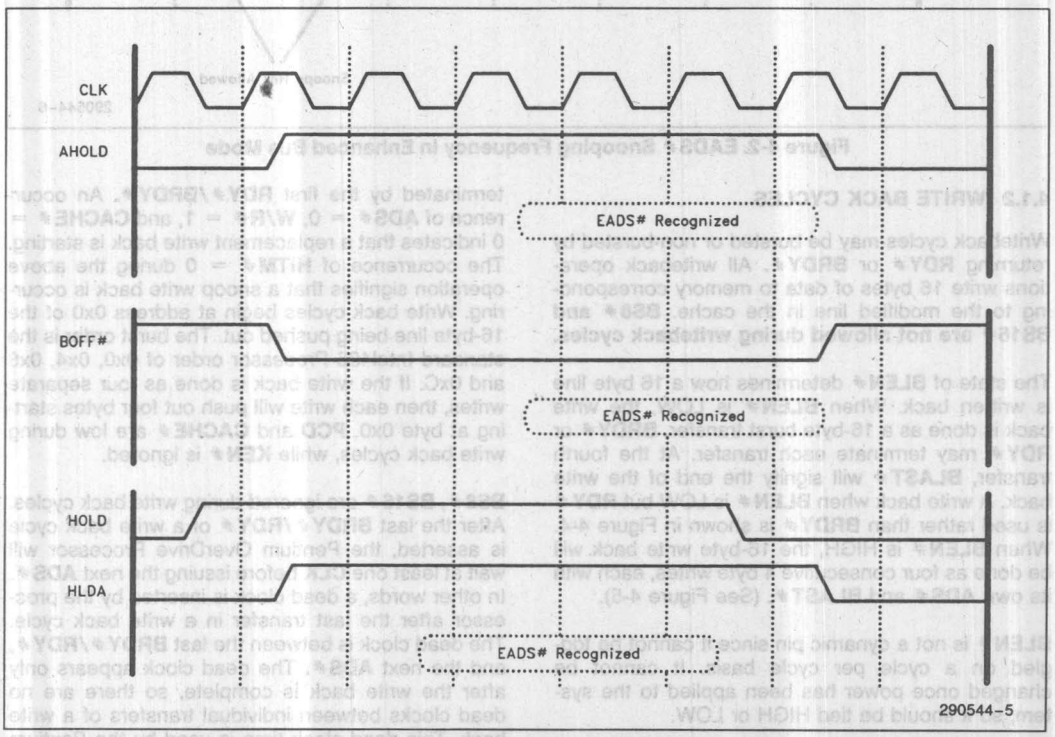


Figure 4-1. EADS# Snooping Window

Figure 4-2 shows that the processor can accept an **EADS#** assertion only every other clock while in enhanced bus mode.

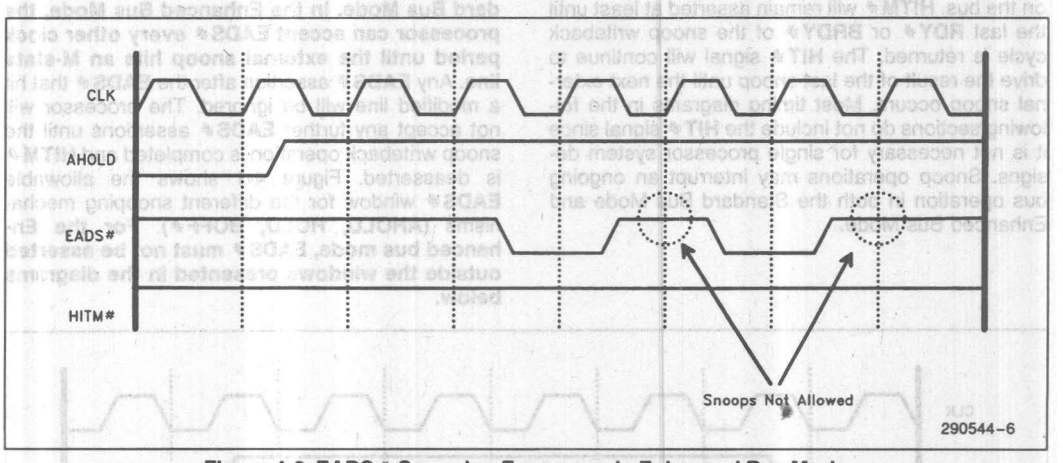


Figure 4-2. EADS# Snooping Frequency in Enhanced Bus Mode

4.1.2 WRITE BACK CYCLES

Writeback cycles may be bursted or non-bursted by returning **RDY#** or **BRDY#**. All writeback operations write 16 bytes of data to memory corresponding to the modified line in the cache. **BS8# and BS16# are not allowed during writeback cycles.**

The state of **BLEN#** determines how a 16 byte line is written back. When **BLEN#** is LOW, the write back is done as a 16-byte burst transfer. **BRDY#** or **RDY#** may terminate each transfer. At the fourth transfer, **BLAST#** will signify the end of the write back. A write back when **BLEN#** is LOW but **RDY#** is used rather than **BRDY#** is shown in Figure 4-4. When **BLEN#** is HIGH, the 16-byte write back will be done as four consecutive 4 byte writes, each with its own **ADS#** and **BLAST#**. (See Figure 4-5).

BLEN# is not a dynamic pin since it cannot be toggled on a cycle per cycle basis. It cannot be changed once power has been applied to the system, so it should be tied HIGH or LOW.

The **CACHE#** pin is used to indicate that a cache operation is taking place. **CACHE#** is active with the first **ADS#** for both write backs and line fills, and is terminated by the first **RDY#/BRDY#**. An occurrence of **ADS#** = 0, **W/R#** = 1, and **CACHE#** = 0 indicates that a replacement write back is starting. The occurrence of **HITM#** = 0 during the above operation signifies that a snoop write back is occurring. Write back cycles begin at address 0x0 of the 16-byte line being pushed out. The burst order is the standard Intel486 Processor order of 0x0, 0x4, 0x8 and 0xC. If the write back is done as four separate writes, then each write will push out four bytes starting at byte 0x0. **PCD** and **CACHE#** are low during write back cycles, while **KEN#** is ignored.

BS8#, BS16# are ignored during write back cycles. After the last **BRDY#/RDY#** of a write back cycle is asserted, the Pentium OverDrive Processor will wait at least one **CLK** before issuing the next **ADS#**. In other words, a dead clock is inserted by the processor after the last transfer in a write back cycle. The dead clock is between the last **BRDY#/RDY#**, and the next **ADS#**. The dead clock appears only after the write back is complete, so there are no dead clocks between individual transfers of a write back. This dead clock time is used by the Pentium OverDrive processor to complete internal cache operations.

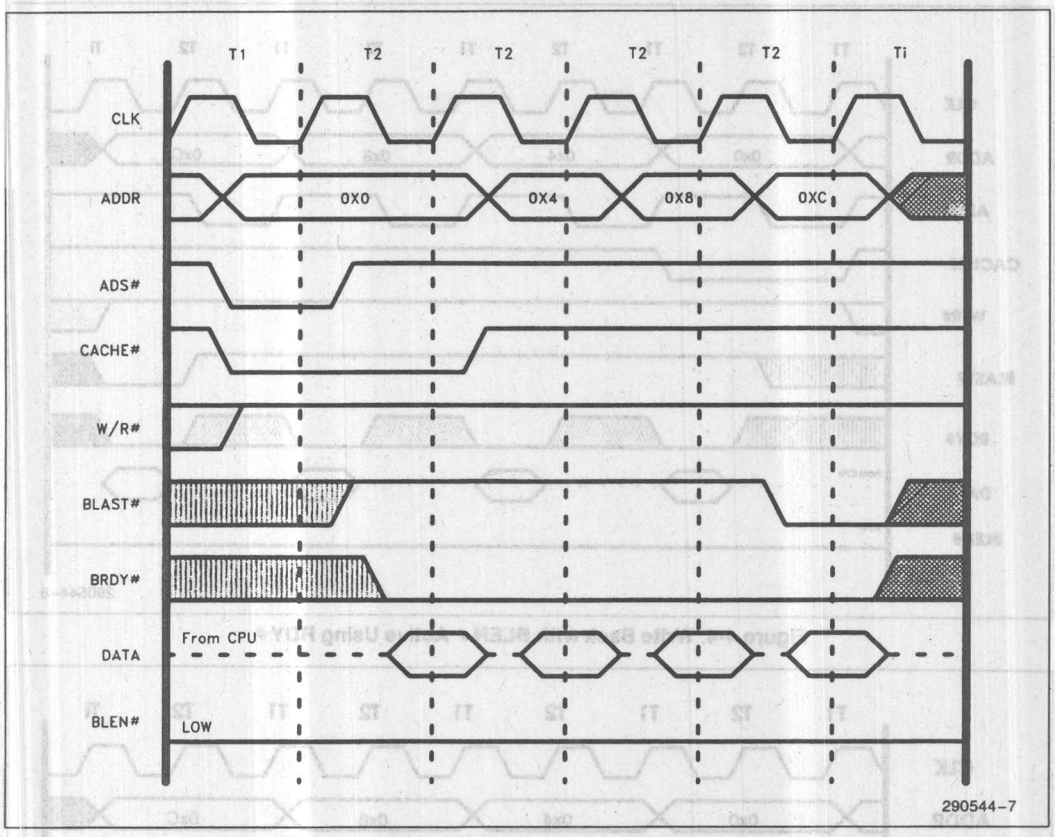


Figure 4-3. Write Back Operation—BLEN# Active

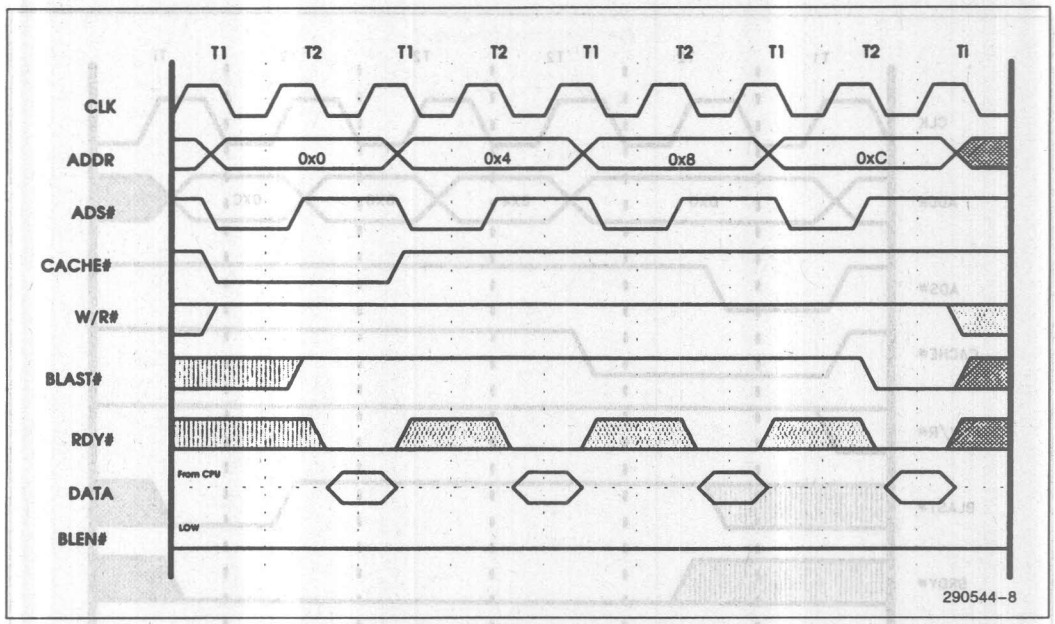


Figure 4-4. Write Back with BLEN# Active Using RDY#

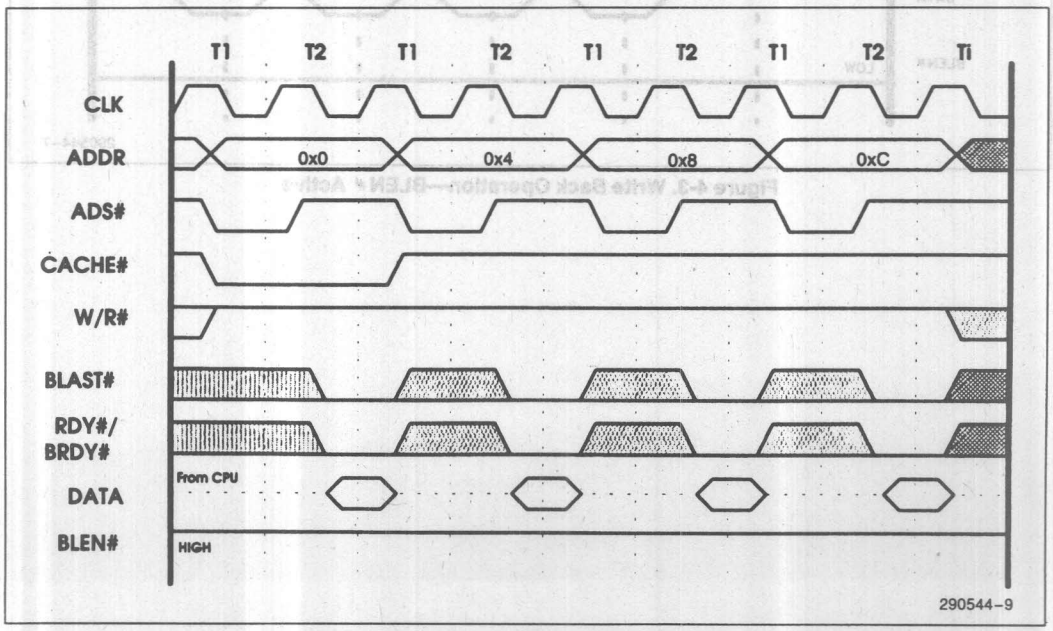


Figure 4-5. Write Back as Four 4-Byte Transfers (BLEN# Inactive)

4.2 WB/WT# As an Initialization Input

To make the Pentium OverDrive processor more compatible with the IntelDX2 processor, several small enhancements have been added to the processor to help distinguish different processor modes of operation. These two modes will be referred to as **"standard bus mode" (Write through processor cache only)** and "enhanced bus mode" (Write back processor enabled and are discussed in the following paragraphs.

In order to allow the Pentium OverDrive processor to operate in more of an IntelDX2 processor manner, the **WB/WT#** pin is used as an initialization input to configure the operating mode of the processor. At the falling edge of **RESET,** the processor can be configured to operate in a write through only (IntelDX2 CPU compatible) L1 cache mode (**standard bus** mode), or in a write back L1 cache mode (enhanced bus mode). Once a mode is selected, the processor will continue to operate in the selected mode and can only be changed to a different mode by starting the **RESET** process again. Assertion of **INIT** will not change the operating mode of the processor. **WB/WT#** has an internal pulldown that will force any design that leaves **WB/WT#** unconnected into the write through mode of operation. Table 4-2 lists the two modes of operation and the differences between them.

For more information on the effect of the mode operation on the various signals mentioned above, please see the *Intel486 Microprocessor Family Data Book*. Unless otherwise mentioned, all other functions of the Pentium OverDrive processor remain identical in both operating modes.

4.3 INIT Functionality

INIT behaves like an edge triggered interrupt on the Pentium OverDrive processor while in both enhanced bus mode (**WB/WT#** = HIGH at **RESET**) and standard bus mode (**WB/WT#** = LOW at **RESET**). Therefore, when **INIT** is asserted, there is a high probability that one or more bus cycles will be run by the processor while **INIT** is HIGH. The following figures demonstrate two scenarios of how the processor can issue an **ADS#** while **INIT** is asserted. Although the figures assume that an initial I/O write causes the **INIT** to be asserted by the support logic, these cases apply whenever **INIT** is HIGH. The first figure describes cycles being run by the processor before **INIT** is recognized. The second details cycles being run after **INIT** has been recognized.

Figure 4-6 shows the **INIT** signal being triggered by an I/O write. Even though **INIT** is asserted immediately, there is a pending prefetch which executes before the **INIT** is recognized.

Table 4-2. Effects of WB/WT# Initialization

State of WB/WT# at Reset Falling	Affect on Processor Operation
WB/WT# = LOW	Processor is in **Standard Bus** Mode ** IntelDX2 Processor Compatible ** 1: No Special **FLUSH#** Acknowledge Cycles are run on the bus after the assertion of the FLUSH# pin. 2: When **FLUSH#** is asserted, the caches will be invalidated in 15–20 system **CLKs**. 3: All Write Back specific inputs are ignored—(**BLEN#, EWBE#, WB/WT#, INV**) 4: **EADS#** is sampled at any time.
WB/WT# = HIGH	Processor is in **Enhanced Bus** Mode ** Intel486 Processor Write Back Bus Operation ** 1: The special **FLUSH#** Acknowledge Cycles will be run on the bus after the assertion of the **FLUSH#** and all the cache write backs (if any) are complete. 2: Write backs will be performed if a cache flush is requested (i.e.: **FLUSH#, WBINVD** inst . . .). The flush will take about 2000+ clocks. The system must watch for the FLUSH# special cycles to determine the end of the flush. 3: **WB/WT#** is sampled on a line by line basis to determine the storage state of a cache line on reads and writes. 4: The **BLEN#, EWBE#** and **INV** are no longer ignored. 5: **EADS#** is sampled only when the processor is an a **HOLD, AHOLD,** or **BOFF#** state. 6: **PLOCK#** is inactive and driven HIGH.

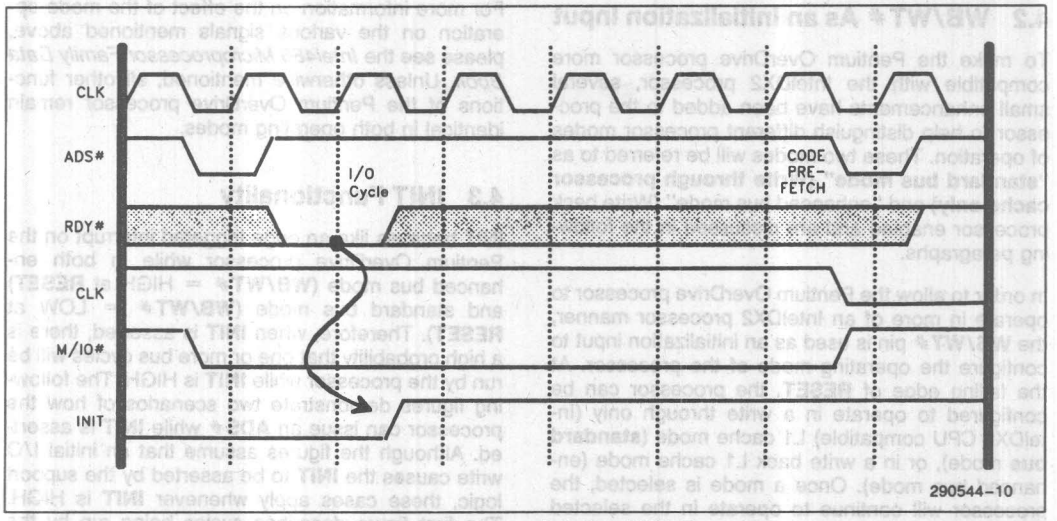


Figure 4-6. ADS# Issued during INIT: Case 1

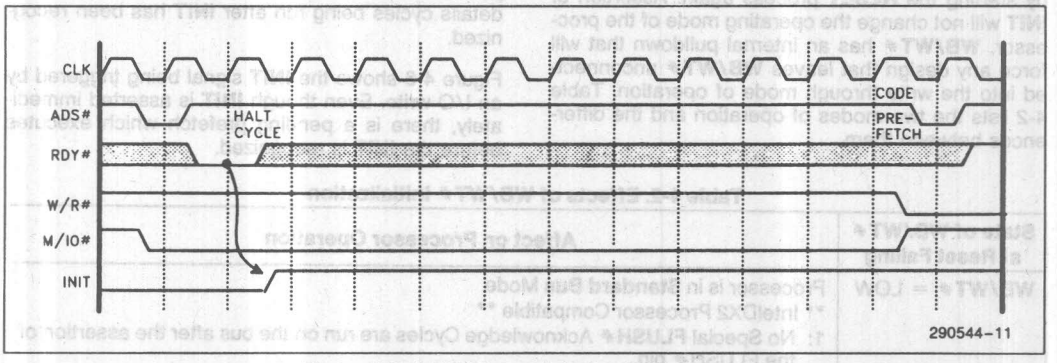


Figure 4-7. ADS# Issued during INIT: Case 2

Figure 4-7 assumes that an I/O cycle was used to generate the **INIT**, but the system waited until all bus activity had stopped (by monitoring the HALT special cycle) before asserting the **INIT** pin. In this case, the processor recognizes **INIT**, and starts a prefetch before **INIT** is deasserted. The prefetch may be from any location, and not necessarily the F..F0h address, even though **INIT** has been recognized.

On other Intel486 write through cache processors (Write-Back Enhanced IntelDX2 in standard bus mode and SL-Enhanced CPUs), the **SRESET** pin is executed immediately, in a manner similar to the **RESET** pin. This means that no cycles will be run after **SRESET** is asserted on these processors. With the Pentium OverDrive processor, it is the responsibility of the system to ensure that any cycles that are issued while INIT is active are completed properly to prevent data corruption, lost bus cycles or system lock-ups.

4.4 Instruction Prefetch

The Pentium OverDrive processor contains a prefetch buffer of several bytes, and can prefetch a significant number of bytes beyond the end of the last executed instruction. In addition, the processor implements a dynamic branch prediction algorithm which speculatively runs code fetch cycles to addresses corresponding to instructions executed some time in the past. Such code fetch cycles are run based on past execution history, regardless of whether the instructions retrieved are relevant to the currently executing instruction sequence.

The effect of both mechanisms is that the Pentium OverDrive processor may run code fetch bus cycles to retrieve instructions which are never executed. Although the opcodes retrieved are discarded, the system must complete the code fetch bus cycle by returning **RDY#/BRDY#**. It is particularly important that the system return **RDY#/BRDY#** for all code fetch cycles, regardless of the address.

Furthermore, it is possible that the processor may run speculative code fetch cycles to addresses beyond the end of the current code segment. Although the processor may prefetch beyond the CS limit, it will not attempt to execute beyond the CS limit, it will raise a GP fault instead. Thus, segmentation cannot be used to prevent speculative code fetches to inaccessible areas of memory. On the other hand, the processor will never run code fetch cycles to inaccessible pages, so the paging mechanism guards against both the fetch and execution of instructions in inaccessible pages.

If the processor has been placed in a halt state with the **HLT** instruction, and the processor has issued the halt cycle, or the processor has run a shutdown cycle, one of the methods of exiting this condition is to assert an interrupt. Once the interrupt is asserted, the Pentium OverDrive processor may issue a prefetch before the interrupt is acknowledged with an interrupt cycle, or the action desired by the interrupt is performed. For example, if the processor is in a halt state, and the **FLUSH#** interrupt is asserted, the processor could exit the halt state, perform a prefetch, and then start driving the write backs for the flush operation. Prefetches of this type may be run after any interrupt, including **INTR.**

For memory reads and writes, both segmentation and paging prevent the generation of bus cycles to inaccessible regions of memory.

5.0 SOFTWARE CONSIDERATIONS

5.1 External Bus Cycle Ordering

5.1.1 WRITE BUFFERS AND MEMORY ORDERING

The Pentium OverDrive processor has write buffers to enhance the performance of consecutive writes to memory. Writes in these buffers are driven out on the external bus in the order they were generated by the processor core. No reads (as a result of cache miss) are reordered around previously generated writes sitting in the write buffers (Unlike the IntelDX2 processor). The implication of this is that the write buffers will be emptied before a subsequent processor generated bus cycle is run on the external bus.

It should be noted that only memory writes are buffered and I/O writes are not. There is no guarantee of synchronization between completion of memory writes on the bus and instruction execution after the write. The OUT instruction or a serializing instruction needs to be executed to synchronize writes with the next instruction. Please refer to the *Pentium Processor Programmers Reference Manual* for information on serializing instructions.

No re-ordering of read cycles occurs on the Pentium OverDrive processor. Specifically, the write buffers are emptied before the IN instruction is executed.

5.1.2 EXTERNAL EVENT SYNCHRONIZATION

When the value of **NMI, INTR, FLUSH#, SMI#** or **INIT** changes as the result of executing an OUT instruction, these inputs must be at a valid state three clocks before **RDY#/BRDY#** is returned to ensure that the new value will be recognized before the next instruction is executed.

Note that if an OUT instruction is used to modify **A20M#**, this will not affect previously prefetched instructions. A serializing instruction must be executed to guarantee recognition of **A20M#** before a specific instruction.

5.2 Model Specific Registers

The Pentium OverDrive processor defines certain Model Specific Registers that are used in execution tracing, performance monitoring and testing. They are unique to the Pentium OverDrive processor and may or may not be implemented in the same way in future processors.

Please contact Intel for more information on the model specific registers.

5.3 Exception Priorities

Exceptions are serviced and recognized on the boundary between instructions. The instruction pointer pushed onto the stack for the interrupt handler points to the next instruction. The priority among simultaneous exceptions is as follows (interrupt vector numbers are shown in decimal in parentheses):

Trap on the previous instruction:

- Breakpoint (#3)

External Interrupts:

- **FLUSH#**
- **SMI#**
- **INIT**
- **NMI**
- **INTR**

Floating Point Errors:

- **FERR#**

External Interrupt:

- **STPCLK#**

Faults on Fetching Next Instruction:

- Code Seg Limit Violation (#13), Page Fault on prefetch (#14) (the relative priority unpredictable)

Faults in Decoding the next Instruction:

- Invalid Opcode (#6), Device Not Available (#7)
- General Protection Fault for Instruction Length > 15B (#13)

Faults on Executing an Instruction (These may occur in a manner that varies from implementation to implementation as necessary to insure functional correctness. They are not listed in any particular order):

- General Detect (#1)
- FP Error (from previous FP instruction) (#16)
- Interrupt on Overflow (#4)
- Bound (#5)
- Invalid TSS (#10)
- Segment Not Present (#11)
- Stack Exception (#12)
- General Protection (#13)
- Data Page Fault (#14)
- Alignment Check (#17)

5.3.1 EXTERNAL INTERRUPT CONSIDERATIONS

The Pentium OverDrive processor recognizes the following external interrupts: **FLUSH#, SMI#, INIT, NMI, INTR** and **STPCLK#.** They are listed in priority order, however, they are subject to the considerations listed below.

FLUSH#

Note that unlike the Intel486 CPU which invalidates its cache a small fixed number of clocks after **FLUSH#** is asserted, the **FLUSH#** pin on the Pentium OverDrive processor is an interrupt and therefore is only recognized at the boundary between instructions. While **FLUSH#** is being serviced, all the dirty lines in the data cache are written back to main memory. This may take several thousand clocks. During this time no instructions are executed and no other interrupts are recognized. If the processor is in the HALT or Shutdown state, **FLUSH#** is still recognized. The processor will return to the HALT or Shutdown state after servicing the **FLUSH#.**

5.4 BIOS and Software

The following should be considered when designing a Pentium OverDrive processor based system.

5.4.1 Pentium® OverDrive® PROCESSOR DETECTION

The component identifier and stepping/revision identifier for the Pentium OverDrive processor is readable in the DX register immediately after RESET, where

DX = 153xh

The x can be any value from 0 to Fh and refers to the stepping of the part.

As with the IntelDX2 microprocessor specification, it is recommended that the BIOS save the contents of the DX register, immediately after RESET, so that this information can be used later, if required.

Software can also find out the component identifier and stepping/revision by invoking the CPUID instruction.

5.4.2 BIOS BOOT CODE ASSUMPTIONS

In preliminary tests with systems that support the Pentium OverDrive processor, it was found that the aggressive prefetch unit of the processor would attempt to fetch from the x0 . . . 00h address after a **RESET.** Since this address exists in real memory and the BIOS had not been able to properly initialize it before this point, parity errors would be detected by the system.

To avoid issue, the Pentium OverDrive processor prefetch unit is disabled any time the processor is restarted with **RESET** to prevent the prefetcher from attempting to fetch code from address x0..00h after wrapping around from xF..FFh. In the sixteen bytes from xF..F0h to xF..FFh, there must be at least one jump instruction (of any type) that transfers code execution out of the xF..F0h to xF..FFh region. If not, the Pentium OverDrive processor will not enable the prefetch unit, and processor operation will stop.

INIT does not place this restriction on the prefetcher since it is assumed that parity will have been initialized in the main memory before **INIT** is executed.

5.4.3 TIMING DEPENDENT LOOPS AND BIOS

The Pentium OverDrive processor executes instructions at a frequency which is a multiple of the bus frequency. The Pentium OverDrive processor also uses advanced design techniques to decrease the number of clocks per instruction (CPI) from that of the Intel486 processors. Thus, software such as instruction based timing loops will execute faster on the Pentium OverDrive processor than on the Intel486 processors at the same bus frequency. Instructions such as NOP, LOOP, and JMP $+2, are frequently used by BIOS to implement timing loops, that are required, for example, to enforce recovery time between consecutive accesses for I/O devices. These instruction based timing loop implementations may require modification to be compatible with the Pentium OverDrive processor.

In order to avoid any incompatibilities, it is recommended that timing loops be implemented in hardware rather than in software. This provides transparency and also does not require any change in BIOS or I/O device drivers in the future when moving to higher processor clock speeds.

As an example, a timing loop may be implemented as follows: The software performs a dummy I/O instruction to an unused I/O port. The hardware for the bus controller logic recognizes this I/O instruction and delays the termination of the I/O cycle to the CPU by keeping **RDY#** or **BRDY#** deasserted for the appropriate amount of time.

5.4.4 TEST REGISTER ACCESS

The IntelDX2 processor has test registers which allow OEM's to test the functionality of different areas of the component. These test registers are accessed on the Intel486 processor family using the "MOV reg, TRx and MOV TRx, reg" instructions. These instructions are not available on the Pentium OverDrive processor. Any attempt to execute them will cause a invalid opcode exception. The Pentium OverDrive processor uses the Model Specific Registers (MSR's) to implement on chip testing. These MSR's are accessed using the RDMSR and WRMSR instructions. BIOS must recognize this fundamental difference between the Pentium OverDrive processor and the IntelDX2 processor and act accordingly.

6.0 DIFFERENCES BETWEEN THE Intel486 FAMILY AND THE Pentium® OverDrive® PROCESSOR

This section covers the differences between the Intel486 family of microprocessors and the Pentium OverDrive processor.

6.1 Software

The Pentium OverDrive processor is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2*, and UNIX*. In addition to being binary compatible with the Intel architecture based processors which preceded the Pentium processor, it can also run programs which have been compiled to utilize Pentium processor instructions. This allows pairing of instructions to take advantage of the Superscalar Architecture and adds floating point instructions if replacing an Intel486 SX or IntelSX2 processor.

6.2 Hardware

The Pentium OverDrive processor is in a 237-Pin Grid Array package while the Intel486 family uses a 168-Pin Grid Array package. These extra pins are used for extra power and ground pins, including separate power and ground for the fan heatsink, also the internal cache write-back signals are on these pins.

7.0 DIFFERENCES BETWEEN THE Pentium® PROCESSOR AND THE Pentium® OverDrive® PROCESSOR

There are several differences between the Pentium processor and the Pentium OverDrive processors. These differences are covered in the next two sections.

7.1 Software

The following paragraphs are provided as a reference for software differences between the Pentium OverDrive processor and the Pentium processor. Unless otherwise stated, it can be assumed that the Pentium OverDrive processor will have the same software characteristics as the Pentium processor. For more information on the software characteristics of the Pentium Processor, please see the *Pentium Processor Data Book* or *Programmers Reference Manual*.

The Pentium OverDrive processor does not support machine check exception. As a result, CR4.MCE is not useful. It will be forced to a zero by the hardware. However, any attempt by the software to set this bit to 1 will not create a general protection exception.

The Pentium OverDrive processor allows two different page sizes: 4 KB and 4 MB. Please contact Intel for more information on the use of 4 MB pages.

The behavior of INVD, WBINVD and INVPLG instructions are similar to the Pentium processor. If the processor is in **the enhanced bus mode,** the WBINVD instruction will write back all dirty lines first, flush the cache and run two special cycles (the write back special cycle followed by the flush special cycle) on the bus. INVD will flush the cache and run one special cycle (The flush special cycle) on the bus. INVD will not write back the dirty lines, if any. All three instructions are privileged level 0 and should be executed by BIOS or operating system code only.

On the IntelDX2 processor, when paging is disabled, and/or when instructions that are not affected by paging are executed, the **PCD** and **PWT** pins are driven with values from CR3.PCD and CR3.PWT bits, respectively. On the Pentium OverDrive processor, when paging is disabled and/or when instructions that are not affected by paging are executed, the **PWT** pin will be drive LOW and the **PCD** pin will reflect the value of the CR0.CD bit.

When the CPUID instruction is performed with EAX = 1, the Pentium OverDrive processor will return the following values to the EDX register. These bits indicate what the features of the processor are.

The various bit positions have the following meaning:

Table 7-1. Feature Bit Assignment

Bit	Value	Meaning
0	1	FPU: Floating Point Unit On-Chip
1	1	VME: Virtual-8086 Mode Enhancements
2	1	DE: Debugging Extensions
3	1	PSE: Page Size Extension
4	1	TSC: Time Stamp Counter
5	1	MSR: Pentium Processor-Style MSR
6	R	Reserved
7	R	Reserved
8	1	CX8: CMPXCHG8B Instruction
9–31	R	Reserved

A value of "R" means that the corresponding bit is reserved and the software should not depend on its value.

7.2 Hardware

This section covers the hardware differences between the Pentium processor and the Pentium OverDrive processor.

The Pentium processor has a 64-bit data bus while the Pentium OverDrive processor has a 32-bit data bus. This is required in order for the Pentium OverDrive processor to work in an Intel486 architecture based system.

The size of the data bus requires a similar decrease in the internal cache line size. A burst memory access is four bus widths of data this is the length of each line in the cache. For an Intel486 based architecture system that is 16-Bytes, for a Pentium processor based system this is 32-bytes. The internal cache in the Pentium processor is expecting 32-bytes. This would require two burst reads. Therefore the cache line size was reduced to 16-bytes wide.

The cache on the Pentium processor is split into two 8 KByte caches. One is for data and the other is the instruction or code cache. The Pentium OverDrive processor keeps the idea of two separate caches but increases the size to 16 KBytes each.

The Pentium OverDrive processor does not have the JTAG boundry scan capabilities that the Pentium processor has.

The package is different. The Pentium processor is packaged in a 273-Pin Grid Array while the Pentium OverDrive processor uses a 237-Pin Grid Array package.

The Pentium OverDrive processor has the integrated fan heatsink attached. This integrated fan informs the processor if the fan has slowed or stopped. This reduces the internal frequency to 1x multiplier from the previous 2.5x. The part can run indefinitely at the lower frequency without incurring any damage. This allows the Pentium OverDrive processor to continue in the system until a replacement fan can be installed.

8.0 TESTABILITY

8.1 Introduction

This section describes the features which are included in the Pentium OverDrive processor for the purpose of enhancing the testability of the part. The capabilities of the Intel486 processor test hooks are included in the processor, however they are implemented differently. In addition, new test features were added to assure timely testing and production of a system product. All features described here are also present in the Pentium processor.

Internal component testing through the Built In Self Test (BIST) feature of the Pentium OverDrive processor provides 100% single stuck at fault coverage of the microcode ROM and large PLAs. Some testing of the instruction cache, data cache, Translation Lookaside Buffers (TLBs), and Branch Target Buffer (BTB) is also performed. In addition, the constant ROMs are checked.

The production version of the Pentium OverDrive processor will not include the boundary scan or testability pins.

Several test registers are also included in the Pentium OverDrive processor to simplify access to all on-chip caches and TLBs. These test registers on the processor are not compatible with the definitions for

Table 8-1. Pentium® OverDrive® Processor RESET Modes

RESET	INIT	Type of Reset	Effect on I/D Caches	Effect on FP Registers	Effect on SMM Base Register
0	0	None	Not Applicable	Not Applicable	Not Applicable
0	1	Warm Reset	None	None	None
1	X	Cold Reset (w/ BIST)	Invalidated	Initialized	Invalidated
1	X	Cold Reset (w/o BIST)	Invalidated	Undefined	Invalidated

the test registers on the IntelDX2 processor, and will be provided by Intel at a later date. For the latest information on these test registers, please contact Intel.

The following list summarizes the Pentium OverDrive processor testability features:

- Built In Self Test
- Cache and TLB Test Registers
- Tristate Test Mode

8.2 Pentium® OverDrive® Processor Reset Pins/BIST Initiation

Two pins, **RESET** and **INIT**, are used to reset the Pentium OverDrive processor in different manners. The following table shows the different types of resets that can be initiated using these pins.

Toggling either the **RESET** pin or the **INIT** pin individually forces the Pentium OverDrive processor to begin execution at address 0FFFFFFF0h. The internal instruction cache and data cache are invalidated when **RESET** is asserted (modified lines in the data cache are NOT written back). The instruction cache and data cache are not altered when the INIT pin is asserted without **RESET.** In neither case are the floating point registers altered. In both cases, the BTB, the segment descriptor cache and both TLBs are all invalidated.

Reset with self test is initiated by holding the **AHOLD** pin HIGH for 2 clocks before and 2 clocks after **RESET** is driven from HIGH to LOW. The instruction cache and data cache are invalidated and the floating point registers are initialized. The processor begins execution at address 0xFFFFFFF0h. The BTB, the segment descriptor cache and both TLBs are all invalidated before execution begins.

At the conclusion of reset, with or without self test, the DX register will contain a component identifier. The upper byte will contain 15h and the lower byte will contain a stepping identifier.

Table 8-2 defines the processor state after **RESET, INIT** and **RESET** with BIST (built in self test).

Table 8-2. Register State after RESET, INIT and BIST
(Register States are given in Hexadecimal Format)

Storage Element	RESET (no BIST)	RESET (BIST)	INIT
EAX	0	0 if pass	0
EDX	1530 + stepping	1530 + stepping	1530 + stepping
ECX, EBX, ESP EBP, ESI, EDI	0	0	0
EFLAGS	2	2	2
EIP	0FFF0	0FFF0	0FFF0
CS	selector = F000	selector = F000	selector = F000
	base = FFFF0000	base = FFFF0000	base = FFFF0000
	limit = FFFF	limit = FFFF	limit = FFFF

Table 8-2. Register State after RESET, INIT and BIST
(Register States are given in Hexadecimal Format) (Continued)

Storage Element	RESET (no BIST)	RESET (BIST)	INIT
DS,ES,FE,GS,SS	selector = 0	selector = 0	selector = 0
	base = 0	base = 0	base = 0
	limit = FFFF	limit = FFFF	limit = FFFF
IDTR	base=0	base=0	base=0
	limit=FFF	limit=FFF	limit=FFF
GDTR,LDTR,TR	undefined	undefined	undefined
CR0	60000010	60000010	Note 1
CR2,3,4	0	0	0
DR3–0	0	0	0
DR6	FFFF0FF0	FFFF0FF0	FFFF0FF0
DR7	00000400	00000400	00000400
Time Stamp Counter	0	0	UNCHANGED
Control and Event Select	0	0	UNCHANGED
TR12	0	0	UNCHANGED
All Other MSR's	undefined	undefined	UNCHANGED
CW	undefined	37F	UNCHANGED
SW	undefined	0	UNCHANGED
TW	undefined	FFFF	UNCHANGED
FIP,FEA,FCS, FDS,FOP	undefined	0	UNCHANGED
FSTACK	undefined	undefined	UNCHANGED
Data and Code Cache	invalid	invalid	UNCHANGED
Code Cache TLB, Data Cache TLB, BTB, SDC	invalid	invalid	invalid

NOTE:
1. CD and NW are unchanged, bit 4 is set to 1, all other bits are cleared.
   State of output pins after RESET:
   High: **LOCK#, ADS#, PCHK#, HIT#, HITM#, FERR#, SMIACT#**
   Low: **HLDA, BREQ**
   High Impedance: **D31–D0**
   Undefined: **A31–A3, BE3#–BE0#, W/R#, M/IO#, D/C#, PCD, PWT, CACHE#**

8.3 Built In Self Test (BIST)

Self test is initiated by holding the **AHOLD** pin HIGH for the clock before **RESET** changes from HIGH to LOW. If asserted asynchronously, AHOLD must be asserted two clocks before and two clocks after **RESET** to guarantee recognition.

No bus cycles are run by the Pentium OverDrive processor during self test. The duration of self test is approximately 2^{19} internal clocks. Approximately 70% of the devices in the processor are tested by BIST.

The Pentium OverDrive processor BIST consists of two parts: hardware self test and microcode self test.

During the hardware portion of BIST, the microcode and all large PLAs are tested. All possible input combinations of the microcode ROM and PLAs are tested.

The constant ROMs, BTB, TLBs, and all caches are tested by the microcode portion of BIST. The array tests (caches, TLBs, and BTB) have two passes. On the first pass, data patterns are written to arrays, read back and checked for mismatches. The second pass writes the complement of the initial data pattern, reads it back, and checks for mismatches. The constant ROMs are tested by using the microcode to add various constants and check the result against a stored value.

Upon completion of BIST, the cumulative result of all tests are stored in the EAX register. If EAX contains 0x0h, then all checks passed; any non-zero result indicates a faulty unit.

During BIST, **EADS#** should not be used to perform snoops, otherwise false **HITM#** indications, with no corresponding write back cycles, can occur.

8.4 Tri-State Test Mode

The Pentium OverDrive processor provides the ability to float all its outputs and bi-directional pins. This includes pins that are floated during bus hold as well as some pins that are not normally floated during normal operation. When the Pentium OverDrive processor is in tri-state test mode, external testing can be used to test on board connections.

The tri-state test mode is invoked by driving **FLUSH#** low for 2 clocks before and 2 clocks after **RESET** going low. The outputs are guaranteed to tri-state no later than 10 clocks after **RESET** goes low. The processor will remain in tri-state test mode until the next **RESET.**

8.5 Cache, TLB and BTB Test Registers

The Pentium OverDrive processor contains several test registers. The purpose of the test registers is to provide direct access to the processor caches, TLBs, and BTB, so user programs can easily exercise these structures. Because the architecture of the caches, TLBs, and BTB is different, a different set of test registers (along with a different test mechanism) is required for each. Most test registers can be shared between the code and data caches.

Since much of the testability hardware is used for other purposes during normal operation of the Pentium OverDrive processor, some restrictions may exist on what software may do while testability operations are being run.

Please contact Intel for more information on the Pentium OverDrive processor Cache, TLB, and BTB Test Registers.

8.6 Fan Protection Mechanism and THermal ERRor Bit

The Pentium OverDrive processor employs an active fan/heatsink unit to assist in cooling the processor. Another integral part of this cooling solution is the ability for software to poll the status of the fan to determine if the fan has fallen to a speed that is unacceptable to cool the processor. Should the fan fall into a speed range that is too slow, a control register will record the event. (For more information, please contact Intel.)

9.0 MECHANICAL AND ELECTRICAL DESIGN CONSIDERATIONS

9.1 Introduction

This section provides mechanical and electrical guidelines for designing a system to support the Pentium OverDrive processor. The layout considerations for the socket and spatial requirements for the Pentium OverDrive processor are discussed first, along with other mechanical issues. Sample circuits for support of the Pentium OverDrive processor in write back or write through cache mode are provided in the electrical section. Any design using the Pentium OverDrive processor must take the thermal considerations of the processor into account as well. To this end, thermal design numbers and calculations for the fan/heatsink unit are also provided.

9.2 Mechanical Design Considerations

This section discusses the mechanical design considerations for the Pentium OverDrive processor, including dimensions and the active heat sink unit.

9.2.1 PHYSICAL DIMENSIONS

The Pentium OverDrive processor is designed to fit in a standard 240-lead (19 x 19) PGA socket with four corner pins removed. The Pentium OverDrive processor will use an active heat sink, and therefore requires more vertical clearance. For more discussion on the Pentium OverDrive processor active heat sink, please see the following section.

The maximum and minimum dimensions of the Pentium OverDrive processor package with the active heat sink are shown in Table 9-1. The active heat sink unit is divided into the size of the actual heat sink, and the required free space above the heat sink. The total height required for the Pentium OverDrive processor from the motherboard will depend on the height of the PGA socket. The total external height given in the table below is only measured from the PGA pin stand-offs. Table 9-1 also details the minimum clearance needed around the PGA package.

Table 9-1. Pentium® OverDrive® Processor, 235-Pin, PGA Package Dimensions with Active Heat Sink Attached

Component (inches)	Length and Width		Height	
	Min	Max	Min	Max
PGA Package	1.950	1.975	0.140	0.180
Adhesive	N/A	N/A	0.008	0.012
Fan/Heat Sink	1.77	1.82	0.790	0.810
Required Airspace	0.200	N/A	0.400	N/A
External Pkg. Total	1.950	1.975	0.938	1.002
Min. Ext. w/ Airspace Fixture	2.150		1.338	

9.2.2 ACTIVE HEAT SINK DETAILS

Since the Pentium OverDrive processor dissipates more power than the Intel486 Family, it requires a larger cooling capacity. To accomplish the task of cooling the Pentium OverDrive processor, an active heat sink is attached to the top of the part. The active heat sink will use a heatsink/fan combination to provide airflow at high velocity to the Pentium OverDrive

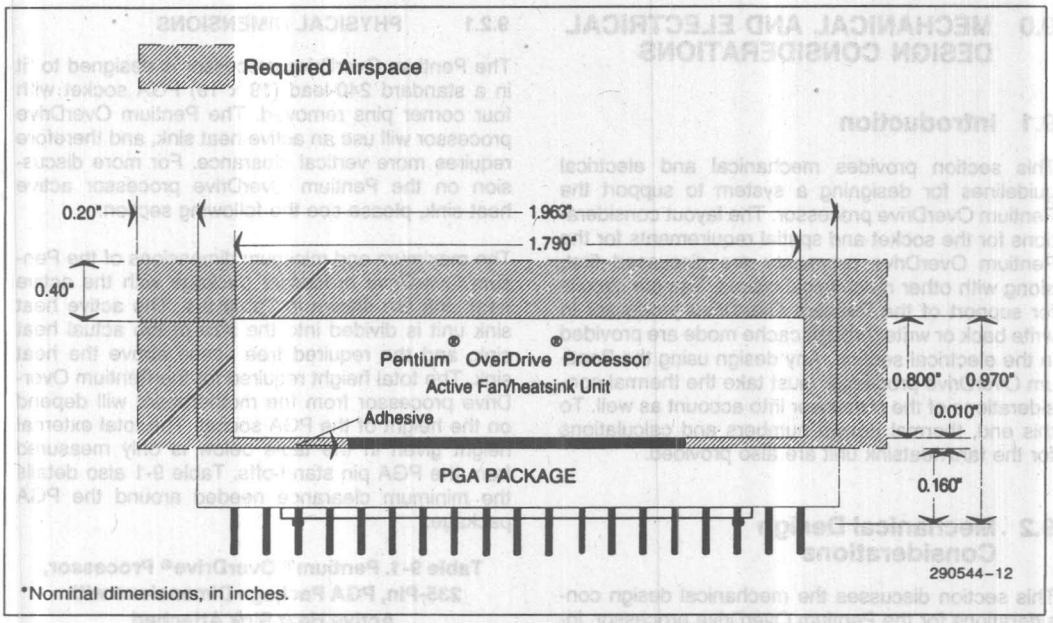


Figure 9-1. 235-Pin, PGA Package with Active Heat Sink Attached

processor. No external connections (Power, etc . . .) will be required for the active heat sink. All the needed connections will be made through the pins of the processor. The amount of extra power needed for the fan is taken into account in the I_{CC} numbers of the processor.

The fan/heatsink unit also supports an integrated thermal protection mechanism that will allow the fan to signal the processor if the speed of the fan should become insufficient to cool the processor. Should this occur, the processor will modify its internal core frequency to match the **CLK** input in a manner that is transparent to the external system. The fan/heatsink has been designed so that should the fan stop, it will have the capability to properly cool the processor in a still air environment. The fan unit is removable so that the unit may be easily replaced. If the fan is removed, or power to the fan is lost, the processor will treat these conditions as if the fan has failed. Figure 9-2 below gives a functional representation of the Pentium OverDrive processor and heat sink unit.

As can be seen in the mechanical dimensions in Table 9-1, the actual height required by the heat sink is less than the total space allotted. Since the Pentium OverDrive processor employs an active heat sink, a certain amount of space is required above the heat sink unit to ensure that the airflow is not blocked. Figure 9-3 shows unacceptable blocking of the airflow for the Pentium OverDrive processor heat sink unit. Figure 9-4 details the minimum space needed around the PGA package to ensure proper heat sink airflow.

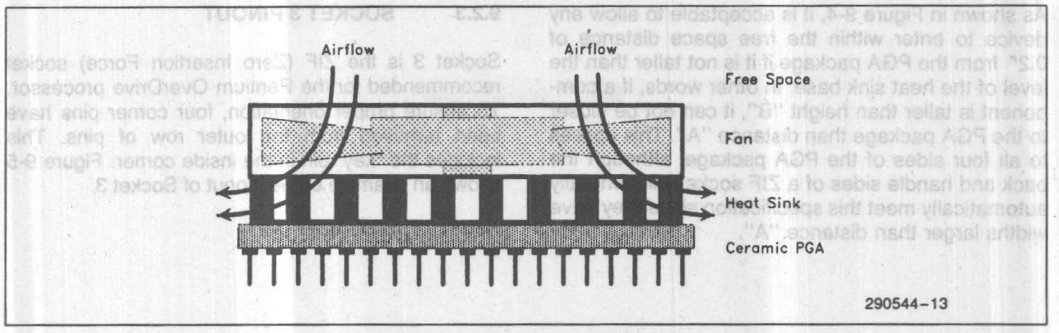


Figure 9-2. Active Heat Sink Example

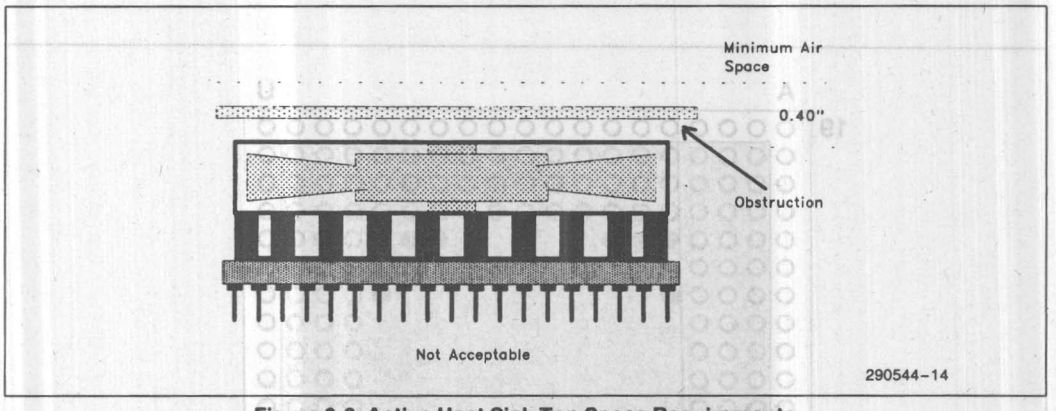


Figure 9-3. Active Heat Sink Top Space Requirements

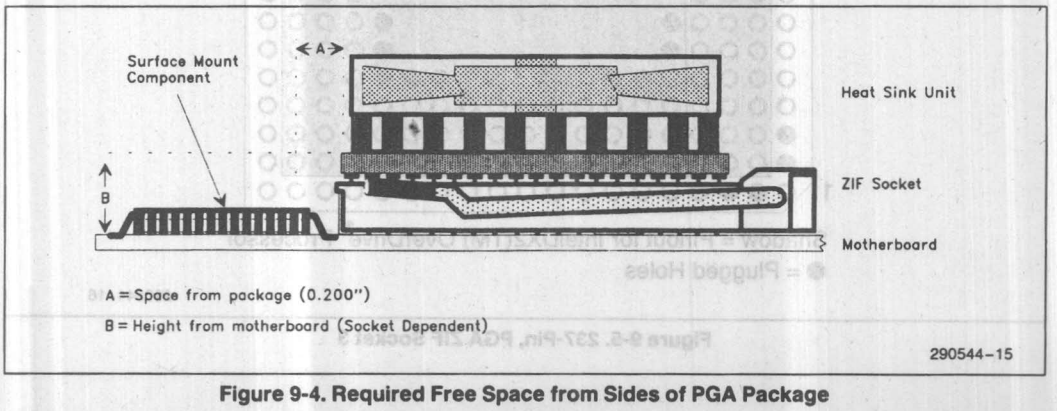


Figure 9-4. Required Free Space from Sides of PGA Package

As shown in Figure 9-4, it is acceptable to allow any device to enter within the free space distance of 0.2" from the PGA package if it is not taller than the level of the heat sink base. In other words, if a component is taller than height "B", it can not be closer to the PGA package than distance "A". This applies to all four sides of the PGA package, although the back and handle sides of a ZIF socket will generally automatically meet this specification since they have widths larger than distance "A".

9.2.3 SOCKET 3 PINOUT

Socket 3 is the ZIF (Zero Insertion Force) socket recommended for the Pentium OverDrive processor. To ensure proper orientation, four corner pins have been removed from the outer row of pins. This includes the "key" pin in the inside corner. Figure 9-5 shows an example of the pinout of Socket 3.

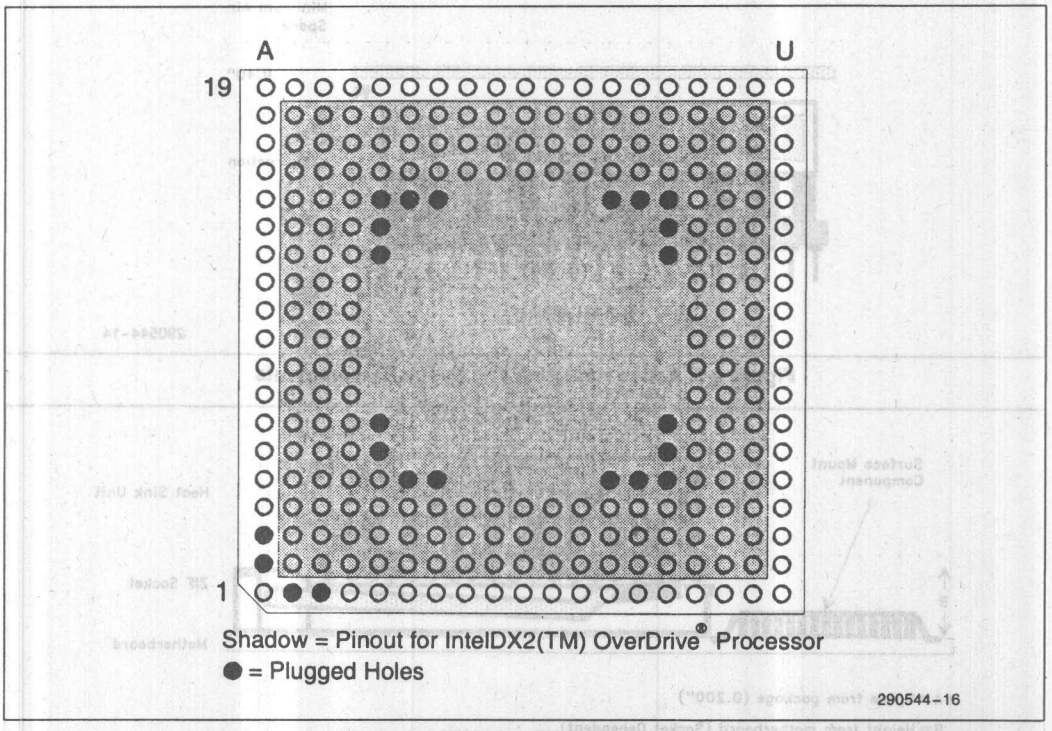


Figure 9-5. 237-Pin, PGA ZIF Socket 3

Product Highlights

- Distinctive socket with the "Socket 3" marking
- Rapid end user access to Socket 3
- Keyed ZIF socket for easy and correct Pentium OverDrive processor installation

9.2.4 "END USER EASY" RECOMMENDATIONS

PC buyers value easy and safe upgrade installation. PC manufacturers can make upgrade component installation in the Pentium OverDrive processor socket simple and foolproof for the end user and reseller by implementing the suggestions listed in Table 9-2. These are presented here as strong guidelines for any Pentium OverDrive processor design.

Table 9-2. Socket and Layout Considerations

"End User Easy" Feature	Implementation
Visible Pentium OverDrive Processor Socket	The Pentium OverDrive processor socket should be easily visible when the PC's cover is removed. Label the Pentium OverDrive Processor socket and the location of pin 1 by silk screening this information on the PC board.
Accessible Pentium OverDrive Processor Socket	Make the Pentium OverDrive processor socket easily accessible to the end user. (e.g., do not place the Pentium OverDrive processor socket under a disk drive.) Be sure to leave enough clearance to open the Zero Insertion Force (ZIF) socket.
Foolproof Chip Orientation	The Pentium OverDrive processor socket must insure proper orientation of the Pentium OverDrive processor. The 236-pin, PGA package of the Pentium OverDrive processor is orientated by the four corner pins that have been removed from the "pin 1" corner. These four contacts (A2, A3, B1, and C1) in the socket should be plugged, such that PGA pins cannot be inserted, to assure correct orientation. All inside contacts (11 innermost rows) should be plugged, except the "key" pin (E5), to insure correct orientation and alignment. The total number of contacts fo the Pentium OverDrive processor socket is therefore 237; a standard 240-pin socket plus the inside "key" pin and less the four outside corner pins. Supplying a 237-pin socket as the Pentium OverDrive processor socket eliminates the possibility of end users or resellers damaging the PC board or the Pentium OverDrive processor by powering up the system with the Pentium OverDrive processor in the incorrect orientation.
Zero Insertion Force Pentium OverDrive Processor Socket	The high pin count of the Pentium OverDrive processor makes the insertion force required for installation into a screw machine PGA socket excessive. Even most Low Insertion Force (LIF) sockets require more than 60 lbs. of insertion force. A Zero Insertion Force (ZIF) socket insures that the chip insertion force does not damage the PC board. Be sure to allow enough clearance for the ZIF socket handle. Do not use a LIF or screw machine socket.
"Plug and Play"	Jumper or switch changes should not be needed to electrically configure the system for the Pentium OverDrive processor.
Thorough Documentation	Describe the Pentium OverDrive processor socket and the Pentium OverDrive processor installation procedure in the PC's User's Manual.

9.2.6 ZIF SOCKET VENDORS

Intel can provide a complete list of socket manufacturers that have been qualified to produce Socket 3. For more information, please contact your local Intel sales office.

9.3 Upgrade Circuit Design

9.3.1 DUAL PROCESSOR SITE DESIGN

The Pentium OverDrive processor can reside on the same processor bus as an Intel486 processors. The Pentium OverDrive processor specifies a **UP#** output (Upgrade Present) pin which should be connected directly to the **UP#** input pin of the Intel486 microprocessor. When the Pentium OverDrive processor occupies the Pentium OverDrive processor socket, the UP# signal (active low) forces the Intel486 microprocessor to tri-state all outputs and reduce power consumption. When the Pentium OverDrive processor is not present, a pull-up resistor, internal to the Intel486 microprocessor, drives **UP#** inactive and allows the Intel486 microprocessor to control the processor bus.

9.3.2 SINGLE PROCESSOR SITE DESIGN

A single processor site is defined as a system design that can accept all Intel486 processors in a single socket location. Doing a single socket design requires that certain pins are connected via the **INC** pins of the Pentium OverDrive processor. See Section 9 for more details on how to design a single socket processor site compatible other Intel486 processors.

9.3.3 CIRCUIT CONSIDERATIONS FOR WRITE BACK CACHE SUPPORT

The Pentium OverDrive processor is specified to support the MESI write back protocol for the on-chip cache. To support the write back protocol, seven new signals , are defined for the Pentium OverDrive processor, four of which are present on the Write-Back Enhanced IntelDX2 processor. The new signals defined for MESI write back capability are **WB/WT#, INV, HIT#, HITM#, CACHE#, EWBE#,** and **BLEN#.** Another new pin, **INIT,** is used to facilitate warm resets. These new signals are defined in detail in Section 2. For more information on designing a system for processor write back cache support that is compatible with the Write-Back Enhanced IntelDX2 processor, please see Section 10.

9.3.4 Pentium® OverDrive® PROCESSOR DECOUPLING CAPACITORS

Because of the fast internal switching speeds of the Pentium OverDrive processor, it is important that the Pentium OverDrive processor use a liberal amount of decoupling capacitors. For proper V_{CC} transient response, Intel recommends that a system design employ at least 4 each of 47 μF bulk capacitors and 9 each of 0.1 μF and 0.01 μF capacitors. It is recommended that surface mount capacitors be used for decoupling the Pentium OverDrive processor. This style of capacitor introduces less inductance than leaded capacitors, so fewer are needed to achieve the same results. The capacitors should be added around the Pentium OverDrive processor in a manner that ensures they are evenly spread about and close to the processor location.

9.4 Socket Test Requirements

The electrical functionality of the Pentium OverDrive processor socket can be verified by fully testing the PC with a populated Pentium OverDrive processor socket. The Pentium OverDrive processor should be used to test for hardware and software compatibility. The BIOS requirements to maintain compatibility with all OverDrive processors are discussed in the Implementation Speicific Details section of the Pentium OverDrive processor Specification. All OverDrive processors undergo thorough application software compatibility testing prior to their introduction. If the system design supports a write back processor cache, the design should be tested with the Write-Back Enchanced IntelDX2 processor as well.

9.5 Thermal Management

The Pentium OverDrive processor and system chassis have several unique design requirements due to the attached active heat sink. The following sections provide sample maximum system operating temperature calculations so that systems may be designed to comply with the thermal requirements of the Pentium OverDrive processor.

9.5.1 THERMAL CALCULATIONS FOR A HYPOTHETICAL SYSTEM

The following equation can be used to calculate the maximum operating temperature of a system.

$T_{A(IN)} = T_{SINK} - (Power * \theta_{SI})$

The parameters are defined as follows:

$T_{A(IN)}$: The temperature of the air going **into** the heat sink fan unit.

T_{SINK}: Temperature of heat sink base, as measured in the center.

Power: Dissipation in Watts = $V_{CC} * I_{CC}$

θ_{SI}: Heat Sink to Internal Temperature [$T_{A(IN)}$] Thermal Resistance

$T_{A(OUT)}$: The temperature of the air outside the system.

Since the Pentium OverDrive processor uses an active heat sink, θ_{SI} is relatively constant, regardless of the airflow provided to the processor. The θ_{SI} is provided in Table 9-3. Table 9-4 details the maximum current requirements of the Pentium OverDrive processor. The maximum allowable $T_{A(IN)}$ is 55°C for both 25 MHz and 33 MHz with the heat sink attached.

Table 9-3. Thermal Resistance (°C/W) θ_{SI}

Processor Type	θ_{SI}—°C/W
Active Heat Sink	2.4

Table 9-4. Pentium® OverDrive® Processor Typical and Maximum I_{CC} Values

System Frequency (MHz)	Processor Typical I_{CC} (mA)	Processor Maximum I_{CC} (mA)
25	TBD	1900
33	TBD	2800

I_{CC} is dependent upon the V_{CC} level of the system, processor bus loading, software code sequences, and silicon process variations. For the Pentium OverDrive processor specifications, the maximum I_{CC} value is derived by testing a sample of components under the following worst case conditions: V_{CC} = 5.3V, full DC current loads on all output pins, and running a file with the predicted worst case software code sequences at the specified frequency. The typical I_{CC} value published is the I_{CC} corresponding to the worst observed I_{CC} value for an average component running under the above worst case conditions. No additional margin is added to this value. I_{CC} typical is not a guaranteed specification.

9.5.2 AIRFLOW

Since the Pentium OverDrive processor employs an active heat sink, it is not as important that the processor heat sink receive direct airflow, rather that the system has sufficient capability to remove the warm air that the Pentium OverDrive processor will generate. This implies that enough airflow exists at the Pentium OverDrive processor socket site to keep localized heating from occurring. This can be accomplished by a standard power supply fan with a clear path to the processor. Figure 9-6 shows how system design can cause localized heating to occur by limiting the airflow in the area of the processor. The airflow supplied in the system should also be enough to insure that the OEM processor shipped with the system will meet the OEM processor thermal specifications before the system is upgraded with the Pentium OverDrive processor.

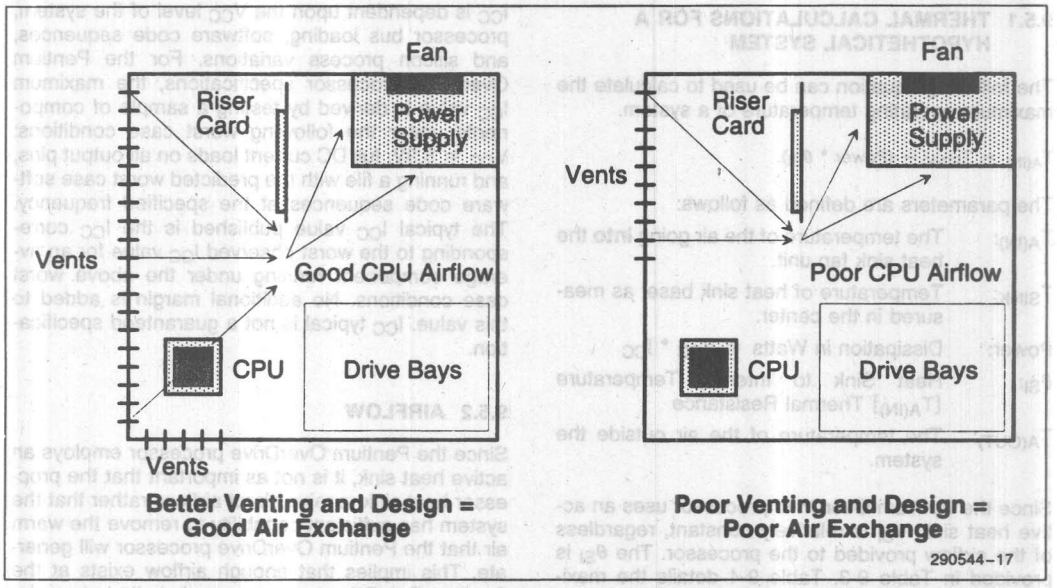


Figure 9-6. Pentium® OverDrive® Processor Airflow Design Examples

10.0 DESIGNING FOR Write-Back Enhanced IntelDX2/Pentium® OverDrive® PROCESSOR COMPATIBILITY

End Users have made upgradability an expected feature in any personal computer purchase. The Pentium OverDrive Processor is the intended upgrade for systems based on the Write-Back Enhanced IntelDX2 processor, an IntelDX2 processor with an on-board write back cache. When installed in a system designed to support a write back processor cache, the Pentium OverDrive processor can reach its full performance potential.

To make the task of designing an upgradable system easier, the Write-Back Enhanced IntelDX2 and the Pentium OverDrive processor have been designed to be compatible with one another. However, since the Pentium OverDrive processor retains many of its Pentium processor features, certain system design considerations must be taken into account to ensure that a Write-Back Enhanced IntelDX2 processor system can be upgraded seamlessly.

Throughout this section, a "Single Socket Design" will refer to a motherboard design that has only one processor site. This means that the Write-Back Enhanced IntelDX2 processor must be removed from the socket before the Pentium OverDrive processor can be installed. A "Dual Socket Design" refers to a two socket motherboard, one in which the Write-Back Enhanced IntelDX2 resides in a fixed location, and the Pentium OverDrive processor is installed into an empty upgrade socket. This section will make reference to both types of designs, but concentrates on the single socket design strategy.

The following section provides a list of considerations that must be examined to allow a Pentium OverDrive processor to operate properly in a system designed to support the Write-Back Enhanced IntelDX2 processor and a write back processor cache. The considerations listed here are only intended to be relevant to the Write-Back Enhanced IntelDX2 processor Enhanced Bus Mode although some may still be valid for the Standard Bus Mode. These considerations are provided as guidelines only, and should be used in conjunction with the rest of this document to ensure proper Pentium OverDrive processor operation.

10.1 Pinout Differences

The Pentium OverDrive processor pinout is based on a 19x19 PGA package as opposed to the Write-Back Enhanced IntelDX2 processor 17x17 PGA package. Most of the signals that are common between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor exist on the same pin on both parts (assuming that pin A1 on the Write-Back Enhanced IntelDX2 processor = Pin B2 on the Pentium OverDrive processor).

NOTE:
All references to Pentium OverDrive processor pins are with respect to a 19x19 grid, while references to Write-Back Enhanced IntelDX2 processor pins are on a 17x17 grid.

10.1.1 ADDITIONAL PINS ON THE Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor defines signal pins that provide functionality that the Write-Back Enhanced IntelDX2 processor does not have. These pins are defined in Table 10-1 below.

Table 10-1. Additonal Pentium® OverDrive® Processor Pins

Signal Name	Pentium® OverDrive® Processor Pin/ Write-Back Enhanced IntelDX2 Processor Pin	Comment
BLEN# (Input)	A7/Not Present	**BLEN#** (Burst Length) controls write bursting on the Pentium OverDrive processor. It can not be toggled and should be tied high, low, or left unconnected. It must be driven LOW if the system is able to accept burst write backs. If **BLEN#** is driven HIGH to force write backs to be written out as four separate write cycles, HOLD will not be recognized until all four cycles have completed, even though each cycle will have its own **ADS#** and **BLAST#**.
EWBE# (Input)	P1/Not Present	**EWBE#** (External Write Buffer Empty) will allow writes to E or M state lines when asserted LOW. If it is sampled HIGH the processor will hold off writes to E or M state lines until asserted LOW again.
HIT# (Output)	U2/Not Present	**HIT#** provides an indication that an external snoop has hit a M,E or S state line in the internal cache.
UP# (Output)	C15/B14	**UP#** is driven LOW to indicate to the system that an upgrade processor is installed. In a single socket design, it shares a pin with the Write-Back Enhanced IntelDX2 processor signal, **TMS.** In a dual socket design, it should be connected to the Write-Back Enhanced IntelDX2 processor **UP#** (Input).

Due to its larger package and the ability to consume more power, the Pentium OverDrive processor also defines a number of extra V_{CC} and V_{SS} pins that the Write-Back Enhanced IntelDX2 processor does not support. The extra pins are listed in Table 10-2.

Table 10-2. Additional V_{CC} and V_{SS} Pins

V_{CC}	V_{SS}	V_{SS}	V_{CC}	V_{SS}	V_{SS}
	A5	U3	K19	G19	
A9	A8	U5	L1	H1	
A10	A12	U6	L19	H19	
A11	A13	U7	R1	M1	
A16	A14	U8	R19	M19	
D1	A15	U12	U4	N19	
D19	A17	U13	U9	Q1	
J1	C19	U14	U10	Q19	
J19	E1	U15	U11	S1	
K1	E19	U17	U16	S19	

10.1.2 PINS NOT SUPPORTED BY THE Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor supports all of the pins on the Write-Back Enhanced IntelDX2 processor except those required for JTAG boundary scan functionality and the **UP#** input pin. Single socket designs should ensure that if boundary scan features are implemented, they will not interfere with the operation of the Pentium OverDrive processor. Dual socket designs should not route the Pentium OverDrive processor into the boundary scan chain. Table 10-3 lists the location of the pins that exist on the Write-Back Enhanced IntelDX2 processor, and the corresponding different signals on the Pentium OverDrive processor.

Table 10-3. Unsupported Write-Back Enhanced IntelDX2 Processor Pins

Write-Back Enhanced IntelDX2 Processor Signal Name/Pin	Pentium® OverDrive® Processor Signal Name/Pin	Comment
TCK (Input) Pin A3	**INC** Pin B4	Pin B4 on the Pentium OverDrive processor is defined as an **INC** pin so that **TCK** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TDI (Input) Pin A14	**INC** Pin B15	Pin B15 on the Pentium OverDrive processor is defined as an **INC** pin so that **TDI** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TDO (Output) Pin B16	**INC** Pin C17	Pin C17 on the Pentium OverDrive processor is defined as an **INC** pin so that **TDO** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TMS (Input) Pin B14	**UP#** (Output) Pin C15	If the Write-Back Enhanced IntelDX2 processor boundary scan features are used in a single socket design, the design should ensure that **TMS** will not conflict with the Pentium OverDrive processor **UP#** when the upgrade is installed.
UP# (Input) Pin C11	**INC** Pin D12	Pin D12 on the Pentium OverDrive Processor is defined as an **INC** pin so that there can be no conflict with **UP#** (Input).

10.1.3 SHARED SIGNALS LOCATED ON DIFFERENT PINS

There are several signals that the Pentium OverDrive Processor has in common with the Write-Back Enhanced IntelDX2 processor, but which are located on different pins. An example of this would be the **HITM#** signal. On the Pentium OverDrive processor, it is located in the outer row of pins, while on the Write-Back Enhanced IntelDX2 processor, it is located on one of the inner row processors. Single socket designs require that these signals be tied together so that the use of a jumper to reroute the signal is unnecessary. This is done through the use of the **INC** pin.

INC pins, by definition are "internally not connected" and may be used for routing of signals. Certain Pentium OverDrive processor **INC** pins should be connected to the signals that correspond to the Write-Back Enhanced IntelDX2 processor write back signals and the **SRESET** signal. Table 10-4 details pins that should be routed together. Please note that the last two columns in Table 10-4 are the pins on the Pentium OverDrive socket which must be routed together.

Table 10-4. Single Socket Compatibility Signals

Signal	Write-Back Enhanced IntelDX2 Processor Signal Pin	Pentium® OverDrive® Processor Signal Pin	Pentium® OverDrive® Processor INC Pins
INV	A10	N1	B11
HITM#	A12	U1	B13
CACHE#	B12	G1	C13
WB/WT#	B13	T1	C14
INIT	C10	F19	D11
FERR#	C14	B14	D15

Figure 10-1 below shows an example of how the INC pins shown in Table 10-4 should be connected together to allow single socket compatibility between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor. The figure is provided as an example only and is not intended to be guide for how the signals should actually be routed on a motherboard.

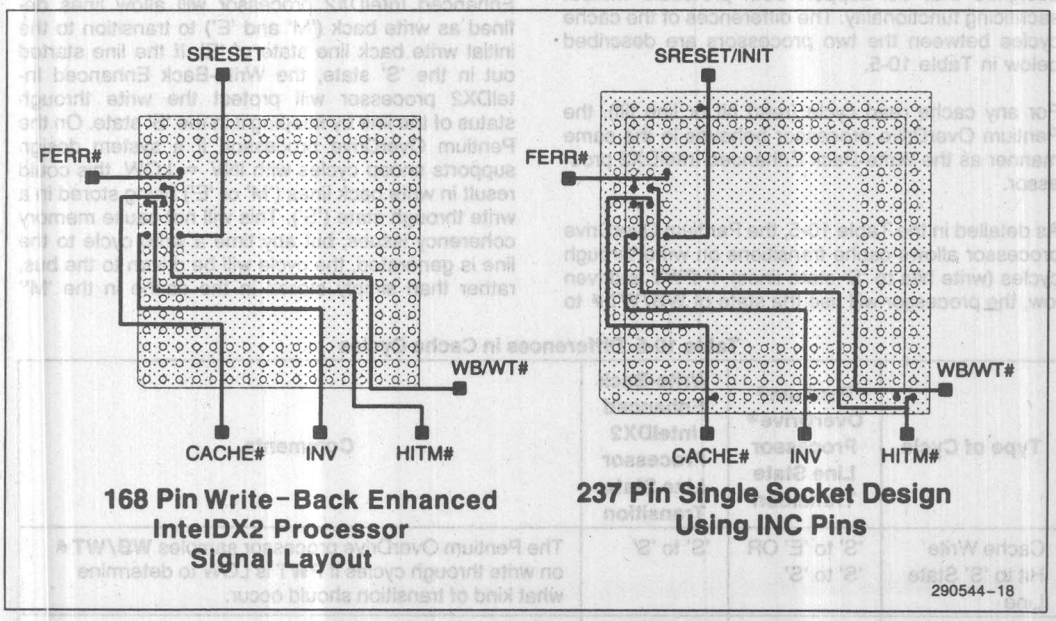


Figure 10-1. Sample Routing of INC Pins

10.2 Functional Differences

The Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor have been designed to be functionally alike, but because the Pentium OverDrive processor is based on the advanced Pentium processor core, there are some minor differences that should be accounted for to ensure that a Pentium OverDrive processor will operate properly in a Write-Back Enhanced IntelDX2 processor-based system.

10.2.1 WRITE BACK PROCESSOR CACHE CONSIDERATIONS

Both the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor support an internal write back processor cache. The Pentium OverDrive processor carries over the Pentium processor cache protocol which supports multiple processors in the same system. The Write-Back Enhanced IntelDX2 processor cache coherency protocol is designed for single processor systems and is a subset of the Pentium OverDrive processor MESI protocol. If implemented correctly, a system can be designed that will support both protocols without sacrificing functionality. The differences of the cache cycles between the two processors are described below in Table 10-5.

For any cache read cycle (read hit or line fill), the Pentium OverDrive processor behaves in the same manner as the Write-Back Enhanced IntelDX2 processor.

As detailed in the Table 10-5, the Pentium OverDrive processor allows cache transitions on write through cycles (write hits to 'S' state lines). If **PWT** is driven low, the processor will use the state of **WB/WT#** to determine the final state of the entire cache line, even if only part of the line was written out by the write through cycle. If **WB/WT#** is driven HIGH, the state of the line will be changed to the 'E' state. If driven LOW, the line will remain in the 'S' state. This differs from the Write-Back Enhanced IntelDX2 processor and its dedicated 'S' state which always enforces the write through properties of a line stored in the 'S' state. If a system allows regions of memory to be stored as write through only via the **WB/WT#** pin, and other memory regions are stored as write back lines, then **WB/WT#** must toggle properly to ensure that 'S' state lines are never changed to write back 'E' lines. If the cache is used in a write back mode only (linefills are never stored in the 'S' state), then there will be no cache coherency issues, but there can be a performance issue due to snoop hits with **INV** = LOW.

For external snoop hits into the cache, the Pentium OverDrive processor differs in behavior from the Write-Back Enhanced IntelDX2 processor only in external snoop hits that drive **INV** = LOW. As shown in Table 10-5, any time a snoop hit occurs with **INV** = LOW, the Pentium OverDrive processor will change the cache line state to 'S'. The Write-Back Enhanced IntelDX2 processor will allow lines defined as write back ('M' and 'E') to transition to the initial write back line state of 'E'. If the line started out in the 'S' state, the Write-Back Enhanced IntelDX2 processor will protect the write through status of the line by keeping it in the 'S' state. On the Pentium OverDrive processor, if a system design supports snoop cycles with INV = LOW, this could result in write back lines ('M' or 'E') being stored in a write through state ('S'). This will not cause memory coherency issues, but any time a write cycle to the line is generated, the cycle will be driven to the bus, rather than simply stored in the cache in the 'M''

Table 10-5. Differences in Cache Cycles

Type of Cycle	Pentium® OverDrive® Processor Line State Transition	Write-Back Enhanced IntelDX2 Processor Line State Transition	Comments
Cache Write Hit to 'S' State Line	'S' to 'E' OR 'S' to 'S'	'S' to 'S'	The Pentium OverDrive processor samples **WB/WT#** on write through cycles if **PWT** is LOW to determine what kind of transition should occur.
External Snoop Hit **INV** = 0	'M' to 'S' 'E' to 'S' 'S' to 'S'	'M' to 'E' 'E' to 'E' 'S' to 'S'	The assumption that a Write-Back Enhanced IntelDX2 processor will operate in a single processor system allows for direct transitions to the 'E' state.

state. To avoid performance issues, systems that can drive **INV** = LOW should drive **WB/WT#** = HIGH when a write through cycle to such a line occurs on the bus. As shown in Table 10-5, this will ensure that a write back line that has accidentally been converted to a write through line will not cause more than one unnecessary write cycle on the bus.

10.2.2 STANDARD/ENHANCED BUS DIFFERENCES

Both the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor use the **WB/WT#** pin as an initialization input on the falling edge of **RESET.** Several signals behave differently depending on if the processors are operating in enhanced bus mode or standard bus mode. Some of these behaviors are slightly different between the Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor, and are listed below in Table 10-6.

Table 10-6. Differences in Bus Modes

Functionality	Pentium® OverDrive® Processor	Write-Back Enhanced IntelDX2 Processor
Standard Bus Mode CPUID	0153xh x = 0 to F	0043xh x = 0 to F
Enhanced Bus Mode CPUID	0153xh x = 0 to F	0047xh x = 0 to F
Standard Bus Mode **INIT**	**INIT** is treated as an Interrupt	SRESET is not an interrupt
Standard Bus Mode **FLUSH#**	**FLUSH#** will take about 15 Bus CLKs No Write Backs	**FLUSH#** will take 1 Bus CLK No Write Backs

One item to note in Table 10-6 is that the **INIT** pin on the Pentium OverDrive processor is treated as an edge triggered interrupt in both the standard and enhanced bus modes. This means that **INIT** will not be recognized until instruction boundaries, and after **INIT** has been asserted and recognized, more ADS# cycles can be started, even if **INIT** has not been deasserted.

10.2.3 SOFTWARE DIFFERENCES

Due to the Pentium processor features found on the Pentium OverDrive processor, there are several software visible differences that should be accounted for in any system specific firmware or BIOS routines.

10.2.3.1 Cache Testing and Test Registers

The cache of the Pentium OverDrive processor is structured as separate code and data caches, each 16 KBytes in size. Because of this structure, the Pentium OverDrive processor supports Model Specific Registers (MSR's) for cache testing, rather than the Write-Back Enhanced IntelDX2 processor Test Registers. Any attempt to access the Write-Back Enhanced IntelDX2 processor test registers on the Pentium OverDrive processor will result in invalid opcode exceptions. For more information on testing the caches of the Pentium OverDrive processor, please contact Intel.

10.2.3.2 Timing Loops

Timing loops (i.e.: executing a tight loop that does nothing) are a common method of providing a software based delay for I/O recovery. Because of the Pentium processor core and an increased core speed, the Pentium OverDrive processor will be able to execute instructions must faster than previous generations of processors. It is suggested that timing loops be avoided, and that a hardware based delay scheme be developed, such as writing to a dummy I/O port that will delay the returning of **RDY#** for a fixed amount of time.

10.2.4 EXTERNAL SNOOPING REQUIREMENTS ON EADS#

The specification set out in the Hardware Design Considerations Section (Sections 4.1.1 and 4.1.2) must be observed to ensure that EADS# will be recognized properly by both the Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor.

10.2.5 DIFFERENCES IN STOP GRANT STATE OPERATION

If the **STPCLK#** pin is asserted and the Pentium OverDrive processor issues the stop grant special cycle, the processor is in the stop grant state. While in this state, the following conditions apply:

1) If any of the following interrupts are asserted, they will be latched and serviced as soon as the **STPCLK#** pin is released and the processor exits the stop grant state:

   FLUSH#, SMI#, NMI, INIT

   If an interrupt is asserted and then released while the processor is in the stop grant state, it will be recognized once the processor exits the stop grant state even though the interrupt may be deasserted. This behavior is different than that of the Write-Back Enhanced IntelDX2 processor, which requires these interrupts to be held until the processor has exited the stop grant state.

   NOTE:
   INTR is a level triggered interrupt and will not be latched. It must be held until the interrupt acknowledge cycle to guarantee recognition.

2) Unlike the Write-Back Enhanced IntelDX2 processor, if **INIT** is asserted while in the stop grant state, the processor will not automatically exit the stop grant state and perform the **INIT.** As mentioned above, **INIT** is latched and will be recognized once the processor exits the stop grant state when **STPCLK#** is deasserted.

11.0 DC/AC SPECIFICATIONS

The electrical specifications in this section represent the electrical interface of the Pentium OverDrive processor. The Pentium OverDrive processor will be compatible to the AC/DC specifications presented in this section.

Table 11-1 provides the absolute maximum ratings. It is a stress rating only, and functional operation at the maximums is not guaranteed. Function operating conditions are given in Section 11.1 (DC Specifications) and 11.2 (A. C. Specifications).

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium OverDrive processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 11-1. Absolute Maximum Ratings

Case Temperature under Bias . . . −30°C to +110°C

Fan/Heatsink Temperature under Bias . . . . . −5°C to +60°C

Processor Storage Temperature . . . . . −30°C to +125°C

Fan/Heatsink Storage Temperature . . . . . −40°C to +70°C

Voltage on any Pin with Respect to Ground . . −0.5V to (V_{CC} + 0.5V)

Supply Voltage with respect to V_{SS} . . . . . −0.5V to +6.5V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

11.1 DC Specifications

Table 11-2 provides the DC operating conditions for the Pentium OverDrive processor.

Functional operating range: V_{CC} = 5V +5%; $T_{A(IN)}$ = 0°C to +55°C @33 MHz and 25 MHz.

Table 11-2. DC Parametric Values

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK = 25 MHz CLK = 33 MHz		 1900 2800	 mA	
I_{LI}	Input Leakage Current		±15	µA	(Note 3)
I_{IH}	Input Leakage Current		200	µA	(Note 4)
I_{IL}	Input Leakage Current		−400	µA	(Note 5)
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		13	pF	F_c = 1 MHz (6)
C_O	I/O or Output Capacitance		17	pF	F_c = 1 MHz (6)
C_{CLK}	CLK Capacitance		15	pF	F_c = 1 MHz (6)

NOTES:

1. This parameter is measured at:
   Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
3. This parameter is for inputs without pullups or pulldowns and $0 < V_{IN} < V_{CC}$.
4. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
5. This parameter is for inputs with pullups and V_{IL} = 0.45V.
6. Not 100% tested.

11.2 AC Specifications

Tables 11-3 and 11-4 provide the AC specifications for the Pentium OverDrive processor at external clock frequencies of 25 MHz and 33 MHz respectively. They consist of output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the rising edge of the input system clock unless otherwise specified. Internal core frequencies will be a multiple of the system bus frequency.

11.2.1 V_{CC} TRANSIENT SPECIFICATION

Due to the on-board voltage regulator, the V_{CC} of the Pentium OverDrive processor is allowed to exceed the DC Voltage specifications (V_{CC} = 5V + 5%) when the processor creates a large current transient, as would be the case in a full operation to Autohalt transition (2.5A to 200 mA I_{CC} change). The width of the pulse that exceeds 5V + 5% should be no wider than 1ms, and can not exceed 5.5V. V_{CC} is not allowed to go below the DC specification of 5V − 5% at any time. This specification applies to the Pentium OverDrive processor only and can not be applied to any other Intel processors. Figure 11-1 shows an example of the V_{CC} transient specification.

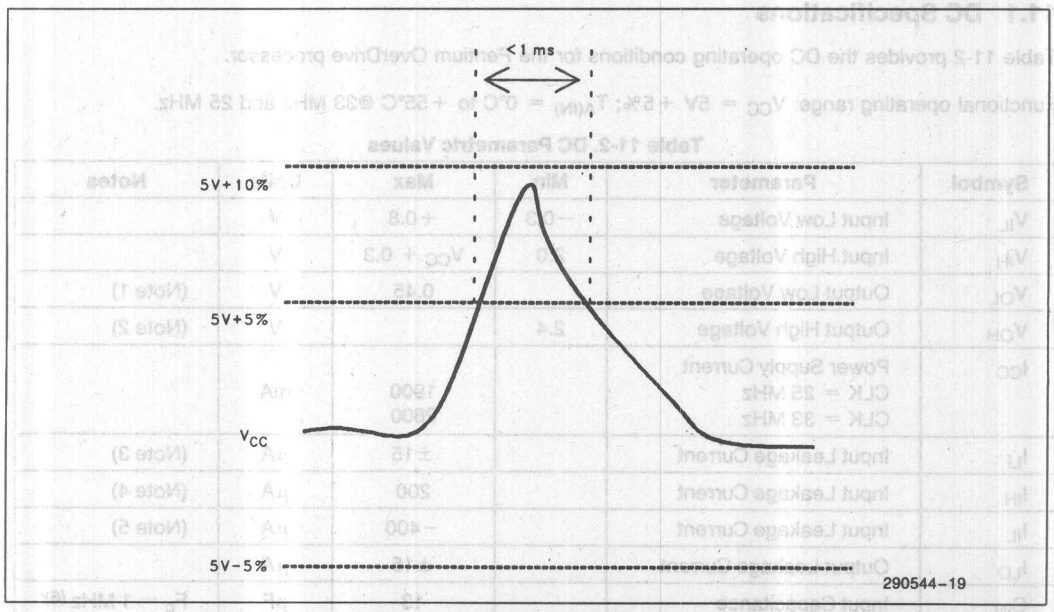


Figure 11-1. V_{CC} Transient Example

Table 11-3. Pentium® OverDrive® Processor—25 MHz AC Characteristics
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
	Frequency	8	25	MHz		1X Clock Input to Processor
t_1	**CLK** Period	40	125	ns	10-1	
t_{1a}	CLK Period Stability		250	ps		Adjacent Clocks
t_2	**CLK** High Time	14		ns	10-1	at 2V
t_3	**CLK** Low Time	11		ns	10-1	at 0.8V
t_4	**CLK** Fall Time		4	ns	10-1	2V to 0.8V
t_5	**CLK** Rise Time		4	ns	10-1	0.8V to 2V
t_6	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#,** Valid Delay	3	19	ns	10-3	
t_7	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#** Float Delay		28	ns	10-3	After Clock Edge(2)
t_8	**PCHK#** Valid Delay	3	24	ns	10-3	
t_{8a}	**BLAST#, PLOCK#** Valid Delay	3	24	ns	10-3	
t_9	**BLAST#, PLOCK#** Float Delay		28	ns	10-3	After Clock Edge(2)
t_{10}	**D0–D31, DP0–3** Write Data Valid Delay	3	20	ns	10-3	
t_{11}	**D0–D31, DP0–3** Write Data Float Delay		28	ns	10-3	After Clock Edge(2)
t_{12}	**EADS#** Setup Time	8		ns	10-2	
t_{13}	**EADS#** Hold Time	3		ns	10-2	
t_{14}	**KEN#, BS16#, BS8#** Setup Time	8		ns	10-2	
t_{15}	**KEN#, BS16#, BS8#** Hold Time	3		ns	10-2	
t_{16}	**RDY#, BRDY#,** Setup Time	8		ns	10-2	
t_{17}	**RDY#, BRDY#,** Hold Time	3		ns	10-2	
t_{18}	**HOLD, AHOLD** Setup Time	8		ns	10-2	
t_{18a}	**BOFF#, SMI#** Setup Time	8		ns	10-2	
t_{19}	**HOLD, AHOLD, BOFF#, SMI#** Hold Time	3		ns	10-2	
t_{20}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Setup Time	8		ns	10-2	
t_{21}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT Hold Time**	3		ns	10-2	

Table 11-3. Pentium® OverDrive® Processor—25 MHz AC Characteristics (Continued)
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified (Continued)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{22}	**D0–D31, DP0–3, A4–A31** Read Setup Time	5		ns	10-2	
t_{23}	**D0–D31, DP0–3, A4–A31** Read Hold Time	3		ns	10-2	
t_{38}	**WB/WT#** and **EWBE#** Setup Time	8		ns	10-2	
t_{39}	**WB/WT#** and **EWBE#** Hold Time	3		ns	10-2	
t_{40}	**INV Setup Time**	8		ns	10-2	
t_{41}	**INV** Hold Time	3		ns	10-2	
t_{42}	**HIT#, HITM#** Valid Delay	3	19	ns	10-3	
t_{43}	**HIT#, HITM#** Float Delay		28	ns	10-3	Only during Three State Test Mode
t_{44}	**CACHE#** Valid Delay	3	19	ns	10-3	
t_{45}	**CACHE#** Float Delay		28	ns	10-3	
t_{46}	**STPCLK#** Setup Time	5		ns	10-2	
t_{47}	**STPCLK#** Hold Time	3		ns	10-2	

NOTES:
1. All timing specifications assume C_L = 50 pF. Section 9.2.1 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
2. Not 100% tested, guaranteed by design characterization.

Table 11-4. Pentium® OverDrive® Processor—33 MHz AC Characteristics
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C TO +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
	Frequency	8	33	MHz		1X Clock Input to Processor
t_1	**CLK** Period	30	125	ns	10-1	
t_{1a}	**CLK** Period Stability		250	ps		Adjacent Clocks
t_2	**CLK** High Time	11		ns	10-1	At 2V
t_3	**CLK** Low Time	8		ns	10-1	At 0.8V
t_4	**CLK** Fall Time		3	ns	10-1	2V to 0.8V
t_5	**CLK** Rise Time		3	ns	10-1	0.8V to 2V
t_6	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#,** Valid Delay	3	14	ns	10-3	
t_7	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# BP3, BP2,** Float Delay		20	ns	10-3	After Clock Edge(2)
t_8	**PCHK#** Valid Delay	3	14	ns	10-3	
t_{8a}	**BLAST#, PLOCK#** Valid Delay	3	14	ns	10-3	
t_9	**BLAST#, PLOCK#** Float Delay		20	ns	10-3	After Clock Edge(2)
t_{10}	**D0–D31, DP0–3** Write Data Valid Delay	3	14	ns	10-3	
t_{11}	**D0–D31, DP0–3** Write Data Float Delay		20	ns	10-3	After Clock Edge(2)
t_{12}	**EADS#** Setup Time	5		ns	10-2	
t_{13}	**EADS#** Hold Time	3		ns	10-2	
t_{14}	**KEN#, BS16#, BS8#** Setup Time	5		ns	10-2	
t_{15}	**KEN#, BS16#, BS8#** Hold Time	3		ns	10-2	
t_{16}	**RDY#, BRDY#,** Setup Time	5		ns	10-2	
t_{17}	**RDY#, BRDY#,** Hold Time	3		ns	10-2	
t_{18}	**HOLD, AHOLD** Setup Time	6		ns	10-2	
t_{18a}	**BOFF#, SMI#** Setup Time	7		ns	10-2	
t_{19}	**HOLD, AHOLD, BOFF#, SMI#** Hold Time	3		ns	10-2	
t_{20}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Setup Time	5		ns	10-2	
t_{21}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Hold Time	3		ns	10-2	

Table 11-4. Pentium® OverDrive® Processor—33 MHz AC Characteristics (Continued)
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C TO +55°C; C_L = 50 pF (1) Unless Otherwise Specified (Continued)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{22}	**D0–D31, DP0–3, A4–A31** Read Setup Time	5		ns	10-2	
t_{23}	**D0–D31, DP0–3, A4–A31** Read Hold Time	3		ns	10-2	
t_{38}	**WB/WT#** and **EWBE#** Setup Time	5		ns	10-2	
t_{39}	**WB/WT#** and **EWBE#** Hold Time	3		ns	10-2	
t_{40}	**INV** Setup Time	5		ns	10-2	
t_{41}	**INV** Hold Time	3		ns	10-2	
t_{42}	**HIT#, HITM#** Valid Delay	3	14	ns	10-3	
t_{43}	**HIT#, HITM#** Float Delay		20	ns	10-3	Only during Three State Test Mode
t_{44}	**CACHE#** Valid Delay	3	14	ns	10-3	
t_{45}	**CACHE#** Float Delay		20	ns	10-3	
t_{46}	**STPCLK#** Setup Time	5		ns	10-2	
t_{47}	**STPCLK#** Hold Time	3		ns	10-2	

NOTES:
1. All signal timings except Boundary Scan timing specifications assume C_L = 50 pF. Section 9.2.1 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
2. Not 100% tested, guaranteed by design characterization.

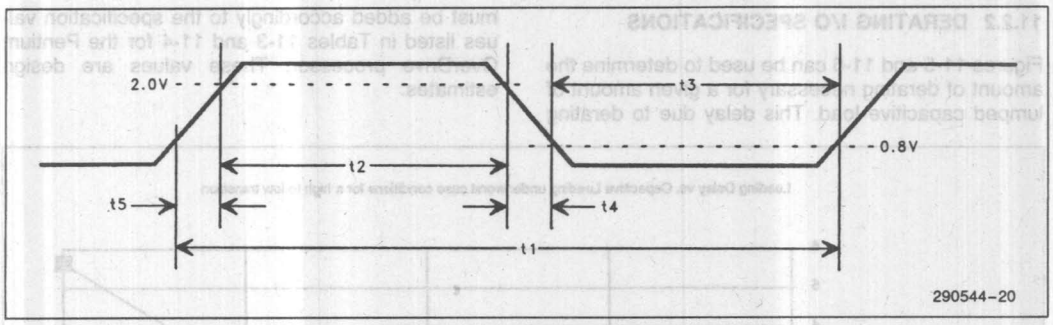


Figure 11-2. CLK Waveform

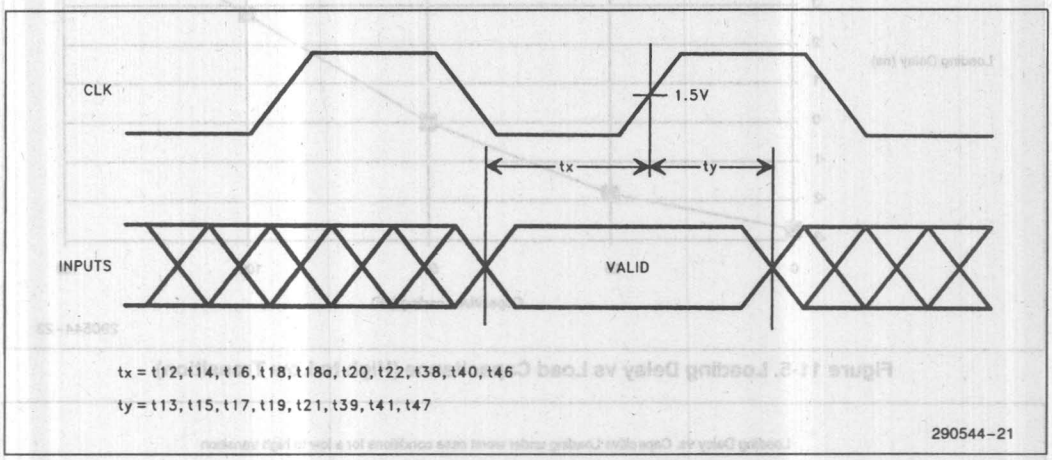


Figure 11-3. SETUP and HOLD Timings

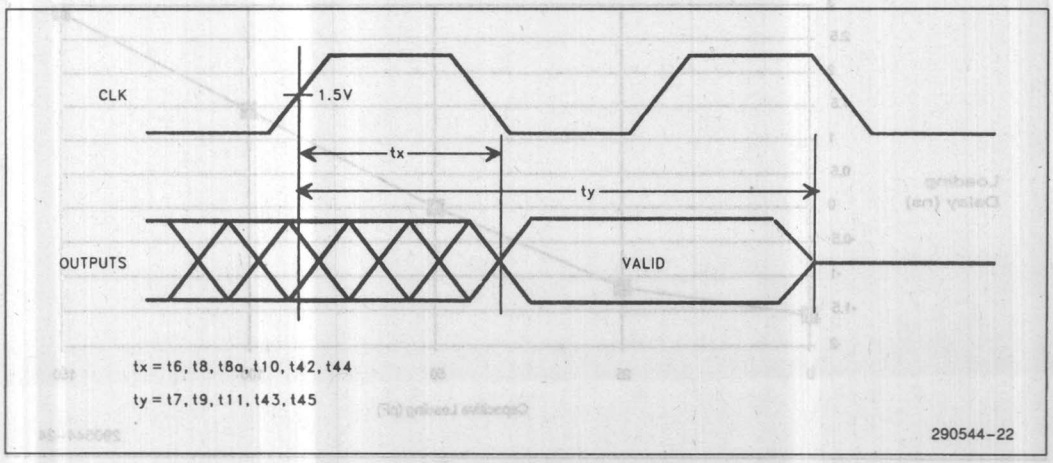


Figure 11-4. Valid and Float Delay Timings

11.2.2 DERATING I/O SPECIFICATIONS

Figures 11-5 and 11-6 can be used to determine the amount of derating necessary for a given amount of lumped capacitive load. This delay due to derating must be added accordingly to the specification values listed in Tables 11-3 and 11-4 for the Pentium OverDrive processor. These values are design estimates.

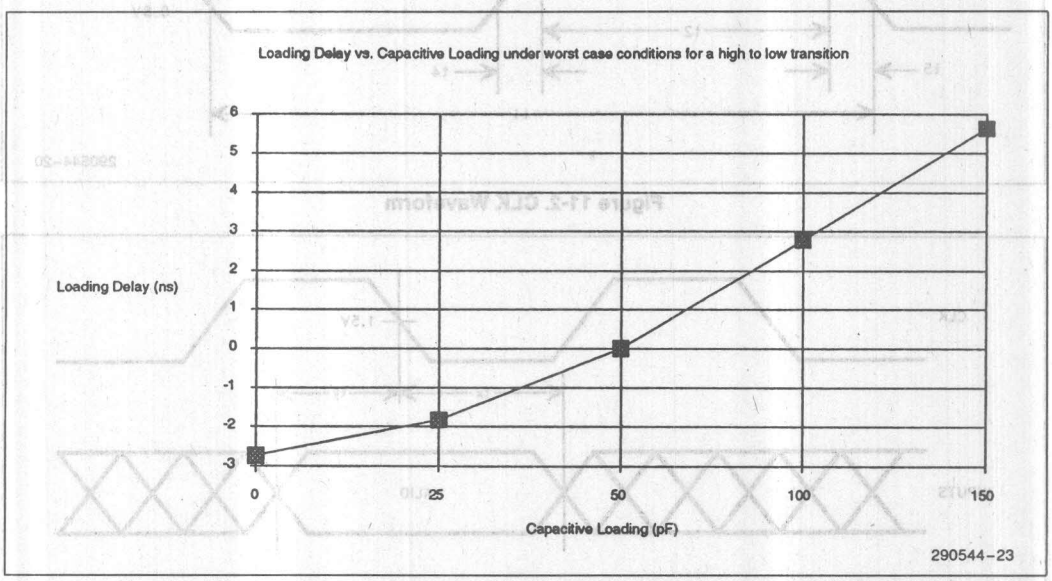


Figure 11-5. Loading Delay vs Load Capacitance (High to Low Transition)

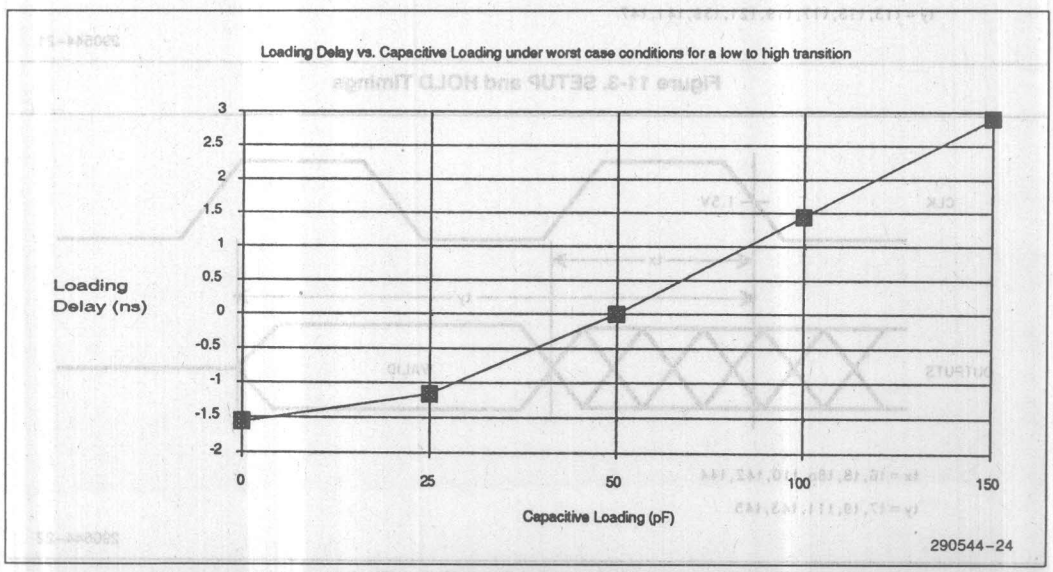


Figure 11-6. Loading Delay vs Load Capacitance (Low to High Transition)

Refer to the Pentium Processor Data Book for more information on instruction execution timing and pairing.

A generic discussion on the operation of cache memories can be found in the Intel Cache Tutorial available from your Intel sales representative or from Intel's Literature department, order #296543-002.

Pentium® OverDrive® PROCESSOR FOR Pentium PROCESSOR-BASED SYSTEMS

120/133-MHz Pentium® OverDrive® Processor -
to upgrade 60- and 66-MHz Pentium Processors

- **Powerful Processor Upgrades for Upgradable Pentium® Processor-Based Systems**
- **Superscalar Architecture**
  - **— Dual Pipelined Integer Units and Pipelined Floating-Point Unit**
- **8KB Data and 8KB Instruction Cache**
- **.35μM BiCMOS Silicon Technology**
- **On-package Voltage Regulation and Voltage Filtering**
- **Integrated Fan/Heatsink Thermal Solution**
- **Compatible with Installed Software Base**
  - **— MS-DOS*, Windows*, Windows 95, Windows NT, OS/2*, UNIX***
- **Product Line Supports Socket 4 Designs**
- **273 pin PGA Package**
- **Easy Installation**
- **Supports 60- and 66-MHz Bus Speeds**
- **5.0 Volt Supply**

The Pentium® OverDrive® processor is an end-user, single chip, processor upgrade for Pentium processor-based systems. The end users are able to increase the performance of their PCs by simply replacing the existing processor with a Pentium OverDrive processor. The Pentium OverDrive processor provides the performance needed for today's mainstream desktop applications and workstations. The Pentium OverDrive processor upgrades Pentium processor-based systems to faster Pentium technology. The Pentium OverDrive processor is binary compatible with the Pentium processors and compatible with the entire installed base of applications for MS-DOS*, Windows*, Windows 95, Windows NT, OS/2*, and UNIX*.

The 120/133-MHz Pentium OverDrive processor is designed to upgrade 60- and 66-MHz Pentium processor-based systems with Zero Insertion Force (ZIF) Socket 4. This upgrade product doubles the internal clock speed of the processor without requiring system jumper changes.

The Pentium OverDrive processors for Pentium processor-based systems have 3.3 million transistors and are built on Intel's advanced 0.35-micron silicon technology. The Pentium OverDrive processors are equipped with high reliability, integrated fan/heatsinks.

August 1997 Order Number: 290579-001

intel

Pentium® OverDrive® PROCESSOR FOR Pentium PROCESSOR-BASED SYSTEMS

120/133-MHz Pentium® OverDrive® Processor
to upgrade 60- and 66-MHz Pentium Processors

- Powerful Processor Upgrades for Upgradable Pentium® Processor-Based Systems
- Superscalar Architecture
  - Dual Pipelined Integer Units and Pipelined Floating-Point Unit
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- On-package Voltage Regulation and Voltage Filtering
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August 1997 Order Number 290279-001

1.0 INTRODUCTION

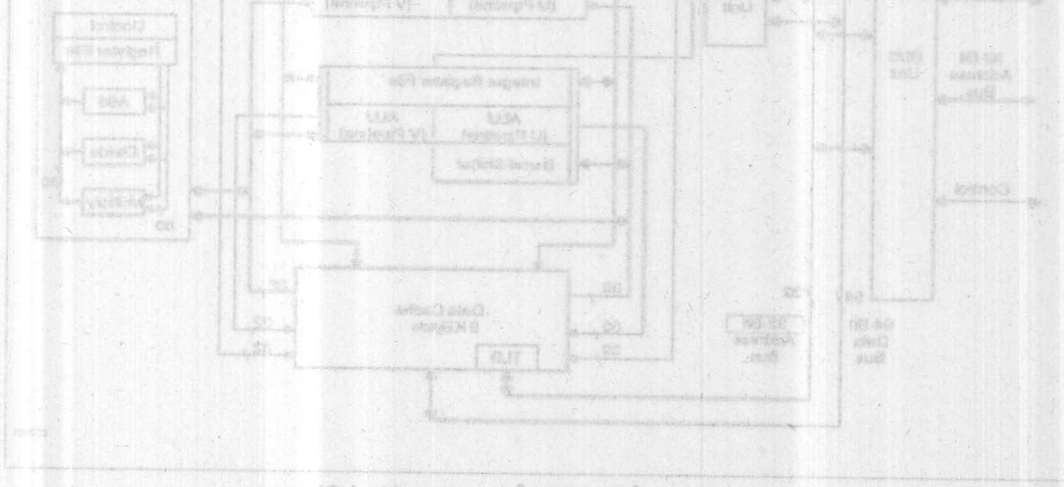
This datasheet describes Intel Pentium OverDrive processor for upgradable Pentium processor based-systems. The Pentium OverDrive processor currently includes upgrades for 60- and 66-MHz Pentium processors. In the future, Intel will also offer faster Pentium OverDrive processors for 120 and 133-MHz Pentium processors, and continues to offer Pentium OverDrive processors for Intel486™ processors. Technical description of the Pentium OverDrive processor for Intel486 processors is available in *Intel OverDrive® Processors* datasheet (Order #290436).

This datasheet is intended to be used in conjunction with the *Pentium® Family User's Manual* (Order #241428), which describes the Pentium family architecture and functionality. All enhancements or differences between the Pentium OverDrive processor and the original processor (i.e., 60/66-MHz Pentium processor vs. 120/133-MHz Pentium OverDrive processor) are described in this datasheet. Pentium processor-based systems that are compatible to the Pentium OverDrive processor(s) must be designed to both the original processor specifications and the Pentium OverDrive processor(s) specifications.

1.1. Product Overview

Pentium OverDrive processors, for upgradable Pentium systems, allow users to upgrade to more advanced Pentium processor technology. The following sections provide an overview of each of the Pentium OverDrive processors. Refer to the later section for more detailed information.

Figure 1 contains the block diagram of the Pentium OverDrive processor. Figure 2 lists some of the key features of the Pentium OverDrive processors. Figure 3 describes the upgrade choices available for an existing Pentium processor system.



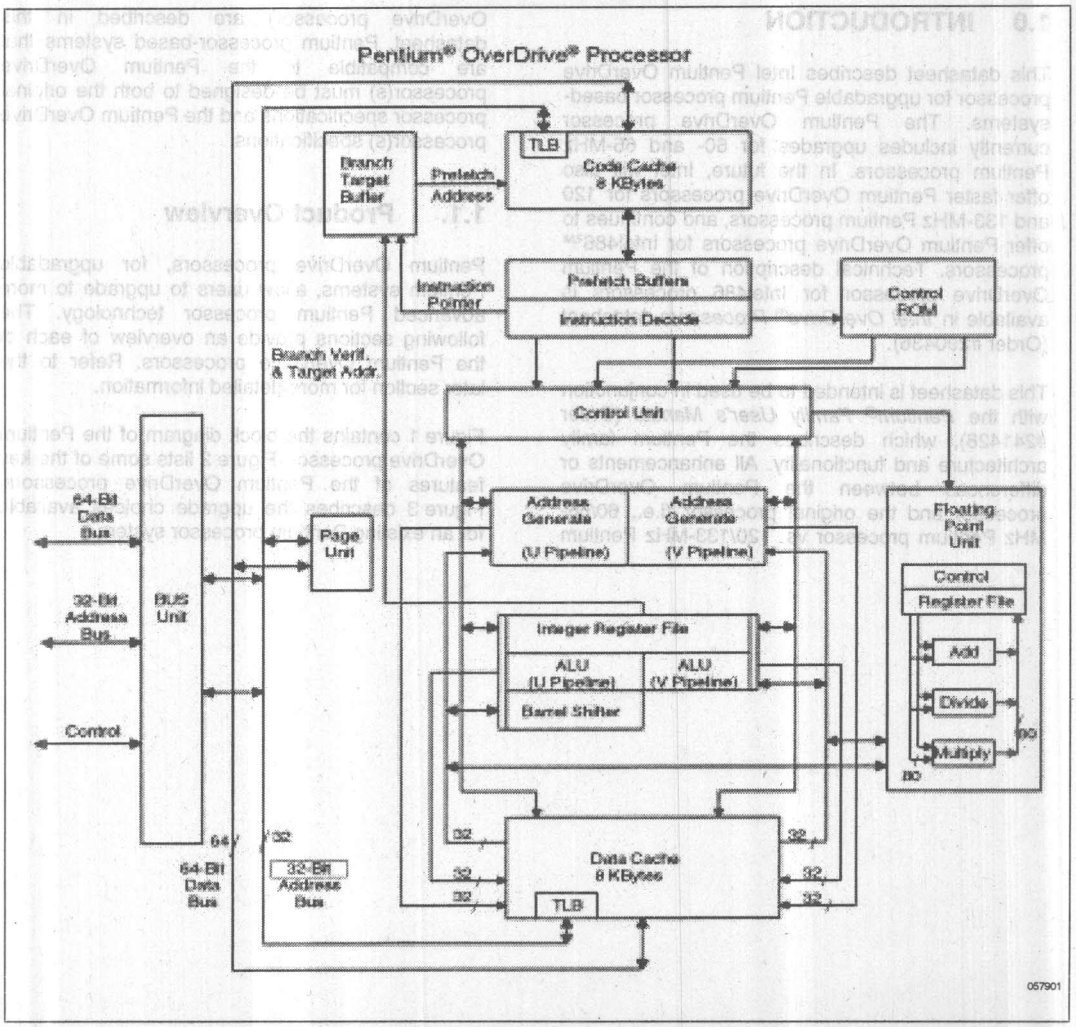


Figure 1. Pentium® OverDrive® Processor Block Diagram

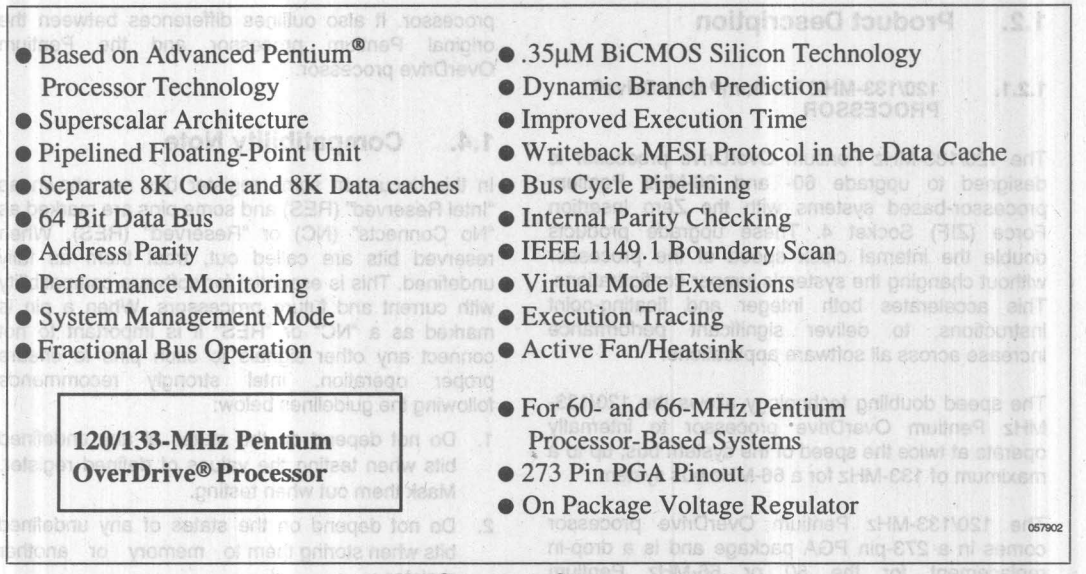


Figure 2. Pentium® OverDrive® Processor Key Features

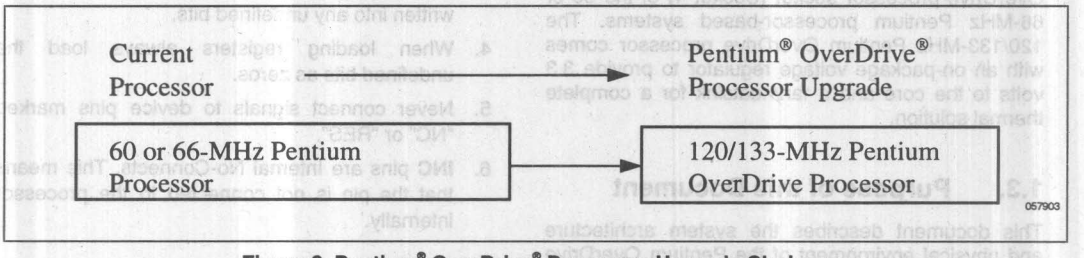


Figure 3. Pentium® OverDrive® Processor Upgrade Choices

1.2. Product Description

1.2.1. 120/133-MHZ Pentium® OverDrive® PROCESSOR

The 120/133-MHz Pentium OverDrive processor is designed to upgrade 60- and 66-MHz Pentium processor-based systems with the Zero Insertion Force (ZIF) Socket 4. These upgrade products double the internal clock speed of the processor without changing the system's jumper configurations. This accelerates both integer and floating-point instructions, to deliver significant performance increase across all software applications.

The speed doubling technology allows the 120/133-MHz Pentium OverDrive processor to internally operate at twice the speed of the system bus; up to a maximum of 133-MHz for a 66-MHz bus system.

The 120/133-MHz Pentium OverDrive processor comes in a 273-pin PGA package and is a drop-in replacement for the 60 or 66-MHz Pentium processor. It is designed to be installed into the OverDrive processor socket (Socket 4) of the 60 or 66-MHz Pentium processor-based systems. The 120/133-MHz Pentium OverDrive processor comes with an on-package voltage regulator to provide 3.3 volts to the core and a fan/heatsink for a complete thermal solution.

1.3. Purpose of this Document

This document describes the system architecture and physical environment of the Pentium OverDrive processor. It also outlines differences between the original Pentium processor and the Pentium OverDrive processor.

1.4. Compatibility Note

In this document some register bits are shown as "Intel Reserved" (RES) and some pins are marked as "No Connects" (NC) or "Reserved" (RES). When reserved bits are called out, treat them as fully undefined. This is essential for software compatibility with current and future processors. When a pin is marked as a "NC" or "RES" it is important to not connect any other signals to such pins to ensure proper operation. Intel strongly recommends following the guidelines below:

1. Do not depend on the states of any undefined bits when testing the values of defined register. Mask them out when testing.
2. Do not depend on the states of any undefined bits when storing them to memory or another register.
3. Do not depend on the ability to retain information written into any undefined bits.
4. When loading registers always load the undefined bits as zeros.
5. Never connect signals to device pins marked "NC" or "RES".
6. **INC** pins are Internal No-Connects. This means that the pin is not connected to the processor internally.

2.0 PINOUT

2.1. 120/133-MHz Pentium® OverDrive® Processor

2.1.1. 273-PGA PIN PINOUT

The 120/133-MHz Pentium OverDrive processor has a 273-pin PGA pinout and designed to be installed into Socket 4. See Section 6.3. for more details on Socket 4.

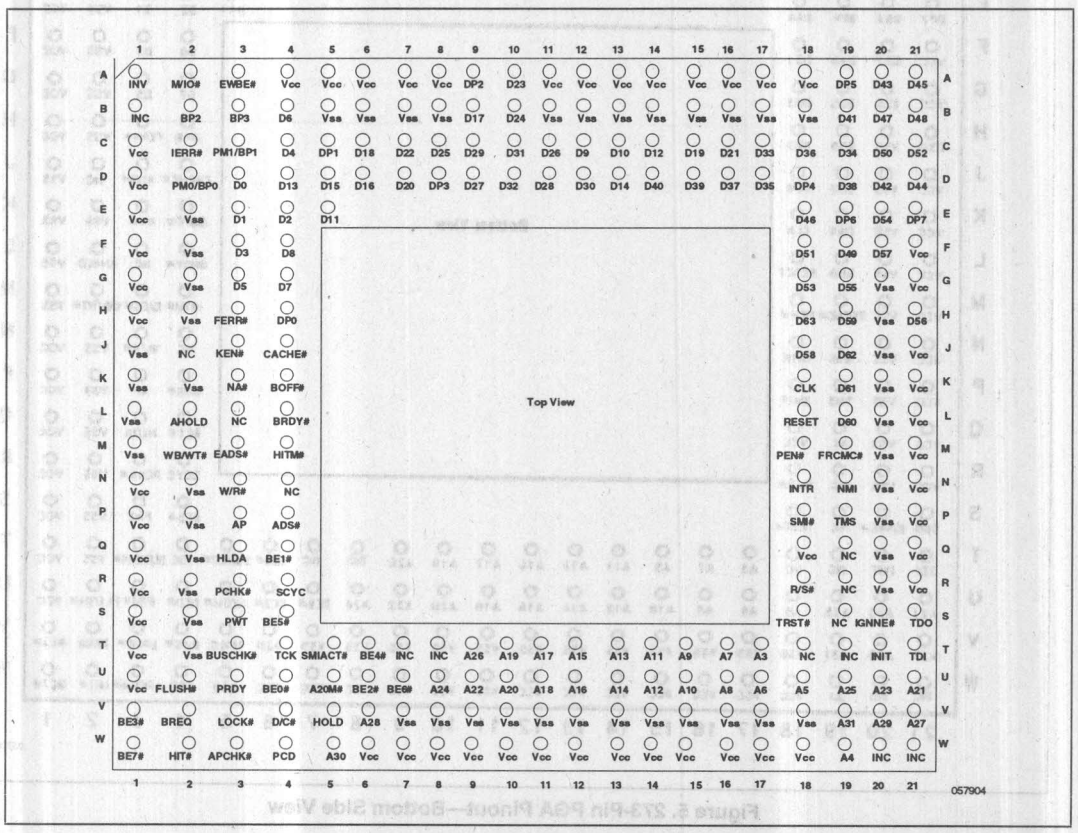


Figure 4. 273-Pin PGA Pinout—Top Side View

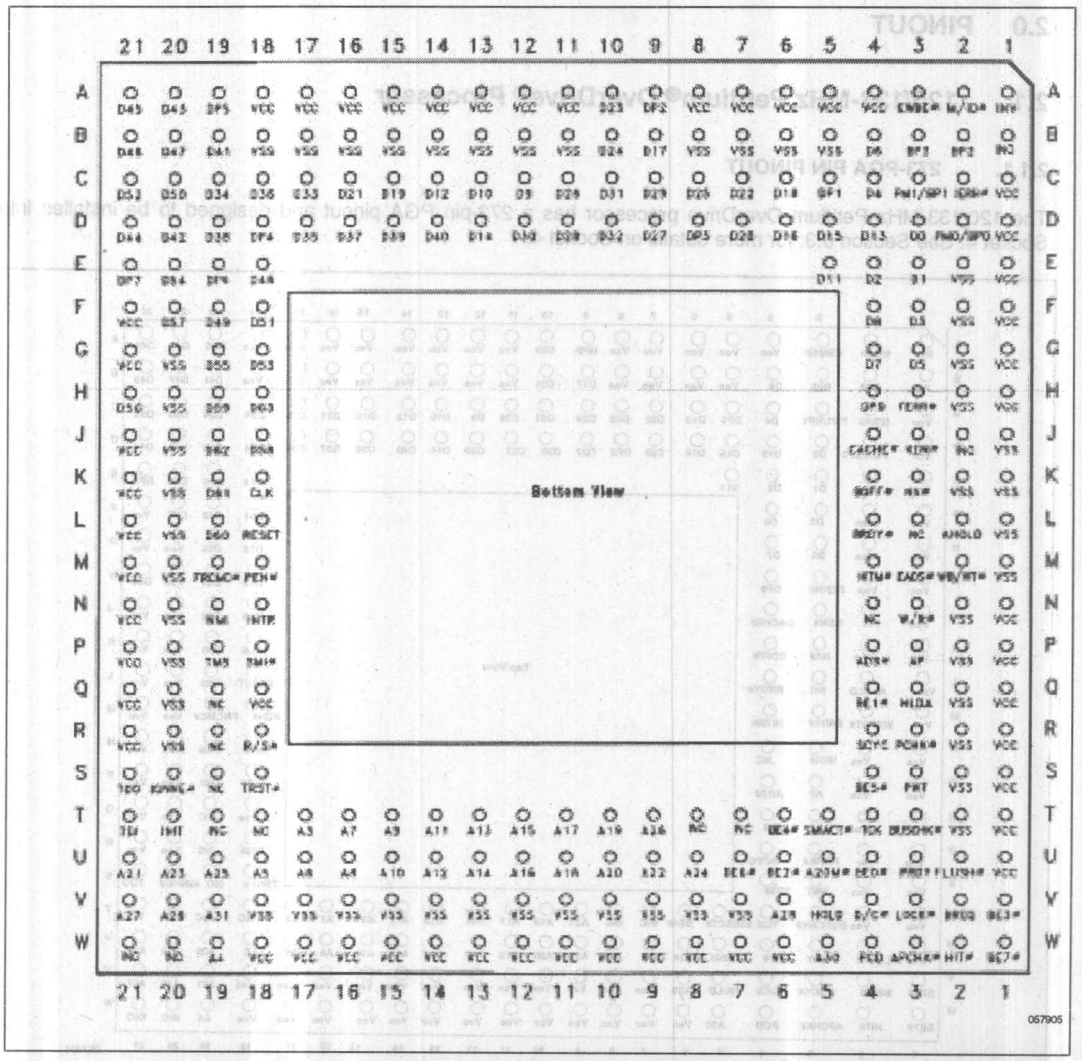


Figure 5. 273-Pin PGA Pinout—Bottom Side View

2.1.2. PIN CROSS REFERENCE

Table 1. 273-Pin PGA Pin Cross Reference Table by Pin Name

Address									
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
A3	T17	A9	T15	A15	T12	A21	U21	A27	V21
A4	W19	A10	U15	A16	U12	A22	U09	A28	V06
A5	U18	A11	T14	A17	T11	A23	U20	A29	V20
A6	U17	A12	U14	A18	U11	A24	U08	A30	W05
A7	T16	A13	T13	A19	T10	A25	U19	A31	V19
A8	U16	A14	U13	A20	U10	A26	T09		
Data									
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
D0	D03	D13	D04	D26	C11	D38	D19	D51	F18
D1	E03	D14	D13	D27	D09	D39	D15	D52	C21
D2	E04	D15	D05	D28	D11	D40	D14	D53	G18
D3	F03	D16	D06	D29	C09	D41	B19	D54	E20
D4	C04	D17	B09	D30	D12	D42	D20	D55	G19
D5	G03	D18	C06	D30	D12	D43	A20	D56	H21
D6	B04	D19	C15	D31	C10	D44	D21	D57	F20
D7	G04	D20	D07	D32	D10	D45	A21	D58	J18
D8	F04	D21	C16	D33	C17	D46	E18	D59	H19
D9	C12	D22	C07	D34	C19	D47	B20	D60	L19
D10	C13	D23	A10	D35	D17	D48	B21	D61	K19
D11	E05	D24	B10	D36	C18	D49	F19	D62	J19
D12	C14	D25	C08	D37	D16	D50	C20	D63	H18

[illegible]	[illegible]	DP1	C05	IV*	B01	WB/WT#	M02
BE0#	U04	DP2	A9	KEN#	J03	W/R#	N03
BE1#	Q04	DP3	D08	LOCK#	V03		
BE2#	U06	DP4	D18	M/IO#	A02		
BE3#	V01	DP5	A19	NA#	K03		
BE4#	T06	DP6	E19	NMI	N19		
BE5#	S04	DP7	E21	PCD	W04		
BE6#	U07	EADS#	M03	PCHK#	R03		
BE7#	W01	EWBE#	A03	PEN#	M18		
BOFF#	K04	FERR#	H03	PM0/BP0	D02		
BP2	B02	FLUSH#	U02	PM1/BP1	C03		
BP3	B03	FRCMC# **	M19	PRDY	U03		
BRDY#	L04	HIT#	W02	PWT	S03		
BREQ	V02	HITM#	M04	RESET	L18		
BT0*	T08	HLDA	Q03	R/S#	R18		
BT1*	W21	HOLD	V05	SCYC	R04		
BT2*	T07	IBT*	T19	SMI#	P18		
BT3*	W20	IERR#	C02	SMIACT#	T05		
BUSCHK#	T03	IGNNE#	S20	TCK	T04		

Table 1. 273-Pin PGA Pin Cross Reference Table by Pin Name (Continued)

Vcc									
A04	A11	A16	E01	J21	N21	Q21	U01	W10	W15
A05	A12	A17	F01	K21	P01	R01	W06	W11	W16
A06	A13	A18	G01	L21	P21	R21	W07	W12	W17
A07	A14	C01	G21	M21	Q01	S01	W08	W13	W18
A08	A15	D01	H01	N01	Q18	T01	W09	W14	
Vss									
B05	B13	E02	J01	L20	P20	T02	V12	V18	
B06	B14	F02	J20	M01	Q02	V07	V13		
B07	B15	G02	K01	M20	Q20	V08	V14		
B08	B16	G20	K02	N02	R02	V09	V15		
B11	B17	H02	K20	N20	R20	V10	V16		
B12	B18	H20	L01	P02	S02	V11	V17		
NC									
L03	N04	Q19	R19	S19	T18				

NOTES:

* These signal pins are not supported by the 120/133-MHz Pentium® OverDrive® processor and are Internal No-Connects (INC).

** This signal is not supported by the 120/133-MHz Pentium OverDrive processor.

2.2. Pentium® OverDrive® Processors Quick Pin Reference

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, Pentium® OverDrive® processor emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the Pentium OverDrive processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A3.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the Pentium OverDrive processor.
ADSC#	O	ADSC# is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium OverDrive processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium OverDrive processor with even parity information on all the Pentium OverDrive processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium OverDrive processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium OverDrive processor.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium OverDrive processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	The APIC is not supported by the Pentium OverDrive processor.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).
[BF] [BF1]	I	**Bus Frequency** determines the bus-to-core frequency ratio on the Pentium processor. BF is an Internal No Connect on the Pentium OverDrive processor. The 120/133-MHz Pentium OverDrive processor has a preset bus fraction of 2/1 core/bus ratio.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium OverDrive processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium OverDrive processor restarts the aborted bus cycle(s) in their entirety.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium OverDrive processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	This signal has the same functionality as BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium OverDrive processor has internally generated a bus request. This signal is always driven whether or not the Pentium OverDrive processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium OverDrive processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium OverDrive processor will vector to the machine check exception.
CACHE#	O	For Pentium OverDrive processor-initiated cycles the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium OverDrive processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the Pentium OverDrive processor. The clock frequency is the operating frequency of the Pentium OverDrive processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK.
CPUTYP	I	**CPUTYP** is internally tied to V_{SS} and is a Internal No-Connect (INC) to the package pin on the Pentium OverDrive processor.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	**D/P#** is a Internal No-Connect (INC) to the package pin on the Pentium OverDrive processor.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by Pentium OverDrive processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium OverDrive processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium OverDrive processor. DP7 applies to D63-D56, DP0 applies to D7-D0.
[DPEN#]	I/O	The Pentium OverDrive processor does not support dual processing.
PICD0		
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium OverDrive processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium OverDrive processor generates a write, and EWBE# is sampled inactive, the Pentium OverDrive processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel 387 math coprocessor. FERR# is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the Pentium OverDrive processor to writeback all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium OverDrive processor indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
FRCMC#	I	The Pentium OverDrive processor does not support functional redundancy checking.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either Pentium OverDrive processor data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium OverDrive processor cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium OverDrive processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and Pentium OverDrive processor will resume driving the bus. If the Pentium OverDrive processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
HOLD	I	In response to the **bus hold request**, Pentium OverDrive processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium OverDrive processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium OverDrive processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium OverDrive processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium OverDrive processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium OverDrive processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium OverDrive processor will stop execution and wait for an external interrupt.
INIT	I	The Pentium OverDrive processor **initialization** input pin forces the Pentium OverDrive processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the Pentium OverDrive processor will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium OverDrive processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium OverDrive processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium OverDrive processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back to back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium OverDrive processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium OverDrive processor supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PBGNT#	I/O	The Pentium OverDrive processor does not support dual processing.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium OverDrive processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium OverDrive processor will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	The Pentium OverDrive processor does not support dual processing.
PHITM#	I/O	The Pentium OverDrive processor does not support dual processing.
PICCLK	I	The Pentium OverDrive processor does not support dual processing.
PICD0-1 [DPEN#] [APICEN]	I/O	The Pentium OverDrive processor does not support dual processing.
PBREQ#	I/O	The Pentium OverDrive processor does not support dual processing.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the Page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external writeback indication on a page by page basis.
R/S#	I	The **run/stop** input is an asynchronous, edge sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	**RESET** forces the Pentium OverDrive processor to begin execution at a known state. All Pentium OverDrive processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH#, and INIT are sampled when RESET transitions from high to low to determine if tristate test mode mode will be entered, or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode (SMM).
TCK	I	The **testability clock** input provides the clocking function for the Pentium OverDrive processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium OverDrive processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium OverDrive processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of Pentium OverDrive processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC}	I	The 120/133-MHz Pentium OverDrive processor has 52 5V **power** inputs.
V_{SS}	I	The 120/133-MHz Pentium OverDrive processor has 49 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line by line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

NOTE:
Highlighted items in Table 2 are signals not supported the Pentium® OverDrive® processor s.

2.3. Pentium® OverDrive® Processor Pin Descriptions

2.3.1. INPUT PINS

Table 3. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2,T12,T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2,T12,T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK

Table 3. Input Pins (Continued)

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

NOTE:
Highlighted signals are original Pentium® processor 75/90/100 MHz signals and are not supported by the Pentium OverDrive® processors.

2.3.2. OUTPUT PINS

Table 4. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
BT3-BT0	n/a	
CACHE#	Low	Bus Hold, BOFF#
D/P#	n/a	
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IBT	n/a	
IERR#	Low	
IU	n/a	
IV	n/a	
LOCK#	Low	Bus Hold, BOFF#
M/IO# , D/C# , W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:
All output pins are floated during tristate test mode (except TDO).
Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processors.

2.3.3. INPUT/OUTPUT PINS

Table 5. Input/Output Pins

Name	Active Level	When Floated	Qualified (When an Input)	Internal Resistor
A31-A3	n/a	Address hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTES:
All input/output pins are floated during tristate test.
Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processors.

Table 6. Interprocessor I/O Pins

Name	Active Level	Internal Resistor
PHIT#	n/a	Pullup
PHITM#	n/a	Pullup
PBGNT#	n/a	Pullup
PBREQ#	n/a	Pullup

NOTE:
Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processors.

2.3.4. PIN GROUPING ACCORDING TO FUNCTION

Table 7 organizes the pins with respect to their function.

Table 7. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT
Address Bus	A31-A3, BE7# - BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

3.1. Core to Bus Ratio for Higher Speed

The Pentium OverDrive processors incorporate an internal Phase Lock Loop (PLL) and clock multiplier to generate the higher internal speeds. This allows the internal processor core to operate at higher frequencies than the external bus.

On the 120/133-MHz Pentium OverDrive processor, the core/bus ratio will be preset to 2/1.

Table 9. Core/Bus Frequency on the Pentium® OverDrive® Processor

Pentium® OverDrive® Processor Internal Speed	Bus Speed	Replaces (Core/Bus)
120-MHz	60-MHz	60-MHz
133-MHz	66-MHz	66-MHz

3.2. Processor Initialization

3.2.1. POWER UP SPECIFICATION

The Pentium OverDrive processors will boot like the respective original Pentium processors. **If the Pentium OverDrive processor is installed in a second socket of dual socket system the primary CPU must be removed or the system will not boot properly.**

3.2.2. TEST AND CONFIGURATION FEATURES (BIST, FRC, TRISTATE TEST MODE)

The Pentium OverDrive processors execute the Built In Self Test (BIST) and Tristate Test Mode same as the respective original Pentium processor. Functional Redundancy Checking is not supported.

3.2.3. INITIALIZATION WITH RESET, INIT AND BIST

The Pentium OverDrive processors handling of RESET, INIT, and the Built In Self Test (BIST) is the same as the original Pentium processors. The register states after RESET, INIT, and BIST are same as the original Pentium processors. For further information refer to Section 8.0. in this datasheet.

Table 10. EAX Bit Values Definition for CPUID

CPU	31...14	13...12	11...8	7...4	3...0
Field Definition	(reserved)	type	family	model	stepping
Pentium® Processor (60, 66-MHz) and 120/133-Mhz Pentium OverDrive® Processor	(reserved)	Table 11	5H	1H	A to F

Table 11. EAX Bit Values Definition for Processor Type

Bit 13	Bit 12	Processor Type
0	0	Primary Pentium® Processor
0	0	120/133-MHz Pentium OverDrive® Processor
0	1	Future Pentium OverDrive Processor
1	0	Dual Pentium Processor *
1	1	Reserved

NOTE:
* Pentium® OverDrive® processor s do not support Dual Processing mode.

3.3. CPUID

The CPUID instruction allows software to determine the type and features of the microprocessor. When executing the CPUID instruction the Pentium OverDrive processors behaves like the original Pentium processors:

- If the value in EAX is '0' then the 12-byte ASCII string "GenuineIntel" (little endian) is returned in EBX, EDX, and ECX. Also, a '1' is returned in EAX.
- If the value in EAX is '1' then the processor version is returned in EAX and the processor capabilities are returned in EDX. The values of EAX and EDX for the Pentium OverDrive processors are given below.
- If the value in EAX is neither '0' nor '1', the Pentium OverDrive processors writes '0' to all registers or is undefined.

The following EAX and EDX values are defined for the CPUID instruction executed with EAX = '1'.

The stepping fields has the same format as the original Pentium processor's and will be the same for the Pentium OverDrive processors. The 120/133-MHz Pentium OverDrive processor will have the same CPUID as the original Pentium processor 051xH. The type field is defined in Table 11.

3.4. On-Package Fan/Heatsink

The on-package fan/heatsink included with the Pentium OverDrive processors requires different stress ratings than the original Pentium processor. The fan is a detachable unit, and the storage temperature is stated separately in Table 13. Operation of the Pentium OverDrive processor is defined at T_A = 0°C to 45°C. The fan/heatsink is shown in Figure 6.

3.5. On-Package Voltage Regulator

The 120/133-MHz Pentium OverDrive processor has an on-package voltage regulator that converts the 5 volts from the system baseboard into the 3.3 volts required by the core.

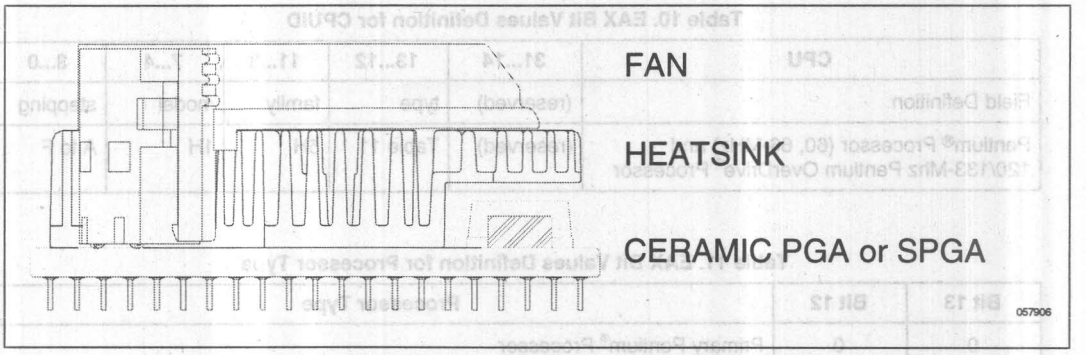


Figure 6. Pentium® OverDrive® Processor with Fan/Heatsink

3.6. Cache Support

The Pentium OverDrive processors have the same intergrated caches as their respective original Pentium processor; 8K-byte data cache and 8K byte code cache. The 120/133-MHz Pentium OverDrive processor supports the Intel 82430 PCI chip set but does not support the 82496 cache controller and 82491 cache SRAM chip set.

3.7. I/O Buffers

The Pentium OverDrive processor buffer models comply with the specifications for the buffer model for the respective original Pentium processor. The circuit topology is the same and the ranges of values in the Pentium OverDrive processor model are within the original Pentium processor ranges. The buffer models used by the Pentium OverDrive processors accurately model flight time and signal quality.

3.8. Test Register Access on the Pentium® OverDrive® Processor

The Pentium OverDrive processors have test registers which allow testing of different areas of the processor. These test registers are called Model Specific Registers (MSR). These MSR's are accessed using the RDMSR and WRMSR instructions. This is true for both Pentium OverDrive processors. The 120/133-MHz Pentium OverDrive processor uses special bus cycles for execution tracing and does not have pins IU, IV, and IBT used by the original Pentium processor.

4.0 BIOS AND SOFTWARE

The Pentium OverDrive processors are drop-in replacements for the respective original Pentium processor. BIOS changes are not normally necessary but might be required. Please call Intel Technical Support hotline if assistance is required. The Pentium OverDrive processors are 100% backward software compatible with their respective original Pentium processors.

5.0 ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium OverDrive processors and their respective original Pentium processor

5.1. Power and Ground

For proper internal on-chip power distribution, the 120/133-MHz Pentium OverDrive processor in the PGA package has 52 V_{CC} (power) and 49 V_{SS} (ground) inputs. Power and ground connections must

be made to all external V_{CC} and V_{SS} pins of the 120/133-MHz Pentium OverDrive processor. On the circuit board all V_{CC} pins must be connected to a 5V V_{CC} plane. The 120/133-MHz Pentium OverDrive processor has an on-package voltage regulator that converts the 5V input voltage to 3.3V for the core.

5.2. Pentium® OverDrive® Processor Decoupling Recommendations

Decoupling recommendation for the original Pentium processor apply to the Pentium OverDrive processor upgradable systems and capacitors should be placed near the Pentium OverDrive processor. The Pentium OverDrive processors can cause transient power surges, particularly when driving large capacitive loads. The Pentium OverDrive processors are shipped with adequate decoupling capacitors on the package to limit transients in excess of Pentium processors tolerance. It is recommended to follow the original Pentium processor specification for decoupling recommendations.

5.3. Other Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground. All NC pins must remain unconnected.

5.4. Absolute Maximum Ratings

Tables in this section provides environmental stress ratings for the Pentium OverDrive processors. Functional operation at the absolute maximum and minimum is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability. Furthermore, precautions should be taken to avoid high static voltages and electric fields to prevent static electric discharge. Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. The tables contain stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.

5.4.1. 120/133-MHZ Pentium® OverDrive® PROCESSOR

Table 12. Absolute Maximum Rating without Fan/Heatsink

Storage temperature	-40°C to 125°C
Case temperature under bias	-40°C to 110°C
Voltage on any pin with respect to ground	-0.5 V to V_{CC} + 0.5 (V)
Supply voltage with respect to V_{SS}	-0.5V to +6.5V
5V Safe Buffer DC Input Voltage	–0.5V to 6.5V (1)

NOTE:
1. See overshoot/undershoot transient specification in the *Pentium® Family User's Manual, Volume 1.*

Table 13. Absolute Maximum Ratings for Fan/Heatsink Only

	Parameter	Min	Max	Unit	Notes
Fan:					
	Storage Temperature	-30	75	° C	
	Case Temperature Under Bias	0	70	° C	
V_{CC5}	5V Fan Supply Voltage with Respect to V_{SS}	-0.5	6.5	V	

5.5. D.C. Specifications

5.5.1. 120/133-MHZ Pentium® OverDrive® PROCESSOR D.C. SPECIFICATIONS

Table 14 lists the D.C. specifications associated with the 120/133-MHz Pentium OverDrive processor.

Table 14. 120/133-MHz Pentium® OverDrive® Processor D.C. Specifications

V_{CC} = See Notes (9), (10); T_A = 0 to 45°C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	-0.3	+0.8	V	TTL Level
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V	TTL Level
V_{OL}	Output Low Voltage		0.45	V	TTL Level (1)
V_{OH}	Output High Voltage	2.4		V	TTL Level (2)
I_{CC}	Power Supply Current		3200 2900	mA mA	66 MHz, (6), (7) 60 MHz, (6), (8)
I_{LI}	Input Leakage Current		±15	uA	$0 \le V_{IN} \le V_{CC}$, (3)
I_{LO}	Output Leakage Current		±15	uA	$0 \le V_{OUT} \le V_{CC}$ Tristate , (3)
I_{IL}	Input Leakage Current		-400	uA	V_{IN} = 0.45V, (4)
I_{IH}	Input Leakage Current		200	uA	V_{IN} = 2.4V, (5)
C_{IN}	Input Capacitance		15	pF	
C_O	Output Capacitance		20	pF	
$C_{I/O}$	I/O Capacitance		25	pF	
C_{CLK}	CLK Input Capacitance		8	pF	
C_{TIN}	Test Input Capacitance		15	pf	
C_{TOUT}	Test Output Capacitance		20	pf	
C_{TCK}	Test Clock Capacitance		8	pf	

NOTES:

1. Parameter measured at 4 mA load.
2. Parameter measured at 3 mA load.
3. This parameter is for input without pullup or pulldown.
4. This parameter is for input with pullup.
5. This parameter is for input with pulldown.
6. Worst case average I_{CC} for a mix of test patterns.
7. (16 W max.) Typical Pentium® processor supply current is 2600 mA (13 W) at 66 MHz BUS.
8. (14.6 W max.) Typical Pentium processor supply current is 2370 mA (11.9 W) at 60 MHz BUS.
9. V_{CC} = 5V ± 5% at 60 MHz.
10. V_{CC} = 4.90V to 5.40V at 66 MHz.

5.6. A.C. Specifications

5.6.1. 120/133-MHZ Pentium® OverDrive® PROCESSOR A.C. SPECIFICATIONS

5.6.1.1. A.C. Tables for a 60-MHz Bus

The 60-MHz and 66-MHz Bus A.C. specifications given in Table 15 and Table 16 consist of output delays, input setup requirements, and input hold requirements. All A.C. specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct processor operation.

Care should be taken to read all notes associated with a particular timing parameter. In addition, the following list of notes apply to the timing specification tables in general and are not associated with any one timing: 2, 5, 6, and 14.

Table 15. 120/133-MHz Pentium® OverDrive® Processor (60-MHz Bus) A.C. Specifications

V_{CC} = 5V ± 5%; T_A = 0 to 45°C; C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	33.33	60	MHz		MAX. CORE FREQ=120 MHz @ 1/2
t_1	CLK Period	16.67		nS	7	
t_{1a}	CLK Period Stability		±250	pS		(18), (19), (20), (21)
t_2	CLK High Time	4		nS	7	@2V, (1)
t_3	CLK Low Time	4		nS	7	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-2.0V), (1)
t_6	ADS#, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Valid Delay	1.5	9.0	nS	8	
t_{6a}	AP Valid Delay	1.5	10.5	nS	8	
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		11	nS	9	(1)
t_8	PCHK#, APCHK#, IERR#, FERR# Valid Delay	1.5	9.3	nS	8	(4)
t_9	BREQ, HLDA, SMIACT# Valid Delay	1.5	9.0	nS	8	(4)
t_{10}	HIT#, HITM# Valid Delay	1.5	9.0	nS	8	
t_{11}	PM0-1, BP0-3 Valid Delay	1.5	11	nS	8	
t_{11a}	PRDY Valid Delay	1.5	9.0	nS	8	
t_{12}	D0-D63,DP0-7 Write Data Valid Delay	1.5	10	nS	8	
t_{13}	D0-D63,DP0-7 Write Data Float Delay		11	nS	9	(1)

Table 15. 120/133-MHz Pentium® OverDrive® Processor (60-MHz Bus) A.C. Specifications (Continued)

V_{CC} = 5V ± 5%; T_A = 0 to 45°C; C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{14}	A5-A31 Setup Time	7		nS	10	
t_{15}	A5-A31 Hold Time	1.5		nS	10	
t_{16}	EADS#, INV, AP Setup Time	5.5		nS	10	
t_{17}	EADS#, INV, AP Hold Time	1.5		nS	10	
t_{18}	KEN#, WB/WT# Setup Time	5.5		nS	10	
t_{18a}	NA# Setup Time	5.0		nS	10	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.5		nS	10	
t_{20}	BRDY# Setup Time	5.5		nS	10	
t_{21}	BRDY# Hold Time	1.5		nS	10	
t_{22}	AHOLD, BOFF# Setup Time	6		nS	10	
t_{23}	AHOLD, BOFF# Hold Time	1.5		nS	10	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.5		nS	10	
t_{25}	BUSCHK#, EWBE#, HOLD, PEN# Hold Time	1.5		nS	10	
t_{26}	A20M#, INTR, Setup Time	5.5		nS	10	(12), (16)
t_{27}	A20M#, INTR, Hold Time	1.5		nS	10	(13)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.5		nS	10	(16), (17)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.5		nS	10	
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2		CLKs		(15), (17)
t_{31}	R/S# Setup Time	5.5		nS	10	(12), (16), (17)
t_{32}	R/S# Hold Time	1.5		nS	10	(13)
t_{33}	R/S# Pulse Width, Async.	2		CLKs		(15), (17)
t_{34}	D0-D63 Read Data Setup Time	4.3		nS	10	
t_{34a}	DP0-7 Read Data Setup Time	4.3		nS	10	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2		nS	10	
t_{36}	RESET Setup Time	5.5		nS	11	(11), (12), (16)
t_{37}	RESET Hold Time	1.5		nS	11	(11), (13)

Table 15. 120/133-MHz Pentium® OverDrive® Processor (60-MHz Bus) A.C. Specifications (Continued)

V_{CC} = 5V ± 5%; T_A = 0 to 45°C; C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	11	(11)
t_{39}	RESET Active After V_{CC} & CLK Stable	1		mS	11	power up, (11)
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.5		nS	11	(12), (16), (17)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.5		nS	11	(13)
t_{42}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2		CLKs	11	(16)
t_{43}	Reset Configuration Signals (INIT, FLUSH#) Hold Time, Async.	2		CLKs	11	
t_{44}	TCK Frequency	—	16	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25		nS	7	@2V, (1)
t_{47}	TCK Low Time	25		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40		nS	13	(1), Async
t_{51}	TDI, TMS Setup Time	5		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13		nS	12	(7)
t_{53}	TDO Valid Delay	3	20	nS	12	(8)
t_{54}	TDO Float Delay		25	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3	20	nS	12	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25	nS	12	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13		nS	12	(3), (7), (10)

5.6.1.2. A.C. Tables for a 66-MHz Bus

Table 16. 120/133-MHz Pentium® OverDrive® Processor (66-MHz Bus) A.C. Specifications

V_{CC} = 4.90V to 5.40V; T_A = 0 to 45°C; C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	33.33	66.66	MHz		MAX. CORE FREQ= 133 MHz @ 1/2
t_1	CLK Period	15		nS	9	
t_{1a}	CLK Period Stability		±250	pS		(18), (19), (20), (21)
t_2	CLK High Time	4		nS	9	@2V, (1)
t_3	CLK Low Time	4		nS	9	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	9	(2.0V-0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	9	(0.8V-2.0V), (1)
t_6	ADS#, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Valid Delay	1.5	8.0	nS	10	
t_{6a}	AP Valid Delay	1.5	9.5	nS	10	
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10	nS	11	(1)
t_8	PCHK#, APCHK#, IERR#, FERR# Valid Delay	1.5	8.3	nS	10	(4)
t_9	BREQ, HLDA, SMIACT# Valid Delay	1.5	8.0	nS	10	(4)
t_{10}	HIT#, HITM# Valid Delay	1.5	8.0	nS	10	
t_{11}	PM0-1, BP0-3 Valid Delay	1.5	10	nS	10	
t_{11a}	PRDY Valid Delay	1.5	8.0	nS	10	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.5	9	nS	10	
t_{13}	D0-D63, DP0-7 Write Data Float Delay		10	nS	11	(1)
t_{14}	A5-A31 Setup Time	6.5		nS	12	
t_{15}	A5-A31 Hold Time	1.5		nS	12	
t_{16}	EADS#, INV, AP Setup Time	5		nS	12	
t_{17}	EADS#, INV, AP Hold Time	1.5		nS	12	
t_{18}	KEN#, WB/WT# Setup Time	5		nS	12	
t_{18a}	NA# Setup Time	4.5		nS	12	

Table 16. 120/133-MHz Pentium® OverDrive® Processor (66-MHz Bus) A.C. Specifications (Continued)

V_{CC} = 4.90V to 5.40V; T_A = 0 to 45°C; C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.5		nS	12	
t_{20}	BRDY# Setup Time	5		nS	12	
t_{21}	BRDY# Hold Time	1.5		nS	12	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	12	
t_{23}	AHOLD, BOFF# Hold Time	1.5		nS	12	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5		nS	12	
t_{25}	BUSCHK#, EWBE#, HOLD, PEN# Hold Time	1.5		nS	12	
t_{26}	A20M#, INTR, Setup Time	5		nS	12	(12), (16)
t_{27}	A20M#, INTR, Hold Time	1.5		nS	12	(13)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5		nS	12	(16), (17)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.5		nS	12	
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2		CLKs		(15), (17)
t_{31}	R/S# Setup Time	5		nS	12	(12), (16), (17)
t_{32}	R/S# Hold Time	1.5		nS	12	(13)
t_{33}	R/S# Pulse Width, Async.	2		CLKs		(15), (17)
t_{34}	D0-D63 Read Data Setup Time	3.8		nS	12	
t_{34a}	DP0-7 Read Data Setup Time	3.8		nS	12	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2		nS	12	
t_{36}	RESET Setup Time	5		nS	13	(11), (12), (16)
t_{37}	RESET Hold Time	1.5		nS	13	(11), (13)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	13	(11)
t_{39}	RESET Active After V_{CC} & CLK Stable	1		mS	13	power up, (11)
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5		nS	13	(12), (16), (17)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.5		nS	13	(13)

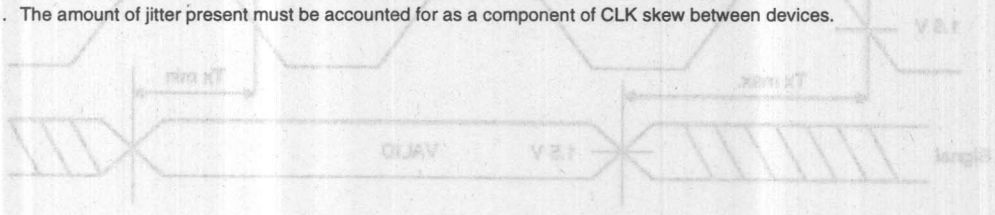
Table 16. 120/133-MHz Pentium® OverDrive® Processor (66-MHz Bus) A.C. Specifications (Continued)

V_{CC} = 4.90V to 5.40V; T_A = 0 to 45°C; C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{42}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2		CLKs	13	(16)
t_{43}	Reset Configuration Signals (INIT, FLUSH#) Hold Time, Async.	2		CLKs	13	
t_{44}	TCK Frequency	—	16	MHz		
t_{45}	TCK Period	62.5		nS	9	
t_{46}	TCK High Time	25		nS	9	@2V, (1)
t_{47}	TCK Low Time	25		nS	9	@0.8V, (1)
t_{48}	TCK Fall Time		5	nS	9	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5	nS	9	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40		nS	15	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5		nS	14	(7)
t_{52}	TDI, TMS Hold Time	13		nS	14	(7)
t_{53}	TDO Valid Delay	3	20	nS	14	(8)
t_{54}	TDO Float Delay		25	nS	14	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3	20	nS	14	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25	nS	14	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5		nS	14	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13		nS	14	(3), (7), (10)

NOTES:

Notes 2, 5, 6, and 14 are general and apply to all timing specified.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/ns rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 16 MHz.
10. During probe mode operation, use the normal specified timings. Do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Pentium® OverDrive® processor timing not applicable to FRCMC#.
12. Setup time is required to guarantee recognition on a specific clock.
13. Hold time is required to guarantee recognition on a specific clock.
14. All TTL timings are referenced from 1.5 V.
15. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
16. This input may be driven asynchronously.
17. When driven asynchronously, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
18. Functionality is guaranteed by design/characterization.
19. Measured on rising edge of adjacent CLKs at 1.5V.
20. To ensure a 1:1 relationship between the magnitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. If this occurs, I/O timings are degraded by twice the jitter component within this frequency range. For example, if 15% of the jitter energy is within this range degrade I/O timings by 2 X 0.15 X magnitude of jitter.
21. The amount of jitter present must be accounted for as a component of CLK skew between devices.



5.6.2. TIMING AND WAVEFORMS

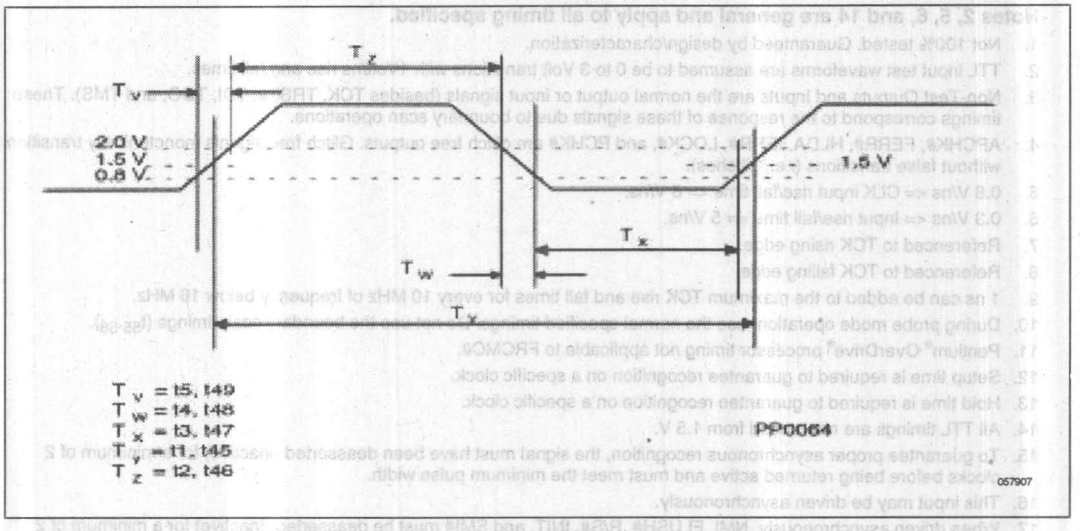


Figure 7. Clock Waveform

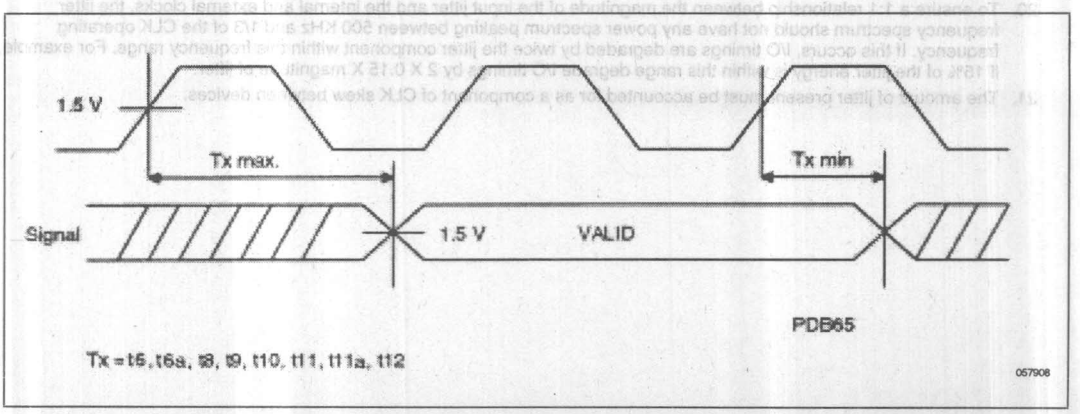


Figure 8. Valid Delay Timing

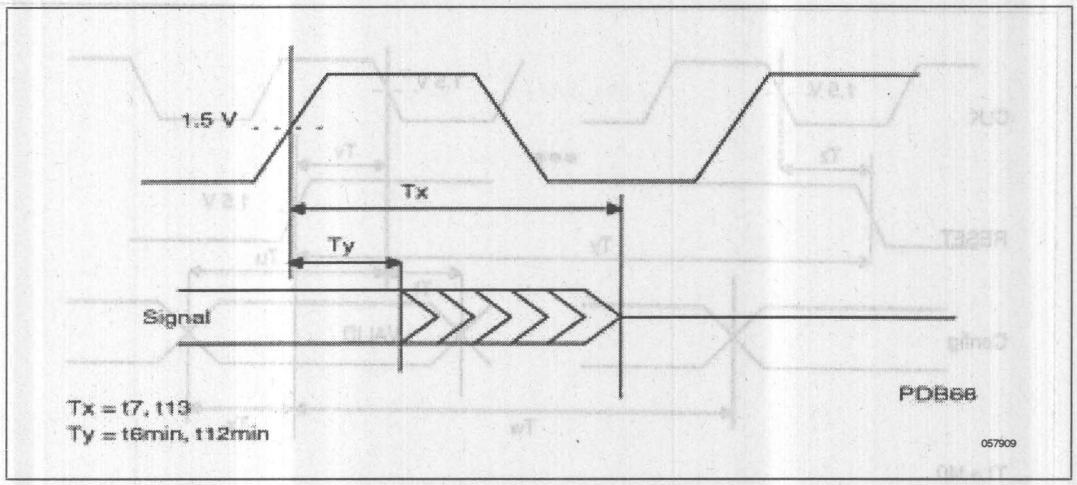


Figure 9. Float Delay Timing

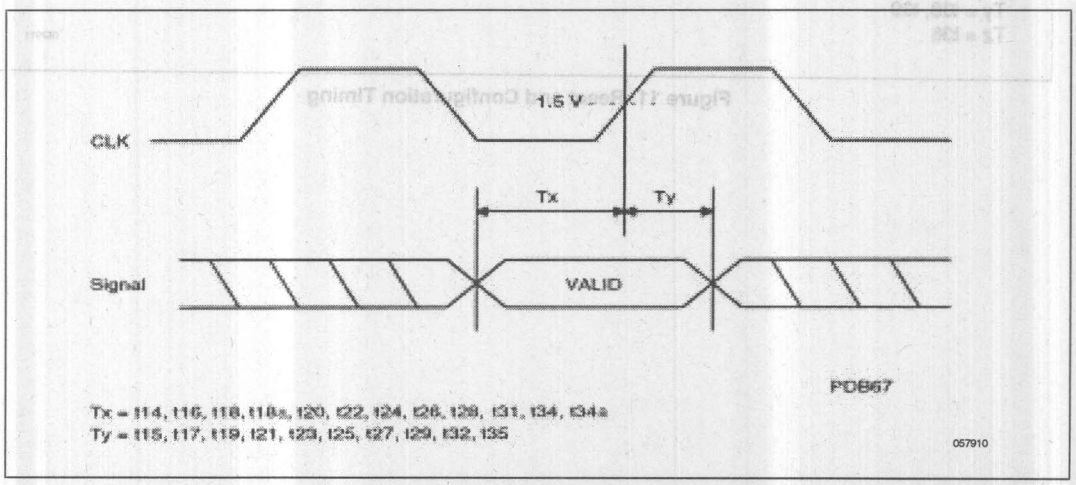


Figure 10. Setup and Hold Timing

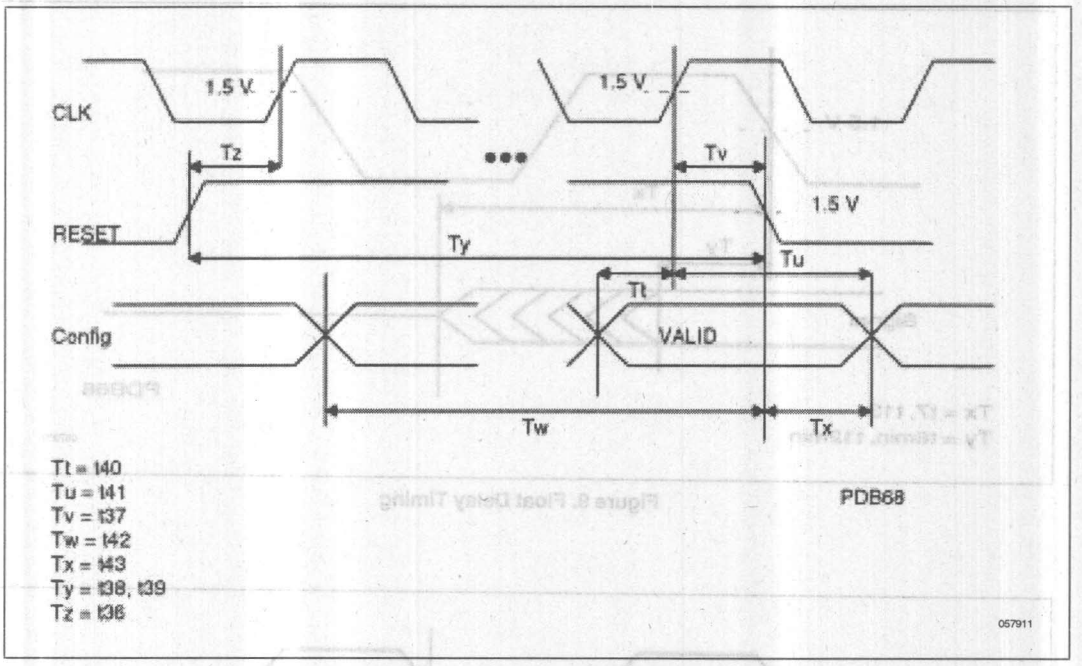


Figure 11. Reset and Configuration Timing

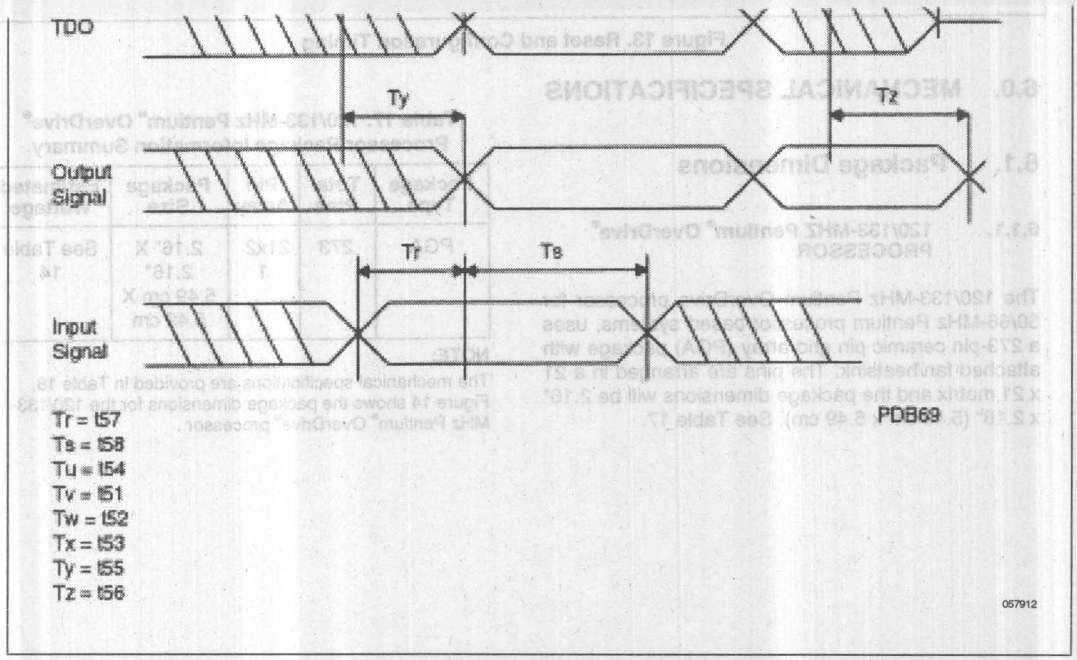


Figure 12. Test Timing

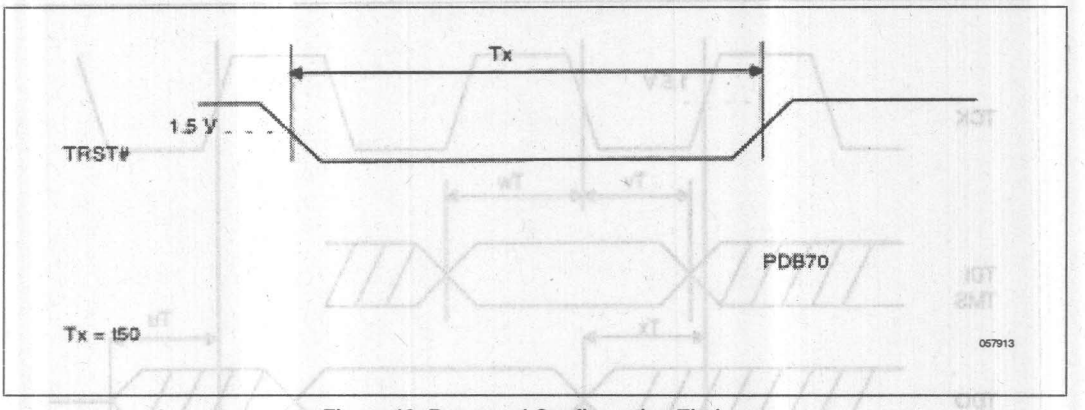


Figure 13. Reset and Configuration Timing

6.0. MECHANICAL SPECIFICATIONS

6.1. Package Dimensions

6.1.1. 120/133-MHZ Pentium® OverDrive® PROCESSOR

The 120/133-MHz Pentium OverDrive processor for 60/66-MHz Pentium processor-based systems, uses a 273-pin ceramic pin grid array (PGA) package with attached fan/heatsink. The pins are arranged in a 21 x 21 matrix and the package dimensions will be 2.16" x 2.16" (5.49 cm x 5.49 cm). See Table 17.

Table 17. 120/133-MHz Pentium® OverDrive® Processor Package Information Summary

Package Type	Total Pins	Pin Array	Package Size	Estimated Wattage
PGA	273	21x21	2.16" X 2.16" 5.49 cm X 5.49 cm	See Table 14

NOTE:
The mechanical specifications are provided in Table 18. Figure 14 shows the package dimensions for the 120/133-MHz Pentium® OverDrive® processor .

Table 18. 120/133-MHz Pentium® OverDrive® Processor Mechanical Specifications

Family: Ceramic Pin Grid Array Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A		33.98	Metal Lid		1.338	Metal Lid
A1	2.84	3.50	Metal Lid	0.112	0.138	Metal Lid
A2	0.33	0.43	Metal Lid	0.013	0.017	Metal Lid
A3	2.51	3.07		0.099	0.121	
A4		20.32			0.800	
A5	10.16			0.400		
B	0.43	0.51		0.017	0.020	
D	54.61	55.11		2.150	2.170	
D1	50.67	50.93		1.995	2.005	
E1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	273		273			
S1	1.65	2.16		0.065	0.065	

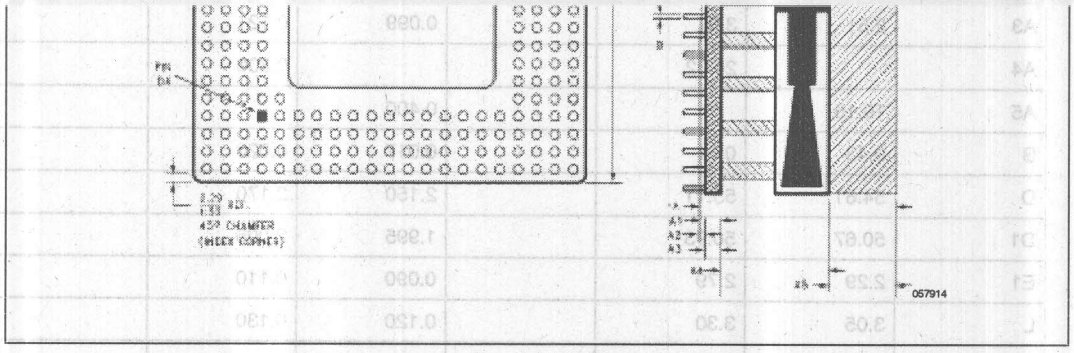


Figure 14. 120/133-MHz Pentium® OverDrive® Processor Package Dimensions

6.2. Spatial Requirements

Both the Pentium OverDrive processors employ a fan/heatsink thermal management device. Clearance requirements must be met around the fan/heatsink to ensure unimpeded air flow for proper cooling. Figure 15 shows the Pentium OverDrive processor's fan/heatsink space requirements.

The Pentium OverDrive processors have spatial requirements defined in the respective socket specification that must be met. As shown in Figure 16, it is acceptable to allow any device (i.e., add-in cards, surface mount device, chassis, etc.) to enter within the free space distance of 0.2" from the Pentium OverDrive processor (PGA or SPGA) package if it is not taller than the level of the heatsink base. In other words, if a component is taller than height "B," it cannot be closer to the Pentium OverDrive processor (PGA or SPGA) package than distance "A". This applies to three of the four sides of the Pentium OverDrive processor (PGA or SPGA) package, although the back and handle sides of a ZIF socket will generally automatically meet this specification since they have widths larger than distance "A." Compliance to this requirement will ensure systems can be upgraded to the respective Pentium OverDrive processor.

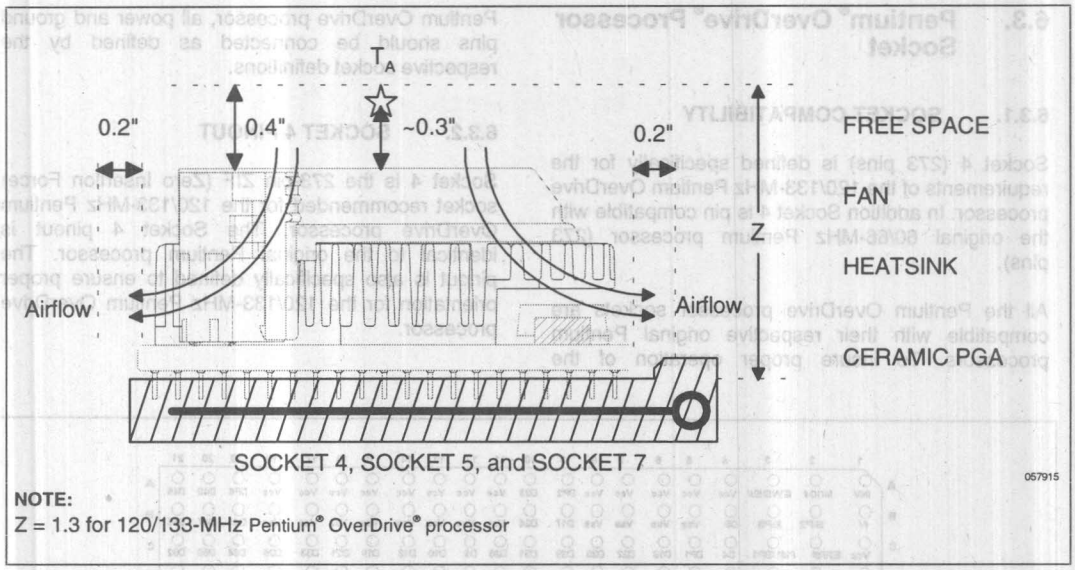


Figure 15. Illustrates Physical Space Requirements for the Pentium® OverDrive® Processors

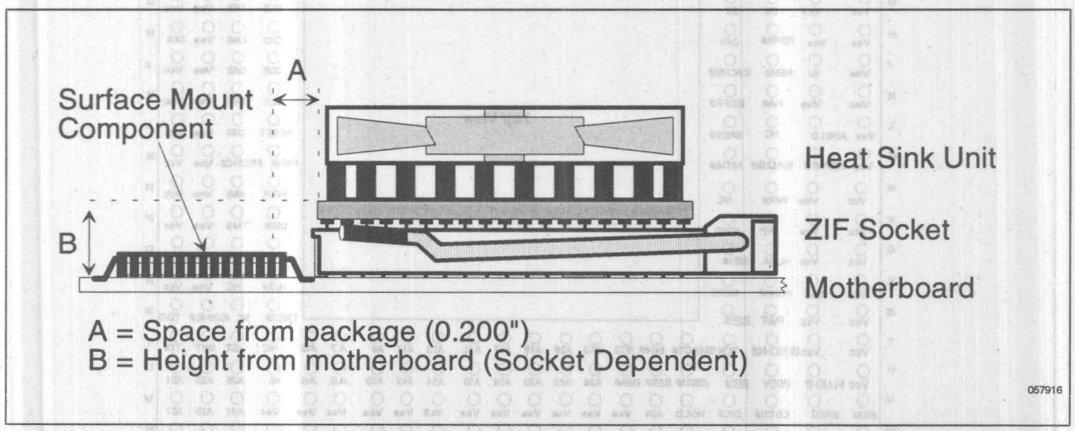


Figure 16. Required Free Space from Sides of PGA Package

6.3. Pentium® OverDrive® Processor Socket

6.3.1. SOCKET COMPATIBILITY

Socket 4 (273 pins) is defined specifically for the requirements of the 120/133-MHz Pentium OverDrive processor. In addition Socket 4 is pin compatible with the original 60/66-MHz Pentium processor (273 pins).

All the Pentium OverDrive processor sockets are compatible with their respective original Pentium processors. To insure proper operation of the Pentium OverDrive processor, all power and ground pins should be connected as defined by the respective socket definitions.

6.3.2. SOCKET 4 PINOUT

Socket 4 is the 273-pin ZIF (Zero Insertion Force) socket recommended for the 120/133-MHz Pentium OverDrive processor. The Socket 4 pinout is identical to the original Pentium processor. The pinout is also specifically defined to ensure proper orientation for the 120/133-MHz Pentium OverDrive processor.

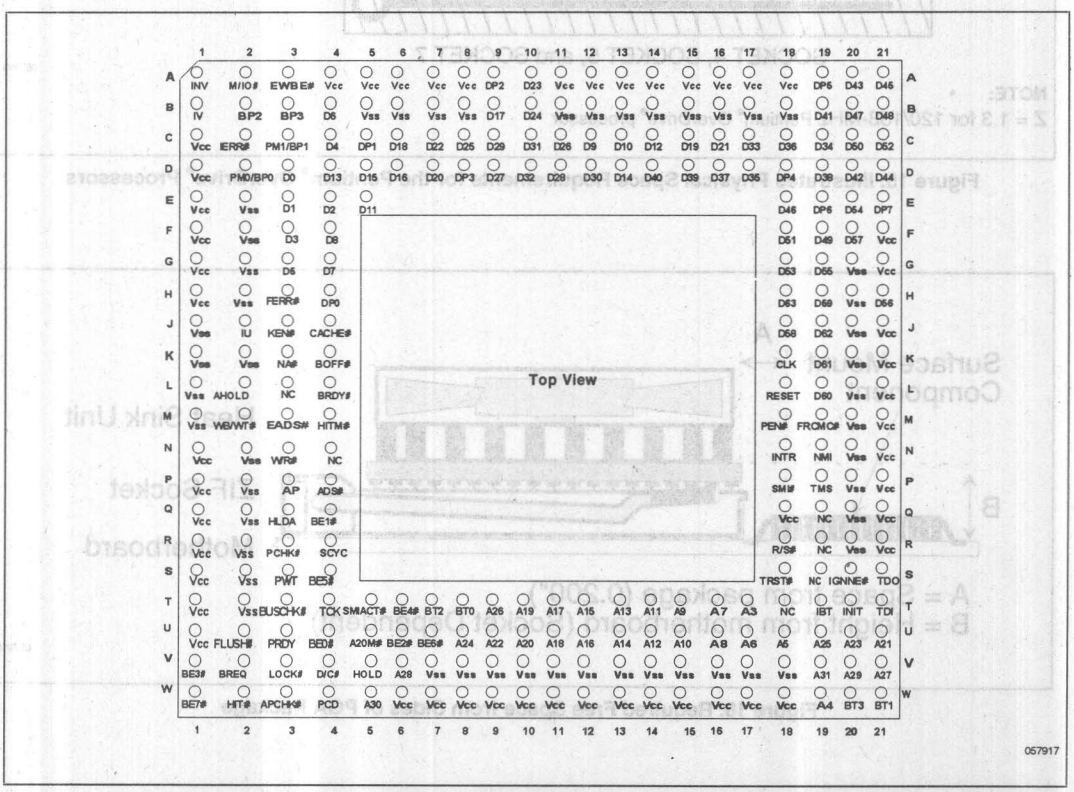


Figure 17. 273-Pin Socket 4 for 120/133-MHz Pentium® OverDrive® Processor

7.0. THERMAL SPECIFICATIONS

7.1. Pentium® OverDrive® Processor

The Pentium OverDrive processors are shipped with an attached fan/heatsink for a complete thermal solution for the processor upgrade. The fan/heatsink cooling solution will properly cool the Pentium OverDrive processor provided the space requirements of Section 6.2. are met and the maximum air temperature entering the fan/heatsink (T_A) does not exceed 45°C. The fan/heatsink inlet temperature (T_A) is measured 0.3" above the centerline of the fan hub at the system maximum ambient operating temperature (See Figure 15).

8.0. TESTABILITY

8.1. Introduction

This section describes the features which are included in the Pentium OverDrive processors for purposes of testability of the part. The testability features provided for the original Pentium processor are also available on the Pentium OverDrive processors. The Pentium OverDrive processors however, do not support the IEEE Standard 1149.1 boundary scan using the Test Access Port (TAP) and TAP Controller as described in Chapters 11 and 27 of the *Pentium® Family User's Manual, Volume 1*. Contact your Intel representative for further details. Some features of testability are described below.

8.2. Built in Self Test (BIST)

Self test is initiated by driving the INIT pin high when RESET transitions from high to low. No bus cycles are run by the Pentium OverDrive processor during self test. The duration of self test is approximately 2^{19} clocks. BIST is used to test approximately 70% of the devices in the Pentium OverDrive processor.

The Pentium OverDrive processor BIST consists of two parts: hardware self test and microcode self test. During the hardware portion of BIST, the microcode and the large PLAs are tested. All possible input combinations of the microcode ROM and PLAs are tested. The microcode self test is done by comparing the stored value of ROM check sums with the result of the self test.

If the mismatch occurs or the errors are detected during BIST, the Pentium OverDrive processor will assert the IERR# pin and attempt to shutdown.

8.3. Tri-State Test Mode

When the FLUSH# pin is sampled low in the clock prior to the RESET pin going from high to low, the Pentium OverDrive processor enters tristate test mode. The Pentium OverDrive processor floats all of its output pins and bi-directional pins including pins which are never floated during normal operation (except TD0). Tristate test mode can be initiated in order to facilitate testing of board connections. The Pentium OverDrive processor remains in tristate test mode until the RESET pin is toggled again.

APPENDIX A

Pentium® OverDrive® PROCESSOR UPGRADABILITY DESIGN CONSIDERATIONS

Intel has designed the family of Pentium OverDrive processors so that they can be easily installed by the end-user. PC manufactures can support this by implementing the design considerations listed in Table 19.

Table 19. Design Considerations

Design Consideration	Implementation
Visible Pentium® OverDrive® Processor Socket	The Pentium OverDrive processor socket should be easily visible when the PC's cover is removed. Label the Pentium OverDrive processor socket and the location of pin 1 by silk screening this information on the PC board.
Accessible Pentium OverDrive Processor Socket	Make the Pentium processor easily accessible to the end user (i.e., do not place the Intel Pentium OverDrive processor socket under the hard disk). If the low insertion force (LIF) is used, position the Pentium OverDrive processor socket on the PC board such that there is ample clearance around the socket.
Foolproof Chip Orientation	Intel packages all Pentium OverDrive processors with a "keyed pin configuration" that insures that the Pentium OverDrive processors fits into the respective sockets in the correct orientation.
Zero Insertion Force Upgrade Socket	The high pin count of the Pentium OverDrive processors often require more than 60 lbs of insertion force for Low Insertion Force (LIF) sockets. A Zero Insertion Force (ZIF) socket insures that the chip insertion force does not damage the PC Board. If the ZIF socket has a handle, be sure to allow enough clearance for the socket handle. If a LIF socket is used, additional PC board support is recommended.
"Plug and Play"	Jumper or switch changes should not be needed to electrically configure the system for the Pentium OverDrive processor.
Thorough Documentation	Describe the Pentium OverDrive processor's installation procedure in the PC's User's Manual.

APPENDIX B

Pentium® OverDrive® PROCESSOR ZIF SOCKET VENDORS

The following list provides examples of sockets which can be used for Pentium processor-based systems.

NOTE:

This is not a comprehensive list, Intel has not tested all of the Vendor's sockets listed below and cannot guarantee that these will meet every PC manufacturer's specific requirement.

	Socket No.	Style	Drawing No.	Part No.
AMP	Socket 5	SLAZ, OC, T	C-916513	916513
(800) 522-6752	Socket 5	SLAZ, OC, T	C-916560	916560
	Socket 5	SLAZ, OC, T	C-916655	916655
	Socket 5	SLAZ, OC, T	C-916656	916656
	Socket 5	SLAZ, OC, T	C-916671	916671
	Socket 5	SLAZ, OC, T	C-916672	916672
	Socket 7	SLAZ, OC, T	C-916637	916637
	Socket 7	SLAZ, OC, T	C-916657	916657
	Socket 7	SLAZ, OC, T	C-916658	916658
Appros	Socket 5	SLAZ, OC, T	KEA391129	SLR-S19-320-LN2
(408) 567-1234	Socket 7	SLAZ, OC, T	KEA391130	SLR-S19-321-LN2
	Average plating thickness used for qualification testing: 11.2 micro inches gold.			
Augat	Socket 5	SLAZ, OC, T	MP-AX159BCD20	MP-AX159BCD203
(800) 999-7646	Socket 5	SLAZ, OC, T	MP-AX159BCD20A	MP-AX159BCD203A
	Socket 5	SLAZ, OC, T	MP-AX159BCD20B	MP-AX159BCD203B
	Socket 7	SLAZ, OC, T	MP-AX164BCD21X	MP-AX164BCD213
	Socket 7	SLAZ, OC, T	MP-AX164BCD21XA	MP-AX164BCD213A
	Socket 7	SLAZ, OC, T	MP-AX164BCD21XB	MP-AX164BCD213B
	Average plating thickness used for qualification testing sockets: 19 micro inches gold.			

	Socket No.	Style	Drawing No.	Part No.
Berg/Mckenzie	Socket 5	SLAZ, OC, T	SAL B 270086-000	ZIF 97050-4020
(510) 654-2700	Socket 5	SLAZ, OC, T	SAL B 270086-000	ZIF 97050-4120
	Socket 7	SLAZ, OC, T	SAL B 270088-000	ZIF 97054-4020
	Socket 7	SLAZ, OC, T	SAL B 270088-000	ZIF 97054-4120
	Average plating thickness used for qualification testing sockets: 35 micro inches gold			
Foxconn	Socket 5	SLAZ, OC, NT	309-0000-049	PZ32023-0120
(408) 749-1228	Socket 5	SLAZ, OC, T	309-0000-049	PZ32033-0120
	Socket 5	SLAZ, OC, T	309-0000-049	PZ32043-0120
	Socket 5	SLAZ, OC, T	309-0000-049	PZ32053-0120
	Socket 7	SLAZ, OC, T	309-0000-062	PZ32143-0120
	Socket 7	SLAZ, OC, T	309-0000-062	PZ32153-0120
	Average plating thickness used for qualification testing: 10.0 micro inches gold			
JAE	Socket 5	SLAZ, OC, T	SJ029842-E	PCPS-ZL320-A9
(714) 753-2628	Socket 7	SLAZ, OC, T	SJ029842-E	PCPS-ZL321-A9
	Average plating thickness used for qualification testing: Socket 5/7 3.7 micro inched gold Flash/31.4 microinches Palladium Nickel, Socket 8 4.5 micro inched gold Flash/34 micro inches Palladium Nickel.			
Producer	Socket 5	SLAZ, OC, T	PD104-3202	PD104-32025
886-2-202-3578	*Average plating thickness used for qualification testing: 5.7 micro inches gold.*			
Yamaichi	Socket 5	SLAZ, OC, T	KL-13790	NP210-320-0100-CC0
(800) 769-0797	Socket 5	SLAZ, OC, T	KL-13425	NP210-320-0100-CC1
	Socket 5	SLAZ, OC, T	KL-13518	NP210-320-0100-CC2
	Socket 5	SLAZ, OC, T	KL-13930	NP210-320-0100-CC3
	Socket 5	SLAZ, OC, T	KL-13625	NP210-320K13625(D)
	Socket 7	SLAZ, OC, T	KL-13823	NP210-321-0100-CC1
	Socket 7	SLAZ, OC, T	KL-13620	NP210-321-0100-CC2
	Socket 7	SLAZ, OC, T	KL-13938	NP210-321-0100-CC3
	Average plating thickness used for qualification testing: 6.1 micro inches gold.			

Pentium® OverDrive® PROCESSOR WITH MMX™ TECHNOLOGY FOR Pentium PROCESSOR-BASED SYSTEMS

200-MHz Pentium® OverDrive® Processor with MMX™ Technology to upgrade 100/133/166-MHz Pentium Processor-Based Systems

180-MHz Pentium OverDrive Processor with MMX Technology to upgrade 90/120/150-MHz Pentium Processor-Based Systems and upgrades 75-MHz Pentium Processor-Based Systems to 150-MHz

166-MHz Pentium OverDrive Processor with MMX Technology to upgrade 100/133-MHz Pentium Processor-Based Systems



- **Support for MMX™ Technology**
- **Powerful Processor Upgrades for Upgradable Pentium® Processor-Based Systems**
- **Superscalar Architecture**
  - **Enhanced pipelines**
  - **Two Pipelined Integer Units Capable of 2 Instructions/Clock**
  - **Pipelined MMX Unit**
  - **Pipelined Floating-Point Unit**
- **Separate Code and Data Caches**
  - **Deeper Write Buffers, "Pool" Configuration**
  - **Enhanced Branch Prediction**
  - **Virtual Mode Extensions**
- **32-Bit CPU with 64-Bit Data Bus**
- **.35μM CMOS Silicon Technology**
- **On-package Voltage Regulation and Voltage Filtering**
- **Integrated Fan/Heatsink Thermal Solution**
- **Compatible with Installed Software Base**
  - **MS-DOS*, Windows*, Windows 95, Windows NT, OS/2*, UNIX***
- **Product Line Supports Socket 5 & Socket 7 Designs**
- **320 pin SPGA Package**
- **Bus/Core Ratio, Hard-Bonded in 2/5 and 1/3 Modes**
- **Easy Installation**
- **Supports 50, 60, 66-MHz Bus Speeds**
- **Single 3.3 Volt Supply**

June 1997

Order Number: 290607-001

processor-based systems.

The Pentium OverDrive processor with MMX technology for Pentium processor-based systems has 4.5 million transistors and is built on Intel's advanced 0.35-micron silicon technology. The Pentium OverDrive processor with MMX technology is equipped with high reliability, integrated fan/heatsinks.

1.0. INTRODUCTION

This datasheet describes Intel's Pentium OverDrive processor with MMX technology for upgradable Pentium processor-based systems. The Pentium OverDrive processor with MMX technology currently includes upgrades for 75, 90, 100, 120, 133, 150, and 166-MHz Pentium processors. Technical descriptions of other Pentium OverDrive processors are available in *Intel OverDrive® Processors* datasheet (Order #290436).

This datasheet is intended to be used in conjunction with the *Pentium® Family User's Manual* (Order #241428), which describes the Pentium family architecture and functionality. All enhancements or differences between the Pentium OverDrive processor with MMX technology and the original Pentium processor (i.e., 75/90/100/120/133/150/166-MHz Pentium processor vs. 200/180/166-MHz Pentium OverDrive processor with MMX technology) are described in this datasheet.

Pentium processor-based systems that are compatible with the Pentium OverDrive processor with MMX technology must be designed to both the original processor specifications and the Pentium OverDrive processor with MMX technology specifications.

1.1. Product Overview

The Pentium OverDrive processor with MMX technology, for upgradable 75, 90, 100, 120, 150, and 166-MHz Pentium systems, allows users to upgrade to more advanced Pentium processor technology and adds Intel's new MMX technology.

Figure 1 contains the block diagram of the Pentium OverDrive processor with MMX technology. Figure 2 lists some of the enhancements of the Pentium OverDrive processor with MMX technology. Figure 3 describes the upgrade choices available for an existing Pentium processor system.

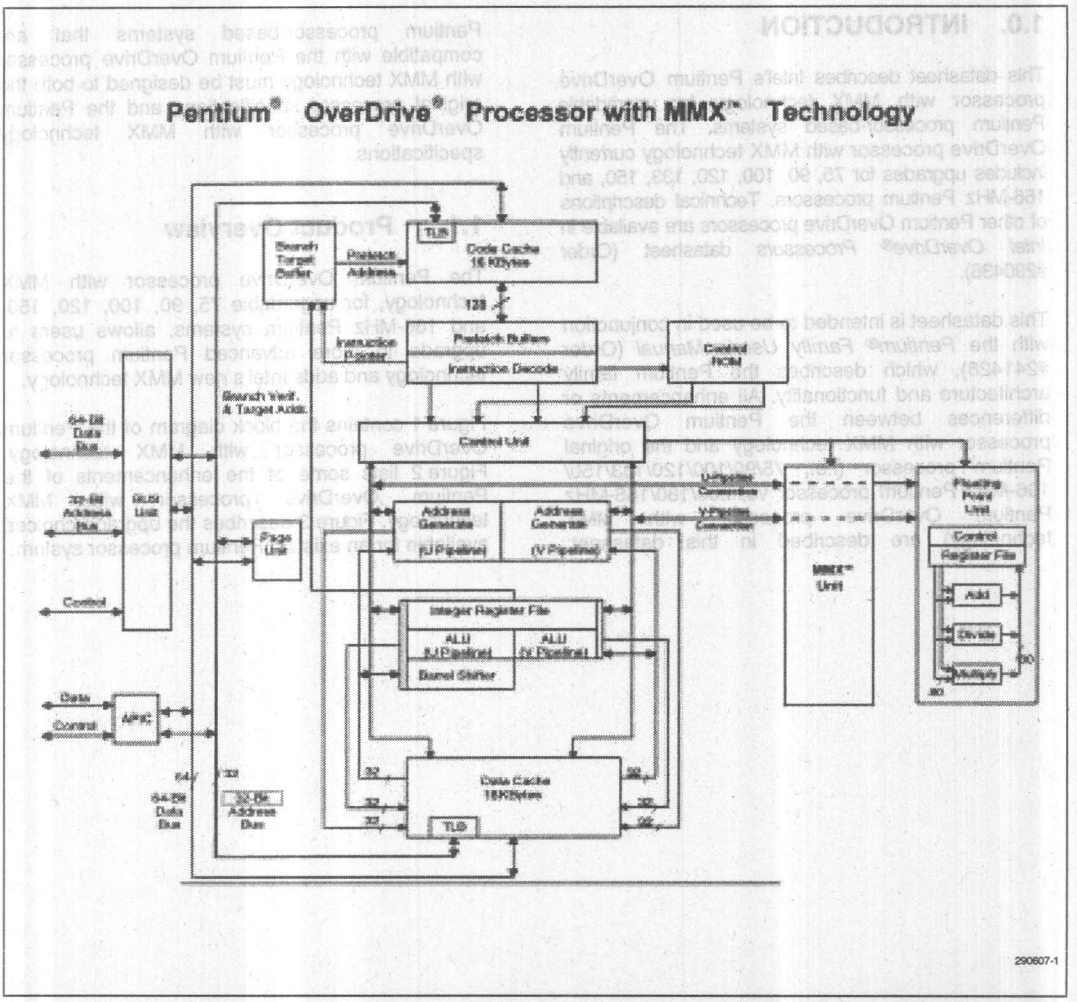


Figure 1. Pentium® OverDrive® Processor with MMX™ Technology Block Diagram

- Based on Advanced Pentium® Processor with MMX™ Technology
- Superscalar Architecture
- Pipelined Floating-Point Unit
- Separate 16K Code and 16K Data caches
- 64 Bit Data Bus
- Address Parity
- Virtual Mode Extensions
- System Management Mode
- Fractional Bus Operation

200, 180, and 166-MHz Pentium OverDrive® Processors with MMX Technology

- .35µM CMOS Silicon Technology
- Dynamic Branch prediction
- Improved Execution Time
- Writeback MESI Protocol in the Data Cache
- Bus Cycle Pipelining
- Internal Parity Checking
- Performance Monitoring
- Execution Tracing
- Active Fan/Heatsink
- For 75, 90, and 100-MHz Pentium Processor-Based Systems
- 320 Pin SPGA Pinout
- On-package Voltage Regulation

290607-2

Figure 2. Pentium® OverDrive® Processor with MMX™ Technology Key Features

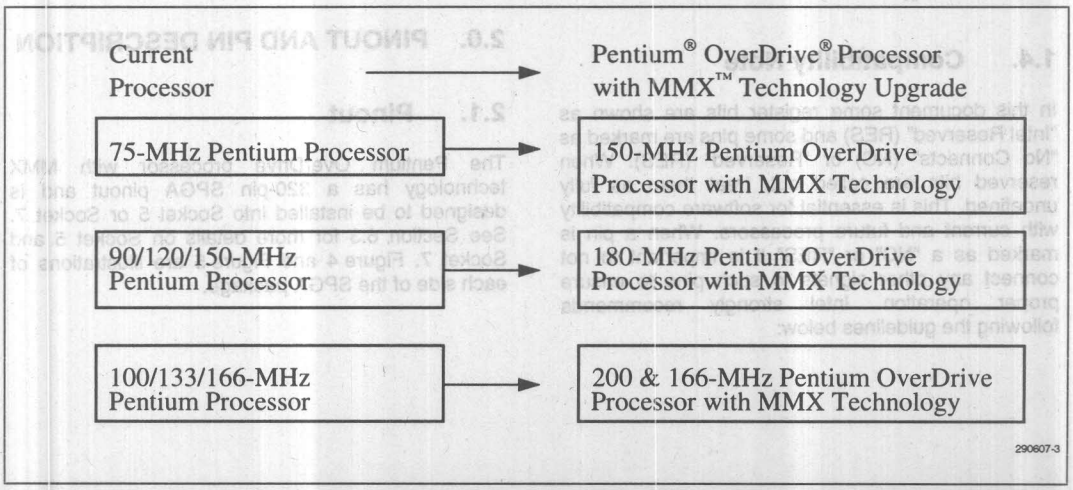


Figure 3. Pentium® OverDrive® Processor with MMX™ Technology Upgrade Choices

1.2. Product Description

The Pentium OverDrive processor with MMX technology comes in a 320-pin SPGA package and is a drop-in replacement for the 75, 90, 100, 120, 133, 150 and 166-MHz Pentium processor. It comes with on-package voltage regulation to provide the required 2.8 volts for the core and a fan/heatsink for a complete thermal solution. The internal core operates at 3.0 and 2.5 times the speed of the system bus for respective 200MHz and 166-MHz Pentium OverDrive processor with MMX technology. For dual socket systems the original processor must be removed and the Pentium OverDrive processor with MMX technology should be installed in the secondary socket since it does not support dual processing.

1.3. Purpose of this Document

This document describes the system architecture and physical environment of Pentium OverDrive processor with MMX technology. It also outlines differences between the originally installed Pentium processor and the Pentium OverDrive processor with MMX technology.

1.4. Compatibility Note

In this document some register bits are shown as "Intel Reserved" (RES) and some pins are marked as "No Connects" (NC) or "Reserved" (RES). When reserved bits are called out, treat them as fully undefined. This is essential for software compatibility with current and future processors. When a pin is marked as a "NC" or "RES" it is important to not connect any other signals to such pins to ensure proper operation. Intel strongly recommends following the guidelines below:

1. Do not depend on the states of any undefined bits when testing the values of defined register. Mask them out when testing.
2. Do not depend on the states of any undefined bits when storing them to memory or another register.
3. Do not depend on the ability to retain information written into any undefined bits.
4. When loading registers always load the undefined bits as zeros.
5. Never connect signals to device pins marked "NC" or "RES".
6. **INC** pins are Internal No-Connects. This means that the pin is not connected to the processor internally. For example; the CPUTYP signal pin on the Pentium OverDrive processor with MMX technology is internally not connected to the package pin. The core is internally tied to V_{SS}. The pin on the package is defined as INC. Any external connections to the package pin will not affect the processor core because the core is physically disconnected from the package pin.

2.0. PINOUT AND PIN DESCRIPTION

2.1. Pinout

The Pentium OverDrive processor with MMX technology has a 320-pin SPGA pinout and is designed to be installed into Socket 5 or Socket 7. See Section 6.3 for more details on Socket 5 and Socket 7. Figure 4 and Figure 5 are illustrations of each side of the SPGA package.

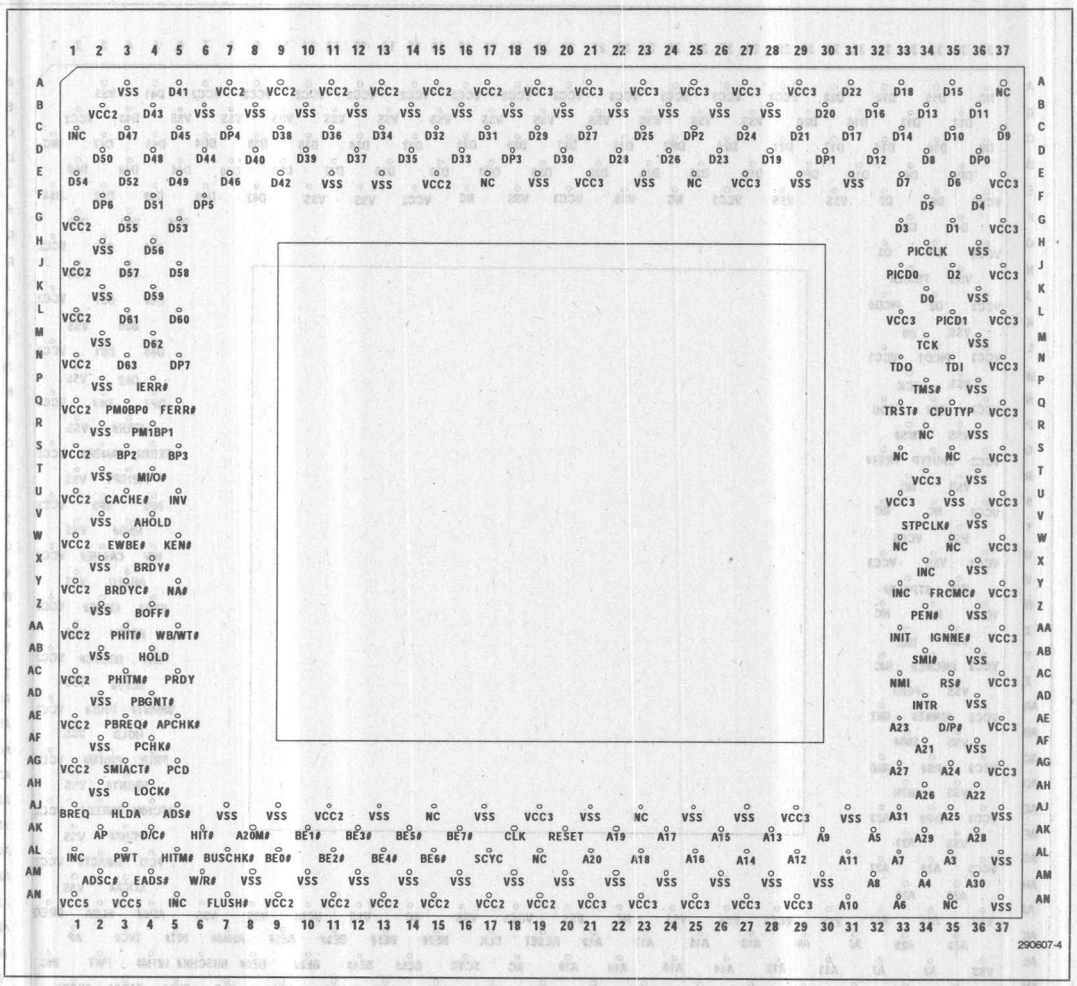


Figure 4. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Top Side View

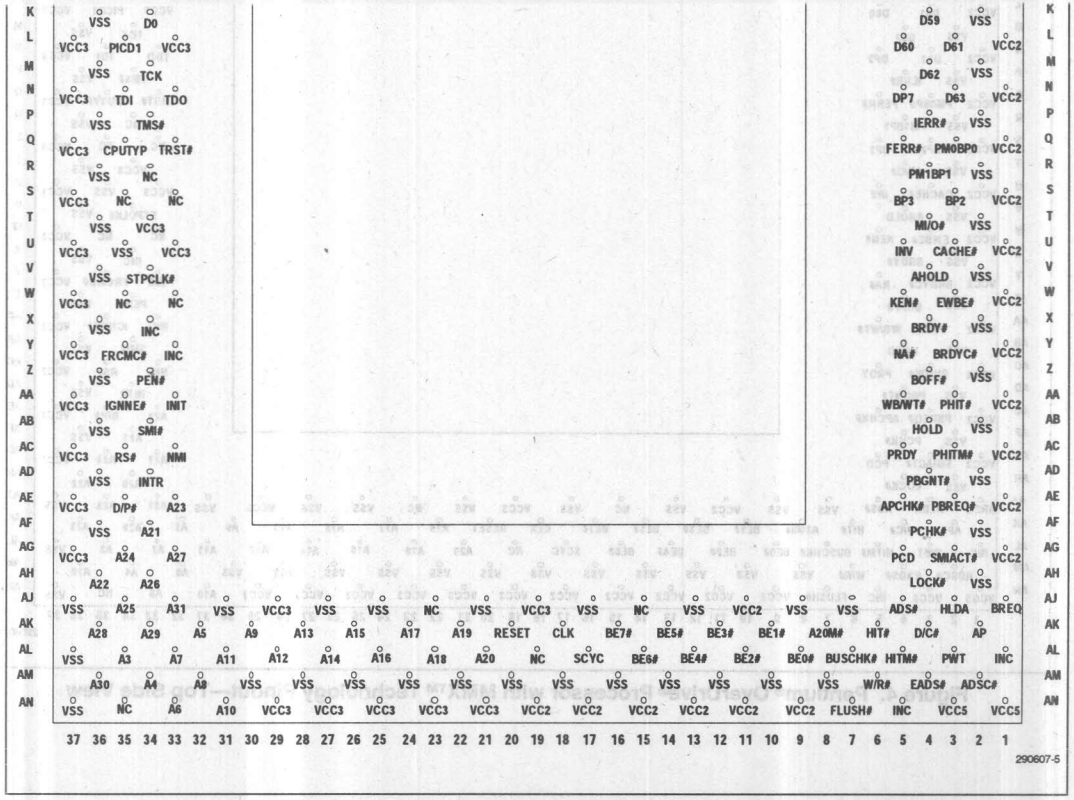


Figure 5. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Pin Side View

2.2. Pin Cross Reference

Table 1. 320-Pin SPGA Pin Cross Reference by Pin Name

Address									
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 1. 320-Pin SPGA Pin Cross Reference by Pin Name (Continued)

Control							
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
A20M#	AK08	BRDYC#	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	FRCMC#	Y35	PM0/BP0	Q03
ADSC#	AM02	BUSCHK#	AL07	HIT#	AK06	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HITM#	AL05	PRDY	AC05
AP	AK02	CPUTYP**	Q35	HLDA	AJ03	PWT	AL03
APCHK#	AE05	D/C#	AK04	HOLD	AB04	R/S#	AC35
BE0#	AL09	D/P#*	AE35	IERR#	P04	RESET	AK20
BE1#	AK10	DP0	D36	IGNNE#	AA35	SCYC	AL17
BE2#	AL11	DP1	D30	INIT	AA33	SMI#	AB34
BE3#	AK12	DP2	C25	INTR/LINT0	AD34	SMIACT#	AG03
BE4#	AL13	DP3	D18	INV	U05	TCK	M34
BE5#	AK14	DP4	C07	KEN#	W05	TDI	N35
BE6#	AL15	DP5	F06	LOCK#	AH04	TDO	N33
BE7#	AK16	DP6	F02	M/IO#	T04	TMS	P34
BOFF#	Z04	DP7	N05	NA#	Y05	TRST#	Q33
BP2	S03	EADS#	AM04	NMI/LINT1	AC33	W/R#	AM06
BP3	S05	EWBE#	W03	PCD	AG05	WB/WT#	AA05
BRDY#	X04	FERR#	Q05	PCHK#	AF04		

APIC		Clock Control		Dual Processor Private Interface	
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**
PICCLK	H34	CLK	AK18	PBGNT#	AD04
PICD0	J33	BF **	Y33	PBREQ#	AE03
[DPEN#]		BF1**	X34	PHIT#	AA03
PICD1 [APICEN]	L35	STPCLK#	V34	PHITM#	AC03

NOTES:

The shaded pin definitions on the Pentium® OverDrive® processor with MMX™ technology are dual processing pins and are not supported by the Pentium OverDrive processor with MMX technology in Table 2.

• The D/P# signal in the 75, 90, 100, 120, 133, 150, and 166-MHz Pentium processor is always driven. Low indicates primary processor has the bus and high indicates the secondary processor is driving the bus. In the Pentium OverDrive processor with MMX technology this pin is defined internal no connect.

** These signals are internally set and are not connected to the Pentium OverDrive processor with MMX technology pins. The pins are defined as Internal No-Connects.

Table 1. 320-Pin SPGA Pin Cross Reference by Pin Name (Continued)

V_{CC}									
A07	A19	B02	G37	N01	T34	Y01	AE01	AJ29	AN19
A09	A21	E15	J01	N37	U01	Y37	AE37	AN09	AN21
A11	A23	E21	J37	Q01	U33	AA01	AG01	AN11	AN23
A13	A25	E27	L01	Q37	U37	AA37	AG37	AN13	AN25
A15	A27	E37	L33	S01	W01	AC01	AJ11	AN15	AN27
A17	A29	G01	L37	S37	W37	AC37	AJ19	AN17	AN29

V_{SS}								
A03	B20	E23	M36	V02	AD02	AJ17	AM10	AM26
B06	B22	E29	P02	V36	AD36	AJ21	AM12	AM28
B08	B24	E31	P36	X02	AF02	AJ25	AM14	AM30
B10	B26	H02	R02	X36	AF36	AJ27	AM16	AN37
B12	B28	H36	R36	Z02	AH02	AJ31	AM18	AL01
B14	E11	K02	T02	Z36	AJ07	AJ37	AM20	
B16	E13	K36	T36	AB02	AJ09	AL37	AM22	
B18	E19	M02	U35	AB36	AJ13	AM08	AM24	

NC/INC							V_{CC5}
A37	E25	S33	W33	C01	AJ23	AN35	AN01
E17	R34	S35	W35	AJ15	AL19	AN05	AN03

NOTE:
The shaded V_{CC}/V_{SS}/NC pins are new pin definitions (additions) on the Pentium® OverDrive® processor with MMX™ technology with the exception of A03 and B02.

A31-A3	I/O	As outputs, the address lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A3.
ADS#	O	The address status indicates that a new valid bus cycle is currently being driven by the Pentium OverDrive processor with MMX technology.
ADSC#	O	ADSC# is functionally identical to ADS#.
AHOLD	I	In response to the assertion of address hold, Pentium OverDrive processor with MMX technology will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	Address parity is driven by the Pentium OverDrive processor with MMX technology with even parity information on all the Pentium OverDrive processor with MMX technology generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium OverDrive processor with MMX technology during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium OverDrive processor with MMX technology
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium OverDrive processor with MMX technology has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	The APIC is not supported by the Pentium OverDrive processor with MMX technology.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).
[BF] [BF1]	I	**Bus Frequency** determines the bus-to-core frequency ratio on the Pentium processor. These are Internal No Connects on the Pentium OverDrive processor with MMX technology which has a preset bus fraction of 5/2 for 166-MHz OverDrive Processor and 3/1 for 200-MHz OverDrive Processor core/bus ratio.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
BOFF#	I	The backoff input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium OverDrive processor with MMX technology will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time Pentium OverDrive processor with MMX technology restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The breakpoint pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the performance monitoring pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The burst ready input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium OverDrive processor with MMX technology data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	This signal has the same functionality as BRDY#.
BREQ	O	The bus request output indicates to the external system that Pentium OverDrive processor with MMX technology has internally generated a bus request. This signal is always driven whether or not the Pentium OverDrive processor with MMX technology is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, Pentium OverDrive processor with MMX technology will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium OverDrive processor with MMX technology will vector to the machine check exception.
CACHE#	O	For Pentium OverDrive processor with MMX technology-initiated cycles the cache pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, Pentium OverDrive processor with MMX technology will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The clock input provides the fundamental timing for Pentium OverDrive processor with MMX technology. The clock frequency is the operating frequency of the Pentium OverDrive processor with MMX technology external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK.
CPUTYP	I	CPUTYP is internally tied to ground and is a Internal No-Connect (INC) to the package pin on the Pentium OverDrive processor with MMX technology.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
D/C#	O	The data/code output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The Pentium OverDrive processor with MMX technology does not support dual processing.
D63-D0	I/O	These are the 64 data lines for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the data parity pins for the processor. There is one for each byte of the data bus. They are driven by Pentium OverDrive processor with MMX technology with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium OverDrive processor with MMX technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium OverDrive processor with MMX technology. DP7 applies to D63-D56, DP0 applies to D7-D0.
[DPEN#] PICD0	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
EADS#	I	This signal indicates that a valid external address has been driven onto the Pentium OverDrive processor with MMX technology address pins to be used for an inquire cycle.
EWBE#	I	The external write buffer empty input, when inactive (high), indicates that a write cycle is pending in the external system. When Pentium OverDrive processor with MMX technology generates a write, and EWBE# is sampled inactive, the Pentium OverDrive processor with MMX technology will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The floating-point error pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I	When asserted, the cache flush input forces the Pentium OverDrive processor with MMX technology to writeback all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium OverDrive processor with MMX technology indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
FRCMC#	I	The Pentium OverDrive processor with MMX technology does not support functional redundancy checking.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
HIT#	O	The hit indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either Pentium OverDrive processor with MMX technology data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium OverDrive processor with MMX technology cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The hit to a modified line output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The bus hold acknowledge pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that Pentium OverDrive processor with MMX technology has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and Pentium OverDrive processor with MMX technology will resume driving the bus. If the Pentium OverDrive processor with MMX technology has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the bus hold request, Pentium OverDrive processor with MMX technology will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium OverDrive processor with MMX technology will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium OverDrive processor with MMX technology will recognize HOLD during reset.
IERR#	O	The internal error pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium OverDrive processor with MMX technology will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the ignore numeric error input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium OverDrive processor with MMX technology will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium OverDrive processor with MMX technology will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium OverDrive processor with MMX technology will stop execution and wait for an external interrupt.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
INIT	I	The Pentium OverDrive processor with MMX technology **initialization** input pin forces the Pentium OverDrive processor with MMX technology to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the Pentium OverDrive processor with MMX technology will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active maskable interrupt input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium OverDrive processor with MMX technology will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The invalidation input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The cache enable pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium OverDrive processor with MMX technology generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The bus lock pin indicates that the current bus cycle is locked. Pentium OverDrive processor with MMX technology will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back to back locked cycles.
M/IO#	O	The memory/input-output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active next address input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium OverDrive processor with MMX technology will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium OverDrive processor with MMX technology supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The non-maskable interrupt request signal indicates that an external non-maskable interrupt has been generated.
PBGNT#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
PCD	O	The page cache disable pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The parity check output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The parity enable input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium OverDrive processor with MMX technology will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium OverDrive processor with MMX technology will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PHITM#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PICCLK	I	The Pentium OverDrive processor with MMX technology does not support dual processing.
PICD0-1 [DPEN#] [APICEN]	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PBREQ#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The probe ready output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
PWT	O	The page write through pin reflects the state of the PWT bit in CR3, the Page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external writeback indication on a page by page basis.
R/S#	I	The run / stop input is an asynchronous, edge sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
RESET	I	**RESET** forces the Pentium OverDrive processor with MMX technology to begin execution at a known state. All Pentium OverDrive processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH#, and INIT are sampled when RESET transitions from high to low to determine if tristate test mode mode will be entered, or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode (SMM).
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium OverDrive processor with MMX technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium OverDrive processor with MMX technology will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for Pentium OverDrive processor with MMX technology boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium OverDrive processor with MMX technology during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium OverDrive processor with MMX technology on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of Pentium OverDrive processor with MMX technology on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the test mode select input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC2}	I	These 28 **power** inputs are defined separately so they may be used in a split voltage plane motherboard design. These pins **must** be supplied with 3.3V for the Pentium OverDrive processor with MMX technology to function.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
V_{CC3}	I	These 32 **power** inputs must be connected to 3.3V in either single or split voltage systems.
V_{CC5}	I	The Pentium OverDrive processor with MMX technology has two 5V **power** inputs.
V_{SS}	I	The Pentium OverDrive processor with MMX technology has 68 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line by line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

NOTE:
Highlighted items in Table 2 are signals not supported on the Pentium® OverDrive® processor with MMX™ technology.

2.4. Pin Descriptions

2.4.1. INPUT PINS

Table 3. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	N/A	Synchronous/RESET	Pulldown	
BF1	N/A	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2,T12,T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2,T12,T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
CPUTYP	N/A	Synchronous/RESET	Pulldown	
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
FRCMC#	N/A	Asynchronous	Pullup	
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PICCLK	N/A	Asynchronous	Pullup	
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	

Table 3. Input Pins (Continued)

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

NOTE:
Highlighted signals are original Pentium® processor 75/90/100/120/133/150/166 MHz signals and are not supported by the Pentium OverDrive® processor with MMX™ technology.

2.4.2. OUTPUT PINS

Table 4. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
D/P#	n/a	
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO# , D/C# , W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:

All output pins are floated during tristate test mode (except TDO).

Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processor with MMX™ technology.

2.4.3. INPUT/OUTPUT PINS

Table 5. Input/Output Pins

Name	Active Level	When Floated	Qualified (When an Input)	Internal Resistor
A31-A3	n/a	Address hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTES:
All input/output pins are floated during tristate test.
Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processor with MMX™ technology.

Table 6. Interprocessor I/O Pins

Name	Active Level	Internal Resistor
PHIT#	n/a	Pullup
PHITM#	n/a	Pullup
PBGNT#	n/a	Pullup
PBREQ#	n/a	Pullup

NOTE:
Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processor with MMX™ technology.

Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

Table 8. Pin Functional Groupings Not Supported by Pentium® OverDrive® Processor with MMX™ Technology

Function	Pins
APIC Support	PICCLK, PICD0-1
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Functional Redundancy Checking	FRCMC#
Miscellaneous Dual Processing	CPUTYP, D/P#
Execution Tracing	BT3-BT0, IU, IV, IBT

3.0. COMPONENT OPERATION

3.1. Core to Bus Ratio for Higher Speed

The Pentium OverDrive processor with MMX technology incorporates an internal Phase Lock Loop (PLL) and clock multiplier to generate the higher internal speeds. This allows the internal processor core to operate synchronously and at higher frequencies than the external bus.

On the 200/180-MHz Pentium OverDrive processor with MMX technology, the bus fraction configuration will be preset to 3/1 internally and 166-MHz to 5/2. See Table 9 for details.

Table 9. Core/Bus Frequencies

Internal Speed	Bus Speed	Replaces (Core/Bus)
150-MHz	50-MHz	75/50-MHz
180-MHz	60-MHz	90/60-MHz
		120/60-MHz
		150/60-MHz
166-MHz	66-MHz	100/66-MHz
		133/66-MHz
200-MHz	66-MHz	100/66-MHz
		133/66-MHz
		166/66-MHz

3.2. Hardware Interface Differences

The Pentium OverDrive processor with MMX technology is pin-for-pin compatible with the respective original Pentium processors, except for the additional pins defined by Socket 5 and 7 for the Pentium OverDrive processor with MMX technology. Some minor differences are discussed in this section and are referenced in tables in previous section. These differences represent features that are not required for an end-user CPU upgrade.

3.2.1. CPUTYP SIGNAL

The Pentium OverDrive processor with MMX technology CPUTYP signal is internally tied to ground and the signal pin on the package is an internal no-connect (INC). The original Pentium processor must be removed for the Pentium OverDrive processor with MMX technology to function properly.

3.3. Processor Initialization

3.3.1. POWER UP SPECIFICATION

The Pentium OverDrive processor with MMX technology will boot like the respective original Pentium processors. If the Pentium OverDrive processor with MMX technology is installed in a second socket of dual socket system the primary CPU must be removed or the system will not boot properly.

3.3.2. TEST AND CONFIGURATION FEATURES (BIST, FRC, TRISTATE TEST MODE)

The Pentium OverDrive processor with MMX technology will execute the Built In Self Test (BIST) and Tristate Test Mode same as the respective original Pentium processor. Functional Redundancy Checking is not supported.

3.3.3. INITIALIZATION WITH RESET, INIT AND BIST

The Pentium OverDrive processor with MMX technology handling of RESET, INIT, and the Built In Self Test (BIST) is the same as the original Pentium processors. The register states after RESET, INIT, and BIST are same as the original Pentium processors. For further information refer to Section 8 in this datasheet.

3.4. Instruction Differences

The Pentium OverDrive processor with MMX technology is 100% compatible with the Pentium processor (75-200). Two additions have been made. The 57 instructions that comprise the MMX Technology Instruction set and the RDPMC (Read Performance Monitoring Counter) instruction. These new instructions are an added feature and will not impact the use of the upgraded system in anyway unless specifically used.

3.4.1. MMX™ TECHNOLOGY EXTENSIONS TO THE INTEL ARCHITECTURE

Intel's MMX technology is an extension to the Intel architecture which provides for additional performance for multimedia and communications applications. Intel processors that include this technology are still 100% compatible with all "scalar" Intel processors. This means that all existing software that runs on existing Intel processors will continue to run (without modification) on an Intel processor that incorporates MMX technology.

Intel's MMX technology uses a SIMD (Single Instruction, Multiple Data) tecnique to speedup multimedia and communications software by processing multiple data elements in parallel. The MMX instruction set all 57 new opcodes and a new 64-bit quadword type. The new 64-bit data type holds packed integer values. These packed integer values can be 8 bytes, 4 words, or 2 double-words.

The Pentium OverDrive processor with MMX technology includes the MMX instruction set as defined by the *Intel Architecture MMX™ Technology Programmers Reference Manual* (Order #243007) and the *Intel Architecture MMX™ Technology Developer's Manual* (Order #243006). Software can determine that the system has been upgraded to a Intel Architecture processor that supports MMX technology via the CPUID instruction.

3.4.2. RDPMC (READ PERFORMANCE MONITORING COUNTER)

RDPMC will enable the user to only READ the performance monitoring counters.

3.5. CPUID

The CPUID instruction allows software to determine the type and features of the microprocessor. When executing the CPUID instruction the Pentium OverDrive processor with MMX technology behaves like the original Pentium processors:

- If the value in EAX is '0' then the 12-byte ASCII string "GenuineIntel" (little endian) is returned in EBX, EDX, and ECX. Also, a '1' is returned in EAX.
- If the value in EAX is '1' then the processor version is returned in EAX and the processor capabilities are returned in EDX. The values of EAX and EDX for the Pentium® OverDrive® processor with MMX™ technology are given below.
- If the value in EAX is neither '0' nor '1', Pentium OverDrive processor with MMX technology writes '0' to all registers or is undefined.

The stepping field has the same format as the original Pentium processor and will be the same for the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology will have a unique CPUID from the original Pentium processor and the Pentium processor with MMX technology (154xH Vs. 052xH and 054xH). The type field is defined in Table 11.

Table 10. EAX Bit Values Definition for CPUID

CPU	31...14	13...12	11...8	7...4	3...0
Field Definition	(reserved)	type	family	model	stepping
Pentium® processor (75, 90, 100)	(reserved)	Table 11	5H	2H	varies
Pentium processor with MMX™ technology (166, 200, 233-MHz)	(reserved)	Table 11	5H	4H	varies
Pentium OverDrive® processor with MMX technology	(reserved)	Table 11	5H	4H	varies

Table 11. EAX Bit Values Definition for Processor Type

Bit 13	Bit 12	Processor Type
0	0	Primary Pentium® processor
0	0	Primary Pentium processor with MMX™ technology
0	1	Pentium OverDrive® processor with MMX technology
1	0	Dual Pentium processor *
1	1	Reserved

NOTE:

* The Pentium® OverDrive® processor with MMX™ technology does not support Dual Processing mode.

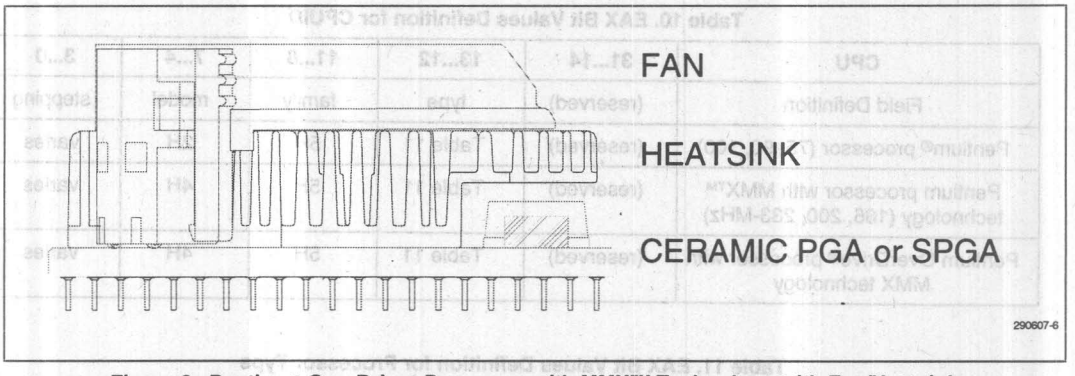


Figure 6. Pentium® OverDrive® Processor with MMX™ Technology with Fan/Heatsink

3.6. On-Package Fan/Heatsink

The on-package fan/heatsink included with the Pentium OverDrive processor with MMX technology requires different stress ratings than the original Pentium processor. The fan is a detachable unit, and the storage temperature is stated separately in Table 12. Operation of the Pentium OverDrive processor with MMX technology is defined at T_A = 10°C to 45°C. The fan/heatsink is shown in Figure 6.

3.7. On-Package Voltage Regulator

The Pentium OverDrive processor with MMX technology has an on-package voltage regulator to supply 2.8 volts to the processor core. This allows the Pentium OverDrive processor with MMX technology to function in a 3.3 volt only system.

3.8. Cache Support

The Pentium OverDrive processor with MMX technology has an enhanced internal cache (2x16KB Total, 4 way set-associative Code and Data caches, each with improved TLBs) and will support the L2 caches supported by the Pentium processor (75-200). The Pentium OverDrive processor with MMX technology supports the Intel 82430 chipsets. **Chipsets with 5V signal levels, 82497/82492 cache controller, and the 82498/82493 cache controller are not supported by the Pentium OverDrive processor with MMX technology.**

3.9. Code Prefetch Queue and Branch Target Buffers

Code should not be written to rely on the specific code prefetch queue or branch target buffer mechanism of a particular processor. With each new generation and family of processors, these mechanisms are subject to change.

3.10. I/O Buffers

The Pentium OverDrive processor with MMX technology buffer models comply with the specifications for the buffer model for the respective original Pentium processor. The circuit topology is the same and the ranges of values in the Pentium OverDrive processor with MMX technology model are within the original Pentium processor ranges. The buffer models used by the Pentium OverDrive processor with MMX technology accurately model flight time and signal quality.

3.11. Test Register Access

The Pentium OverDrive processor with MMX technology have test registers which allow testing of different areas of the processor. These test registers are called Model Specific Registers (MSR). These MSR's are accessed using the RDMSR and WRMSR instructions.

4.0. BIOS AND SOFTWARE

The Pentium OverDrive processor with MMX technology is a drop-in replacement for the respective original Pentium processor. BIOS changes are not normally necessary but might be required. Please call Intel Technical Support hotline if assistance is required. Pentium OverDrive processor with MMX technology is 100% backward software compatible with their respective original Pentium processors.

5.0. ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium processor (75-200) and the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology requires 3.3 volts to power the processor. The voltage to the socket is 3.3 volt and is converted by an on-package voltage regulator to the proper voltage for the processor's internal core voltage plane. The internal 3.3 volt I/O plane is powered from the socket to the processor. The Pentium OverDrive processor with MMX technology looks like a 3.3 volt device externally.

5.1. Power and Ground

For clean on-chip power distribution, the Pentium OverDrive processor with MMX technology in an SPGA package has 60 V_{CC} (power) and 68 V_{SS} (ground) inputs. The 28 V_{CC2} pins are connected internally to a power plane that provides power to the on-package voltage regulator for the core supply. The 32 V_{CC3} pins are connected internally to a separate power plane that provides power to the I/O buffers. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium OverDrive processor with MMX technology. On the circuit board all V_{CC} pins must be connected to a 3.3V V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

The Pentium OverDrive processor with MMX technology pinout contains two 5V V_{CC} pins (V_{CC5}) used to provide power to the fan/heatsink. These pins should be connected to +5 volts ±5% regardless of the system design.

5.2. Decoupling Recommendations

Decoupling recommendation for the original Pentium processor apply to the Pentium OverDrive processor with MMX technology upgradable systems and capacitors should be placed near the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology can cause transient power surges, particularly when driving large capacitive loads. The Pentium OverDrive processor with MMX technology are shipped with adequate decoupling capacitors on the package to limit transients in excess of Pentium processors tolerance. It is recommended to follow the original Pentium processor specification for decoupling recommendations.

5.3. Other Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground. All NC pins must remain unconnected.

5.4. Absolute Maximum Ratings

The tables in this section provide environmental stress ratings for the Pentium OverDrive processor with MMX technology. Functional operation at the absolute maximum and minimum is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability. Furthermore, precautions should be taken to avoid high static voltages and electric fields to prevent static electric discharge. Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. The tables contain stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.

Table 12. Absolute Maximum Ratings without Fan/Heatsink

Symbol	Parameter	Min	Max	Unit	Notes
	Storage Temperature	-40	+125	°C	
	Case Temperature Under Bias	-40	+110	°C	
V_{CC3}	3.3 V Supply Voltage with respect to V_{SS}	-0.5	+4.6	V	
V_{CC5}	5 V Supply Voltage with respect to V_{SS}	-0.5	6.5	V	
V_{IN}	3.3 V Only Buffer DC Input Voltage	-0.5	V_{CC3}+0.5V not to exceed 4.6V MAX	V	(2)
V_{INSB}	5.0V Safe Buffer DC Input Voltage	-0.5	+6.5	V	(1) (3)

NOTES:
1. Applies to the CLK and PICCLK.
2. Applies to all Pentium® OverDrive® processor with MMX™ technology inputs except CLK and PICCLK.
3. See overshoot/undershoot transient specification in the *Pentium® Family User's Manual, Volume 1.*

Table 13. Absolute Maximum Ratings for Fan/Heatsink Only

	Parameter	Min	Max	Unit	Notes
Fan:					
	Storage Temperature	-40	70	°C	
	Case Temperature Under Bias	-5	60	°C	
V_{CC5}	5V Fan Supply Voltage with Respect to V_{SS}	-0.5	6.5	V	

5.5. D.C. Specifications

The Pentium OverDrive processor with MMX technology will have compatible D.C. specifications to the original Pentium processor, except for I_{CC} (Power Supply Current) and I_{CC5} (Fan/Heatsink Current). The Pentium OverDrive processor with MMX technology voltage specification are V_{CC3} = 3.135V to 3.6V and V_{CC5} = 5V ±5%.

Table 14 lists the D.C. specifications which apply to the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology requires a 3.3V power supply and 3.3V input signals with the exception of CLK and signals which are 5V tolerant.

Table 14. 3.3V D.C. Specifications

V_{CC} = 3.135V to 3.6V (See Notes 6, 7), T_A = 10 to 45°C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	-0.3	0.8	V	TTL Level (3)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	TTL Level (3)
V_{OL}	Output Low Voltage		0.4	V	TTL Level (1) (3)
V_{OH}	Output High Voltage	2.4		V	TTL Level (2) (3)
V_{IL5}	Input Low Voltage	-0.3	0.8	V	TTL Level (8)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level (8)
I_{CC5}	Fan/Heatsink Current		200	mA	
I_{CC3}	Power Supply Current		4330	mA	@50/125 MHz (4)(5)
			4330	mA	@60/150 MHz (4)(5)
			4330	mA	@60/180 MHz (4)(5)
			4330	mA	@66/166 MHz (4)(5)
			5000	mA	@66/200 MHz (4)(5)
I_{CC5}	Fan/Heatsink Current		200	mA	
I_{CCSB}	Standby	450	770	mA	

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3 volt TTL levels apply to all signals except CLK and PICCLK.
4. For worst case conditions: V_{CC3}+5% and T_{CASE} = 10°C.
5. Power supply transient response and decoupling capacitors must be sufficient to handle the current transients required when transitioning from standby to full power mode.
6. Refer to Chapter 23 in the *Pentium® Family User's Manual, Volume 1*, for a listing of the remaining D.C. Specifications.
7. The worst case ambient temperature is T_A = 45° C.
8. Applies to 5V safe inputs: CLK and PICCLK.

Table 15. 50-MHz Bus A.C. Specifications

3.135 < V_{CC} < 3.6V, TA = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	25.0	50.0	MHz		Max core Freq = 125 MHz @ 2/5
t_{1a}	CLK Period	20.0	40.0	nS	7	
t_{1b}	CLK Period Stability		±250	pS	7	Adjacent Clocks, (1), (25)
t_2	CLK High Time	4.0		nS	7	@2V, (1)
t_3	CLK Low Time	4.0		nS	7	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-2.0V), (1)
t_{6a}	ADS#, ADSC#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	8	
t_{6b}	AP Valid Delay	1.0	8.5	nS	8	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	8	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	8	(1)
t_8	PCHK#, APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	8	(4)
t_9	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	8	(4)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	8	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	8	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	8	

Table 15. 50-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to 45°C, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	8	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	8	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	9	(1)
t_{14}	A5-A31 Setup Time	6.5		nS	10	
t_{15}	A5-A31 Hold Time	1.0		nS	10	
t_{16a}	INV, AP Setup Time	5.0		nS	10	
t_{16b}	EADS# Setup Time	6.0		nS	10	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	10	
t_{18a}	KEN# Setup Time	5.0		nS	10	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	10	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	10	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	10	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	10	
t_{22}	BOFF# Setup Time	5.5		nS	10	
t_{22a}	AHOLD Setup Time	6.0		nS	10	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	10	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	10	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	10	
t_{25b}	HOLD Hold Time	1.5		nS	10	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	10	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	10	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	10	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	10	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	11	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	10	(12)

Table 15. 50-MHz Bus A.C. Specifications

3.135 < V_{CC} < 3.6V, TA = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	10	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	10	
t_{36}	RESET Setup Time	5.0		nS	11	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	11	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	11	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	11	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	11	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	11	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	11	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	11	To RESET falling edge (20)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	11	To RESET falling edge (20)
t_{42d}	Reset Configuration Signals (BRDYC#) Hold Time, RESET Driven Synchronously.	1.0		nS		To RESET falling edge (1), (27)
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25.0		nS	7	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	13	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	12	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	12	(8)

Table 15. 50-MHz Bus A.C. Specifications

$3.135 < V_{CC} < 3.6V$, TA = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{54}	TDO Float Delay		25.0	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	12	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	12	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	12	(3), (7), (10)

NOTES:

Notes 2, 6, and 13 are general and apply to all standard TTL signals used with the Pentium® OverDrive processor with MMX™ technology.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/nS rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the max TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock. This is not applicable to the Pentium OverDrive processor with MMX technology.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously. However, when operating the Pentium® OverDrive® processor with MMX™ technology, FLUSH# and RESET must be asserted synchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF, BF1, and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency specturm should not have any power spectrum peaking between 500KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. BRDYC# and BUSCHK# are used as Reset configuration signals to select buffer size.
21. The value of this signal may have been changed, check the latest Pentium Processor Data Book for the updated values.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

5.6.2. A. C. TABLES FOR A 60-MHZ BUS

The A.C. specifications given in Table 16 consist of output delays, input setup requirements and input hold requirements for a 60-MHz external bus. All A.C. specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct 180-MHz Pentium OverDrive processor with MMX technology operation.

Table 16. 60-MHz Bus A.C. Specifications

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	30	60.0	MHz		Max core Freq = 150 MHz @ 2/5
t_{1a}	CLK Period	16.67	33.33	nS	7	
t_{1b}	CLK Period Stability		±250	pS	7	Adjacent Clocks, (1), (25)
t_2	CLK High Time	4.0		nS	7	@2V, (1)
t_3	CLK Low Time	4.0		nS	7	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-2.0V), (1)
t_{6a}	ADS#, ADSC#, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	nS	8	
t_{6b}	AP Valid Delay	1.0	8.5	nS	8	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	8	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	9	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	8	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.8	nS	8	(4)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	8	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	8	(4)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	8	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	8	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	8	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	8	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	8	

Table 16. 60-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	9	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	10	
t_{15}	A5-A31 Hold Time	1.0		nS	8	
t_{16a}	INV, AP Setup Time	5.0		nS	8	
t_{16b}	EADS# Setup Time	5.5		nS	8	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	8	
t_{18a}	KEN# Setup Time	5.0		nS	8	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	8	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	8	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	8	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	8	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	8	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	8	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	8	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	8	
t_{25a}	HOLD Hold Time	1.5		nS	8	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	8	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	8	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	8	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	8	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	8	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	8	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.0		nS	8	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	8	

Table 16. 60-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{36}	RESET Setup Time	5.0		nS	9	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	9	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	9	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	9	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	9	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	9	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	9	(15)
t_{42b}	Reset Configuration Signals (FLUSH#, BRDYC#, INIT, BUSCHK#) Hold Time, Async.	2.0		CLKs	9	(20)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	9	(20)
t_{42d}	Reset Configuration Signals (BRDYC#) Hold Time, RESET Driven Synchronously.	1.0		nS		To RESET falling edge (1), (27)
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25.0		nS	7	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	13	Asynchronous, (1)
t_{51}	TDI, TMS Setup Time	5.0		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	12	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	12	(8)
t_{54}	TDO Float Delay		25.0	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	12	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	12	(1), (3), (8), (10)

Table 16. 60-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	12	(3), (7), (10)

NOTES:

Notes 2, 6, and 13 are general and apply to all standard TTL signals used with the Pentium® OverDrive processor with MMX™ technology.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/nS rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the max TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock. This is not applicable to the Pentium OverDrive processor with MMX technology.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously. However, when operating the Pentium® OverDrive® processor with MMX™ technology, FLUSH# and RESET must be asserted synchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF, BF1, and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency specturm should not have any power spectrum peaking between 500KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. BRDYC# and BUSCHK# are used as Reset configuration signals to select buffer size.
21. The value of this signal may have been changed, check the latest Pentium Processor Data Book for the updated values.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

5.6.3. A. C. TABLES FOR A 66-MHZ BUS

The A.C. specifications given in Table 17 consist of output delays, input setup requirements and input hold requirements for a 66-MHz external bus. All A.C. specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct 200-MHz Pentium OverDrive processor with MMX technology operation.

Table 17. 66-MHz Bus A.C. Specifications

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	33.33	66.6	MHz		Max core Freq = 166 MHz @ 2/5
t_{1a}	CLK Period	15.0	30.0	nS	7	
t_{1b}	CLK Period Stability		±250	pS	7	Adjacent Clocks, (1), (25)
t_2	CLK High Time	4.0		nS	7	@2V, (1), (5)
t_3	CLK Low Time	4.0		nS	7	@0.8V, (1), (5)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V),(1),(5)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-.0V),(1),(5)
t_{6a}	ADSC#, PWT, PCD, BE0-7#, D/C#, W/R#, CACHE#, SCYC, Valid Delay	1.0	7.0	nS	8	
t_{6b}	AP Valid Delay	1.0	8.5	nS	8	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	8	
t_{6d}	ADS#, MIO# Valid Delay	1.0	6.0	nS	8	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	9	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	8	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	8	(4)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	8	(4), (21)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	8	(4), (21)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	8	(21)
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	8	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	8	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	8	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	8	(21)

Table 17. 66-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	9	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	10	
t_{15}	A5-A31 Hold Time	1.0		nS	10	
t_{16a}	INV, AP Setup Time	5.0		nS	10	
t_{16b}	EADS# Setup Time	5.5		nS	10	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	10	
t_{18a}	KEN# Setup Time	5.0		nS	10	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	10	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	10	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	10	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	10	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	10	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	10	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	10	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	10	
t_{25b}	HOLD Hold Time	1.5		nS	10	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	10	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	10	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	10	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	10	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	10	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	10	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.0		nS	10	(21)
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	10	(21)

Table 17. 66-MHz Bus A.C. Specifications (Continued)

3.135 < V_{CC} < 3.6V, T_A = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{36}	RESET Setup Time	5.0		nS	11	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	11	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	11	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	11	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	11	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	11	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	11	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#,BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	11	To RESET falling edge (20)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	11	To RESET falling edge (20)
t_{42d}	Reset Configuration Signals (BRDYC#) Hold Time, RESET Driven Synchronously.	1.0		nS		To RESET falling edge (1), (27)
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25.0		nS	7	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	13	Asynchronous, (1)
t_{51}	TDI, TMS Setup Time	5.0		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	12	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	12	(8)
t_{54}	TDO Float Delay		25.0	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	12	(3), (8), (10)

Table 17. 66-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	12	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	12	(3), (7), (10)

NOTES:

Notes 2, 6, and 13 are general and apply to all standard TTL signals used with the Pentium® OverDrive processor with MMX™ technology.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/nS rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the max TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock. This is not applicable to the Pentium OverDrive processor with MMX technology.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously. However, when operating the Pentium® OverDrive® processor with MMX™ technology, FLUSH# and RESET must be asserted synchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF, BF1, and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency specturm should not have any power spectrum peaking between 500KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. BRDYC# and BUSCHK# are used as Reset configuration signals to select buffer size.
21. The value of this signal may have been changed, check the latest Pentium Processor Data Book for the updated values.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

5.6.4. TIMING AND WAVEFORMS

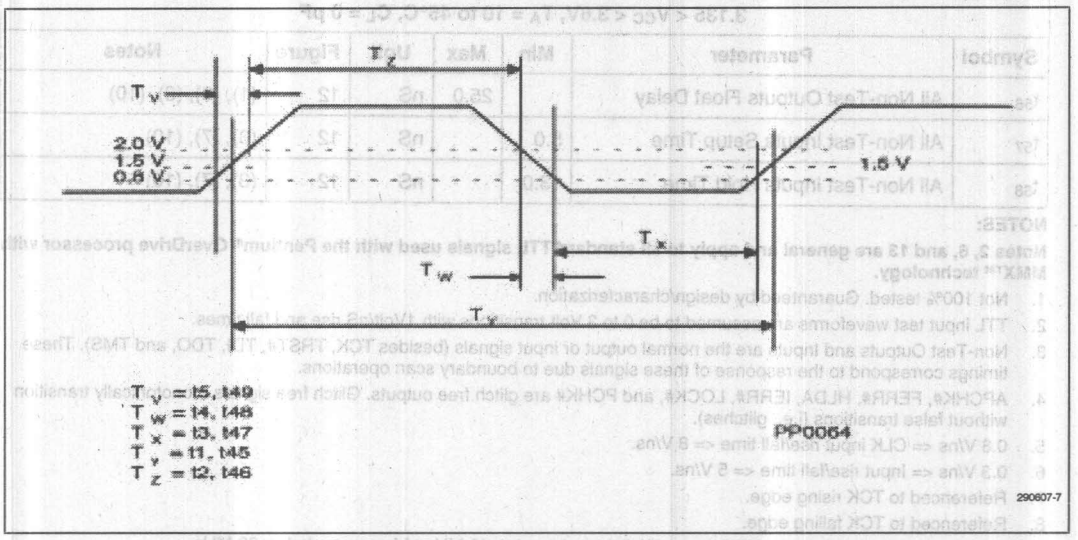


Figure 7. Clock Waveform

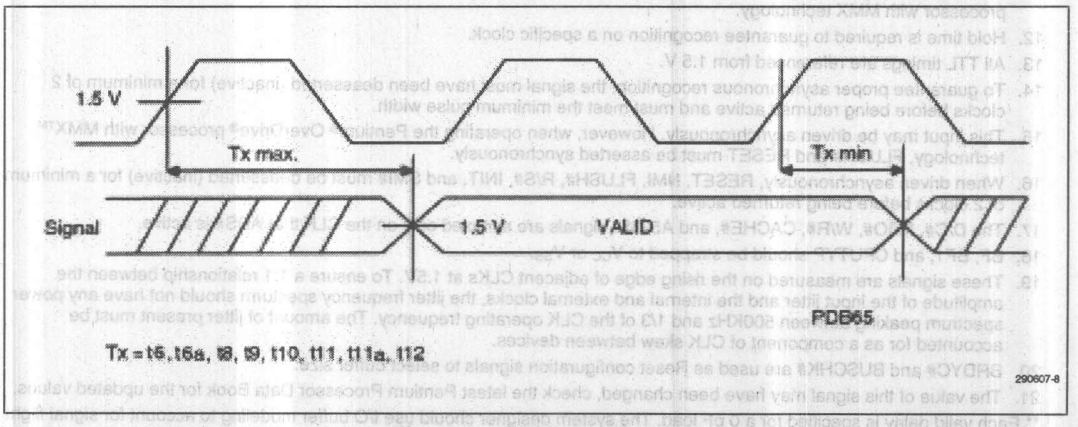


Figure 8. Valid Delay Timing

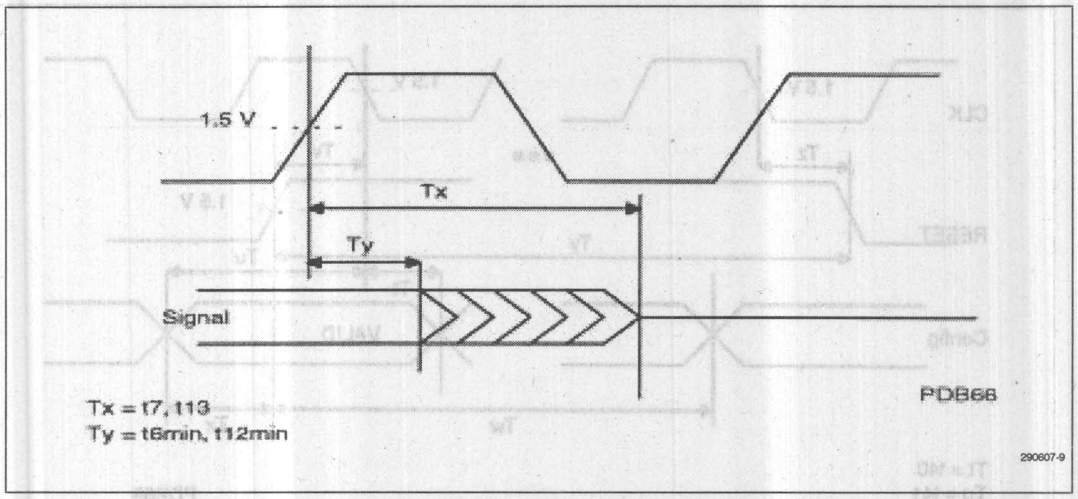


Figure 9. Float Delay Timing

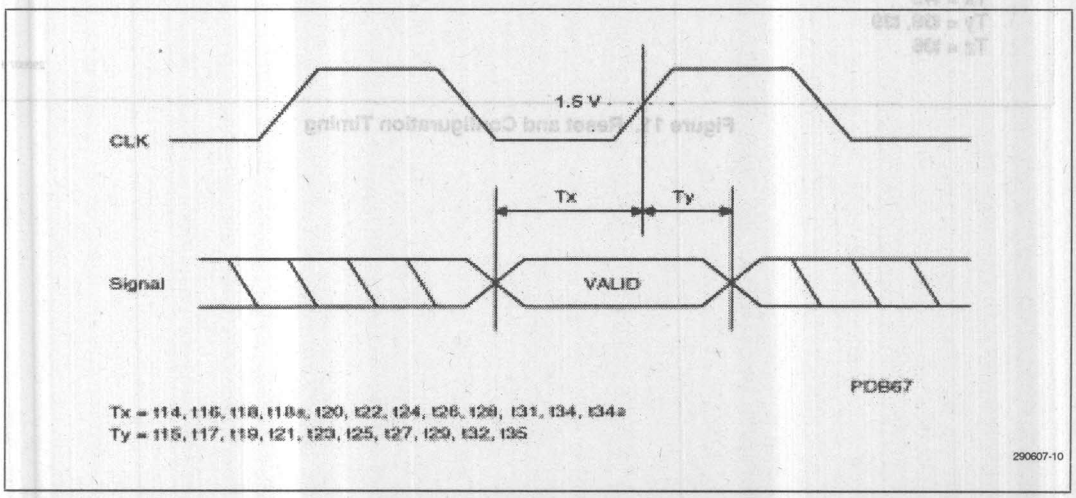


Figure 10. Setup and Hold Timing

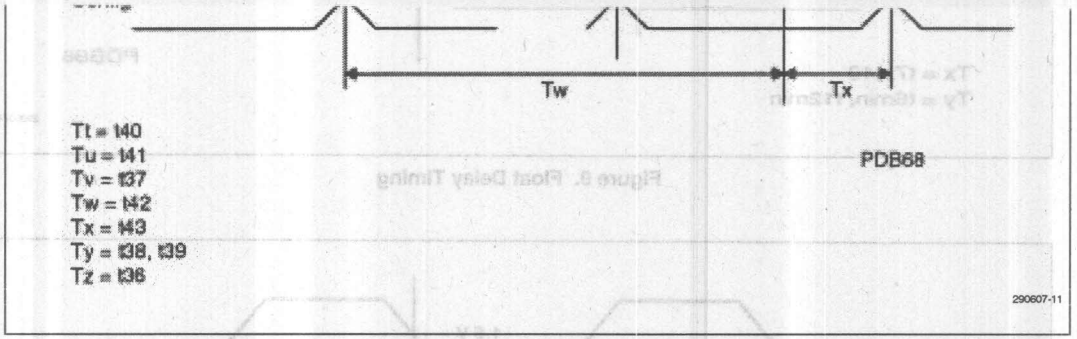


Figure 11. Reset and Configuration Timing

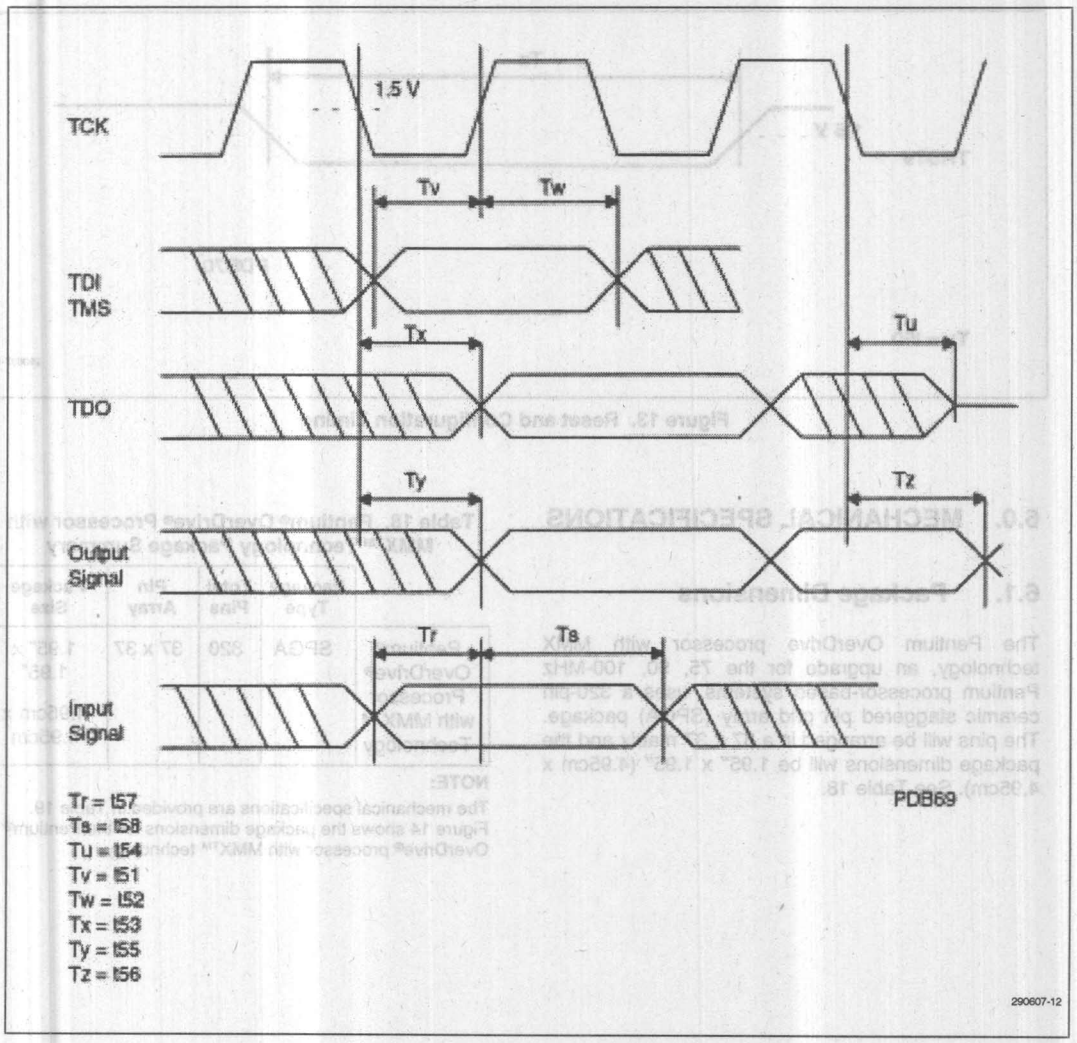


Figure 12. Test Timing

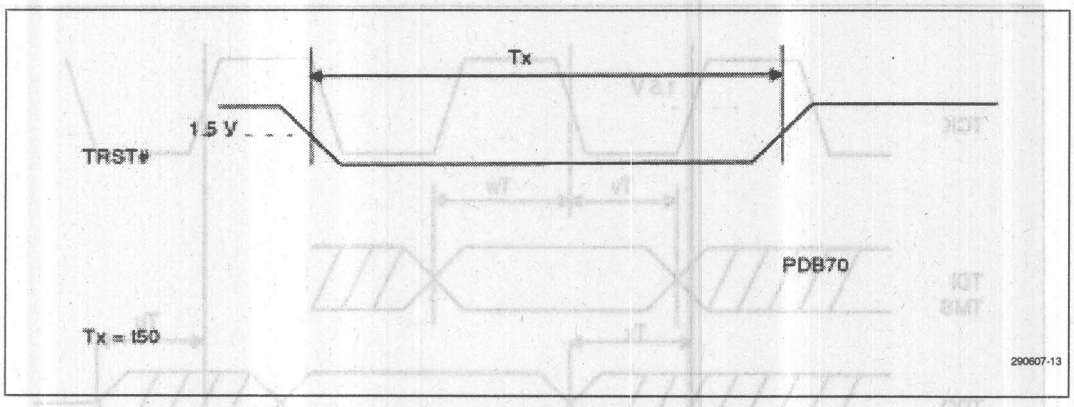


Figure 13. Reset and Configuration Timing

6.0. MECHANICAL SPECIFICATIONS

6.1. Package Dimensions

The Pentium OverDrive processor with MMX technology, an upgrade for the 75, 90, 100-MHz Pentium processor-based systems, uses a 320-pin ceramic staggered pin grid array (SPGA) package. The pins will be arranged in a 37 x 37 matrix and the package dimensions will be 1.95″ x 1.95″ (4.95cm x 4.95cm). See Table 18.

Table 18. Pentium® OverDrive® Processor with MMX™ Technology Package Summary

	Package Type	Total Pins	Pin Array	Package Size
Pentium® OverDrive® Processor with MMX™ Technology	SPGA	320	37 x 37	1.95" x 1.95" 4.95cm x 4.95cm

NOTE:
The mechanical specifications are provided in Table 19. Figure 14 shows the package dimensions for the Pentium® OverDrive® processor with MMX™ technology.

Table 19. Package Dimensions

Family: Ceramic Staggered Pin Grid Array Package						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
A*		33.88	Solid Lid		1.334	Solid Lid
A1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A2	2.62	2.97		0.103	0.117	
A4		20.32			0.800	
A5	10.16		Air Space	0.400		Air Space
B	0.43	0.51		0.017	0.020	
D	49.28	49.91		1.940	1.965	
D1	45.47	45.97		1.790	1.810	
E1	2.41	2.67		0.095	0.105	
E2	1.14	1.40		0.045	0.055	
L	3.05	3.30		0.120	0.130	
N	320		SPGA pins	320		SPGA pins
S1	1.52	2.54		0.060	0.100	

NOTES:

* Assumes the minimum air space above the fan/heatsink.

A 0.2" clearance around three of four sides of the package is also required to allow free airflow through the fan/heatsink.

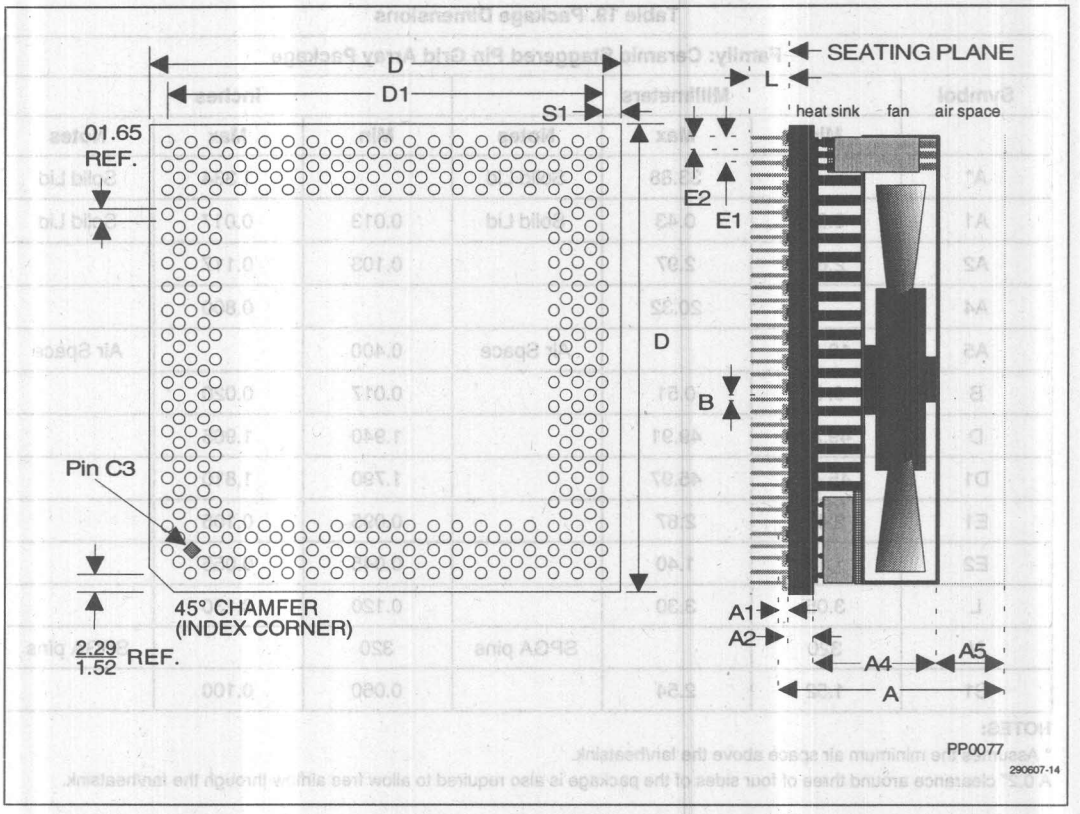
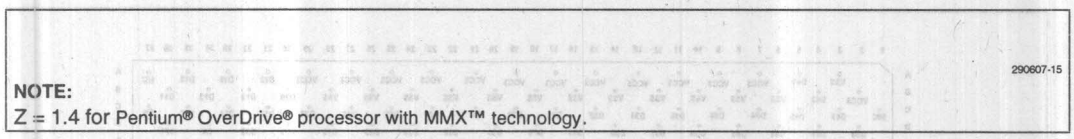


Figure 14. Pentium® OverDrive® Processor with MMX™ Technology Package Dimensions

6.2. Spatial Requirements

The Pentium OverDrive processor with MMX technology employs a fan/heatsink thermal management device. Clearance requirements must be met around the fan/heatsink to ensure unimpeded air flow for proper cooling. Figure 15 shows the Pentium OverDrive processor with MMX technology's fan/heatsink space requirements.

The Pentium OverDrive processor with MMX technology has spatial requirements defined in the respective socket specification that must be met. As shown in Figure 16, it is acceptable to allow any device (i.e., add-in cards, surface mount device, chassis, etc.) to enter within the free space distance of 0.2" from the Pentium OverDrive processor with MMX technology package if it is not taller than the level of the heatsink base. In other words, if a component is taller than height "B," it cannot be closer to the Pentium OverDrive processor with MMX technology package than distance "A". This applies to three of the four sides of the Pentium OverDrive processor with MMX technology package, although the back and handle sides of a ZIF socket will generally automatically meet this specification since they have widths larger than distance "A." Compliance to this requirement will ensure systems can be upgraded to the Pentium OverDrive processor with MMX technology.



NOTE:
Z = 1.4 for Pentium® OverDrive® processor with MMX™ technology.

Figure 15. Illustrates Physical Space Requirements for the Pentium® OverDrive® Processor with MMX™ Technology

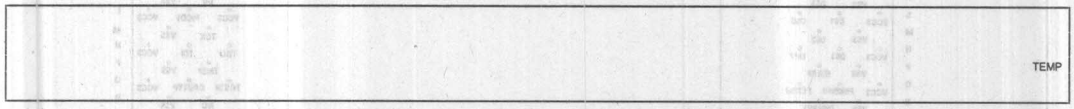


Figure 16. Required Free Space from Sides of SPGA Package

6.3. Socket

6.3.1. SOCKET COMPATIBILITY

Socket 5 (320 pins) and Socket 7 (321 pins) are defined specifically for the requirements of the Pentium OverDrive processor with MMX technology. Socket 5 and Socket 7 define a fifth row of pins in the inside of the 296-pin SPGA socket. The rows "E" and "AJ" are the new rows of pins defined by Socket 5 and Socket 7. Socket 5 and Socket 7 are a superset of the original 75, 90, and 100-MHz Pentium processor (296 pins) pinout.

The Pentium OverDrive processor with MMX technology sockets are compatible with their respective original Pentium processors. To insure proper operation of Pentium OverDrive processor with MMX technology, all power and ground pins should be connected as defined by the respective socket definitions.

6.3.2. SOCKET 5 PINOUT

Socket 5 is the 320-pin ZIF (Zero Insertion Force) socket recommended for the 150/166-Pentium OverDrive processor with MMX technology. The Socket 5 pinout is defined with additional power and ground pins to ensure proper functionality of the Pentium OverDrive processor with MMX technology. The pinout is also specifically defined to ensure proper orientation for the Pentium OverDrive processor with MMX technology.

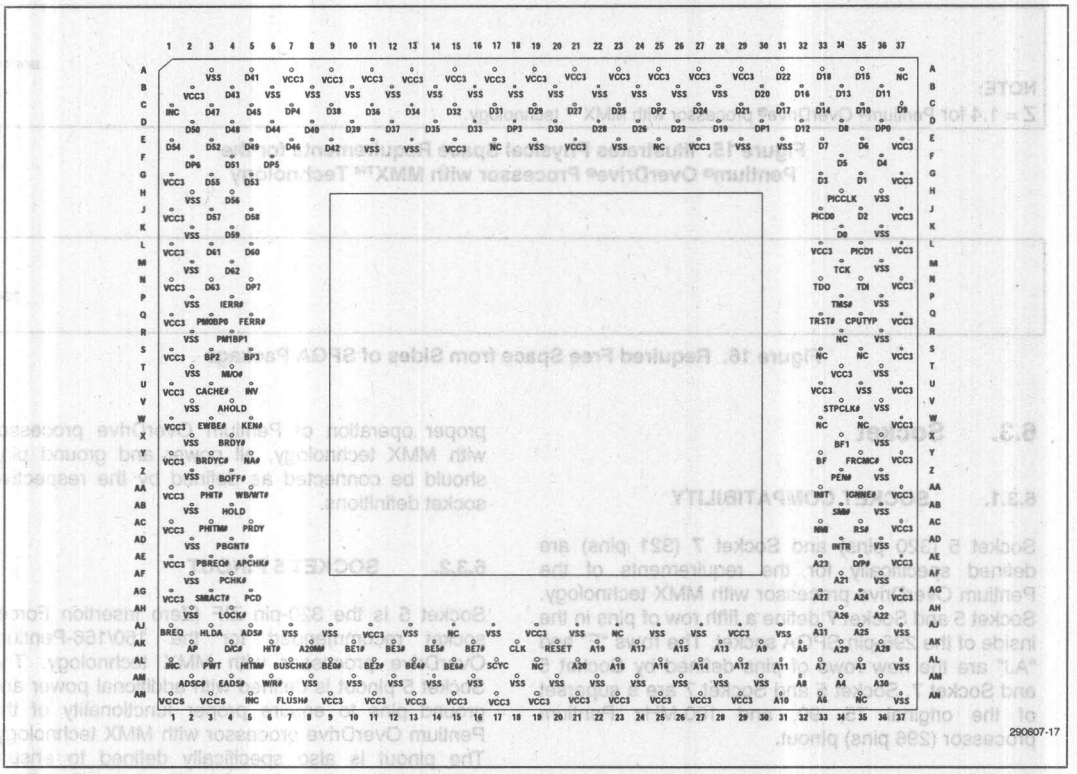
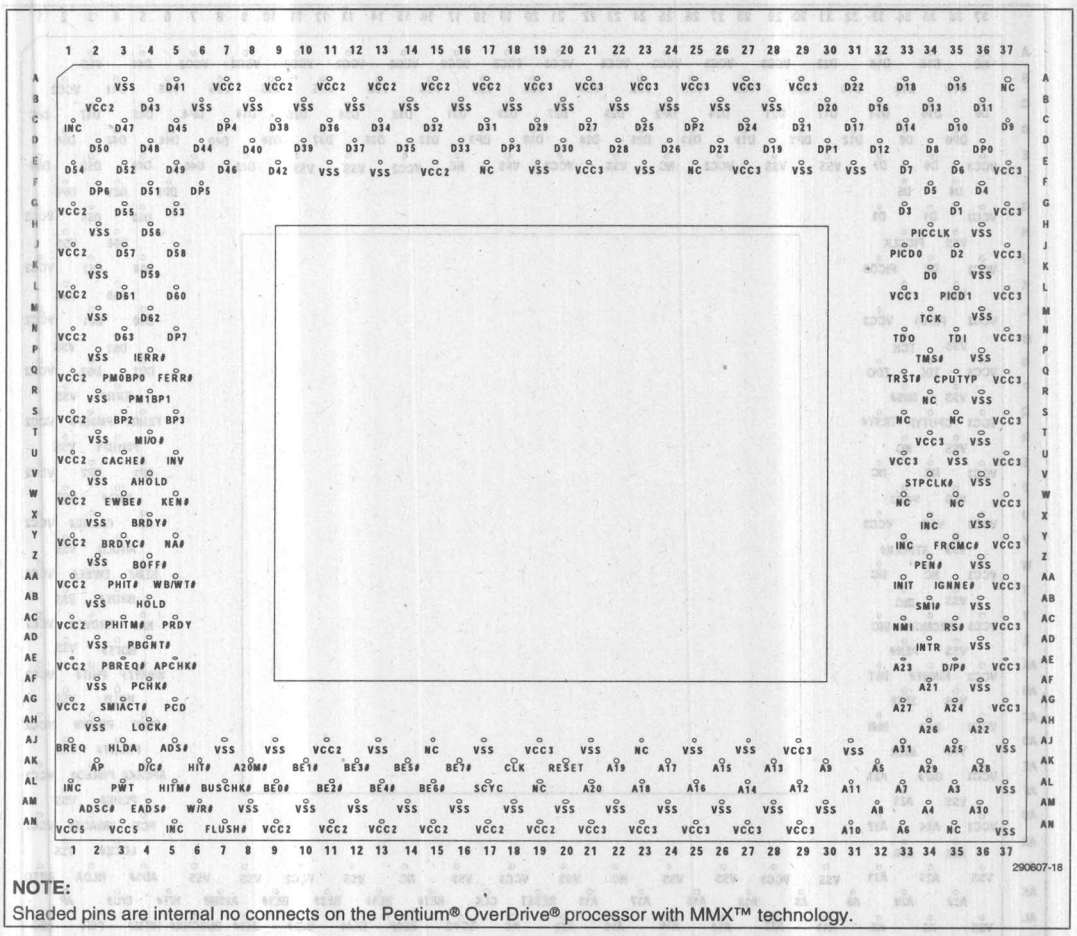


Figure 17. 320-Pin Socket 5

6.3.3. SOCKET 7 PINOUT

Socket 7 is a 321-pin ZIF (Zero Insertion Force) socket recommended for future Pentium and Pentium OverDrive processors and should be used for all new designs. Socket 7 is pin compatible with the 320-pin Socket 5 with the addition of a key pin. Contact Intel for further information.



NOTE:
Shaded pins are internal no connects on the Pentium® OverDrive® processor with MMX™ technology.

Figure 18. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Top Side View

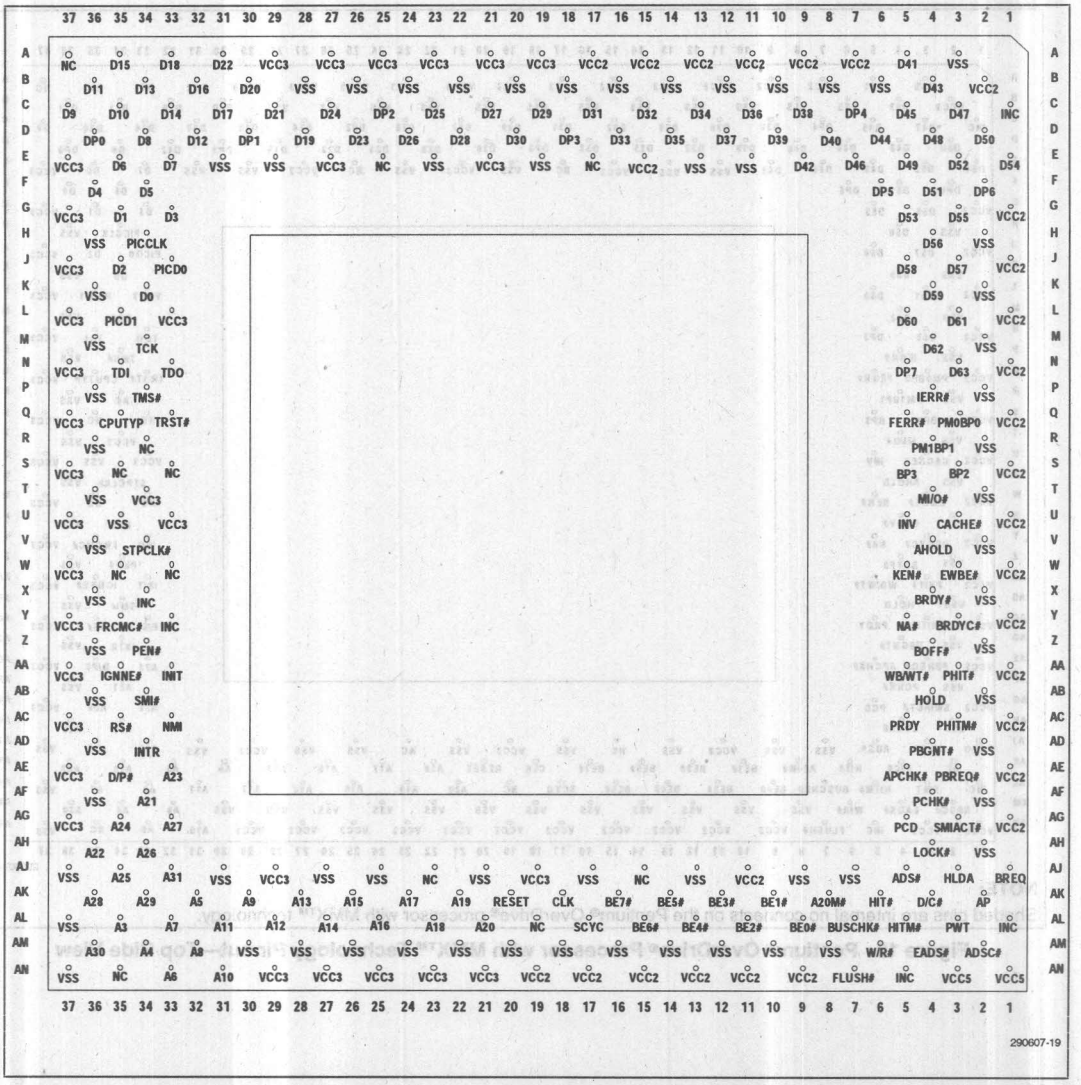


Figure 19. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Pin Side View

7.0. THERMAL SPECIFICATIONS

The Pentium OverDrive processor with MMX technology is shipped with an attached fan/heatsink for a complete thermal solution for the processor upgrade. The fan/heatsink cooling solution will properly cool the Pentium OverDrive processor with MMX technology provided the space requirements of Section 6.2 are met and the maximum air temperature entering the fan/heatsink (T_A) does not exceed 45°C. The fan/heatsink inlet temperature (T_A) is measured 0.3" above the centerline of the fan hub at the system maximum ambient operating temperature (see Figure 15).

8.0. TESTABILITY

8.1. Introduction

This section describes the features which are included in the Pentium OverDrive processor with MMX technology for purposes of testability of the part. The testability features provided for the original Pentium processor are also available on the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology however, does not support the IEEE Standard 1149.1 boundary scan using the Test Access Port (TAP) and TAP Controller as described in Chapters 11 and 27 of the *Pentium® Family User's Manual, Volume 1*. Contact your Intel representative for further details. Some features of testability are described below.

8.2. Built in Self Test (BIST)

Self test is initiated by driving the INIT pin high when RESET transitions from high to low. No bus cycles are run by the Pentium OverDrive processor with MMX technology during self test. The duration of self test is approximately 2^{19} clocks. BIST is used to test approximately 70% of the devices in the Pentium OverDrive processor with MMX technology.

The Pentium OverDrive processor with MMX technology BIST consists of two parts: hardware self test and microcode self test. During the hardware portion of BIST, the microcode and the large PLAs are tested. All possible input combinations of the microcode ROM and PLAs are tested. The microcode self test is done by comparing the stored value of ROM check sums with the result of the self test.

If a mismatch occurs or errors are detected during BIST, the Pentium OverDrive processor with MMX technology will assert the IERR# pin and attempt to shutdown.

8.3. Tri-State Test Mode

When the FLUSH# pin is sampled low in the clock prior to the RESET pin going from high to low, the Pentium OverDrive processor with MMX technology enters tristate test mode. The Pentium OverDrive processor with MMX technology floats all of its output pins and bi-directional pins including pins which are never floated during normal operation (except TD0). Tristate test mode can be initiated in order to facilitate testing of board connections. The Pentium OverDrive processor with MMX technology remains in tristate test mode until the RESET pin is toggled again.

Design Consideration	Implementation
Visible Pentium® OverDrive® Processor with MMX™ Technology Socket	The Pentium OverDrive processor socket should be easily visible when the PC's cover is removed. Label the Pentium OverDrive processor socket and the location of pin 1 by silk screening this information on the PC board.
Accessible Pentium OverDrive Processor Socket	Make the Pentium processor easily accessible to the end user (i.e., do not place the Intel Pentium OverDrive processor socket under the hard disk). If the low insertion force (LIF) is used, position the Pentium OverDrive processor socket on the PC board such that there is ample clearance around the socket.
Foolproof Chip Orientation	Intel packages all Pentium OverDrive processors with a "keyed pin configuration" that insures that the Pentium OverDrive processors fits into the respective sockets in the correct orientation.
Zero Insertion Force Upgrade Socket	The high pin count of the Pentium OverDrive processors often require more than 60 lbs of insertion force for Low Insertion Force (LIF) sockets. A Zero Insertion Force (ZIF) socket insures that the chip insertion force does not damage the PC Board. If the ZIF socket has a handle, be sure to allow enough clearance for the socket handle. If a LIF socket is used, additional PC board support is recommended.
"Plug and Play"	Jumper or switch changes should not be needed to electrically configure the system for the Pentium OverDrive processor.
Thorough Documentation	Describe the Pentium OverDrive processor's installation procedure in the PC's User's Manual.

APPENDIX B

Pentium® OverDrive® Processor with MMX™ Technology ZIF SOCKET VENDORS

The following list provides examples of sockets which can be used for Pentium processor-based systems.

NOTE

This is not a comprehensive list, Intel has not tested all of the Vendor's sockets listed below and cannot guarantee that these will meet every PC manufacturer's specific requirement.

	Socket No.	Style	Drawing No.	Part No.
AMP	Socket 5	SLAZ, OC, T	C-916513	916513
(800) 522-6752	Socket 5	SLAZ, OC, T	C-916560	916560
	Socket 5	SLAZ, OC, T	C-916655	916655
	Socket 5	SLAZ, OC, T	C-916656	916656
	Socket 5	SLAZ, OC, T	C-916671	916671
	Socket 5	SLAZ, OC, T	C-916672	916672
	Socket 7	SLAZ, OC, T	C-916637	916637
	Socket 7	SLAZ, OC, T	C-916657	916657
	Socket 7	SLAZ, OC, T	C-916658	916658
Appros	Socket 5	SLAZ, OC, T	KEA391129	SLR-S19-320-LN2
(408) 567-1234	Socket 7	SLAZ, OC, T	KEA391130	SLR-S19-321-LN2
	Average plating thickness used for qualification testing: 11.2 micro inches gold.			
Augat	Socket 5	SLAZ, OC, T	MP-AX159BCD20	MP-AX159BCD203
(800) 999-7646	Socket 5	SLAZ, OC, T	MP-AX159BCD20A	MP-AX159BCD203A
	Socket 5	SLAZ, OC, T	MP-AX159BCD20B	MP-AX159BCD203B
	Socket 7	SLAZ, OC, T	MP-AX164BCD21X	MP-AX164BCD213
	Socket 7	SLAZ, OC, T	MP-AX164BCD21XA	MP-AX164BCD213A
	Socket 7	SLAZ, OC, T	MP-AX164BCD21XB	MP-AX164BCD213B
	Average plating thickness used for qualification testing sockets: 19 micro inches gold.			

	Socket No.	Style	Drawing No.	Part No.
Berg/Mckenzie	Socket 5	SLAZ, OC, T	SAL B 270086-000	ZIF 97050-4020
(510) 654-2700	Socket 5	SLAZ, OC, T	SAL B 270086-000	ZIF 97050-4120
	Socket 7	SLAZ, OC, T	SAL B 270088-000	ZIF 97054-4020
	Socket 7	SLAZ, OC, T	SAL B 270088-000	ZIF 97054-4120
	Average plating thickness used for qualification testing sockets: 35 micro inches gold			
Foxconn	Socket 5	SLAZ, OC, NT	309-0000-049	PZ32023-0120
(408) 749-1228	Socket 5	SLAZ, OC, T	309-0000-049	PZ32033-0120
	Socket 5	SLAZ, OC, T	309-0000-049	PZ32043-0120
	Socket 5	SLAZ, OC, T	309-0000-049	PZ32053-0120
	Socket 7	SLAZ, OC, T	309-0000-062	PZ32143-0120
	Socket 7	SLAZ, OC, T	309-0000-062	PZ32153-0120
	Average plating thickness used for qualification testing: 10.0 micro inches gold			
JAE	Socket 5	SLAZ, OC, T	SJ029842-E	PCPS-ZL320-A9
(714) 753-2628	Socket 7	SLAZ, OC, T	SJ029842-E	PCPS-ZL321-A9
	Average plating thickness used for qualification testing: Socket 5/7 3.7 micro inched gold Flash/31.4 microinches Palladium Nickel, Socket 8 4.5 micro inched gold Flash/34 micro inches Palladium Nickel.			
Producer	Socket 5	SLAZ, OC, T	PD104-3202	PD104-32025
886-2-202-3578	*Average plating thickness used for qualification testing: 5.7 micro inches gold.*			
Yamaichi	Socket 5	SLAZ, OC, T	KL-13790	NP210-320-0100-CC0
(800) 769-0797	Socket 5	SLAZ, OC, T	KL-13425	NP210-320-0100-CC1
	Socket 5	SLAZ, OC, T	KL-13518	NP210-320-0100-CC2
	Socket 5	SLAZ, OC, T	KL-13930	NP210-320-0100-CC3
	Socket 5	SLAZ, OC, T	KL-13625	NP210-320K13625(D)
	Socket 7	SLAZ, OC, T	KL-13823	NP210-321-0100-CC1
	Socket 7	SLAZ, OC, T	KL-13620	NP210-321-0100-CC2
	Socket 7	SLAZ, OC, T	KL-13938	NP210-321-0100-CC3
	Average plating thickness used for qualification testing: 6.1 micro inches gold.			

intel

Chapter 6: Chipsets for Embedded Applications

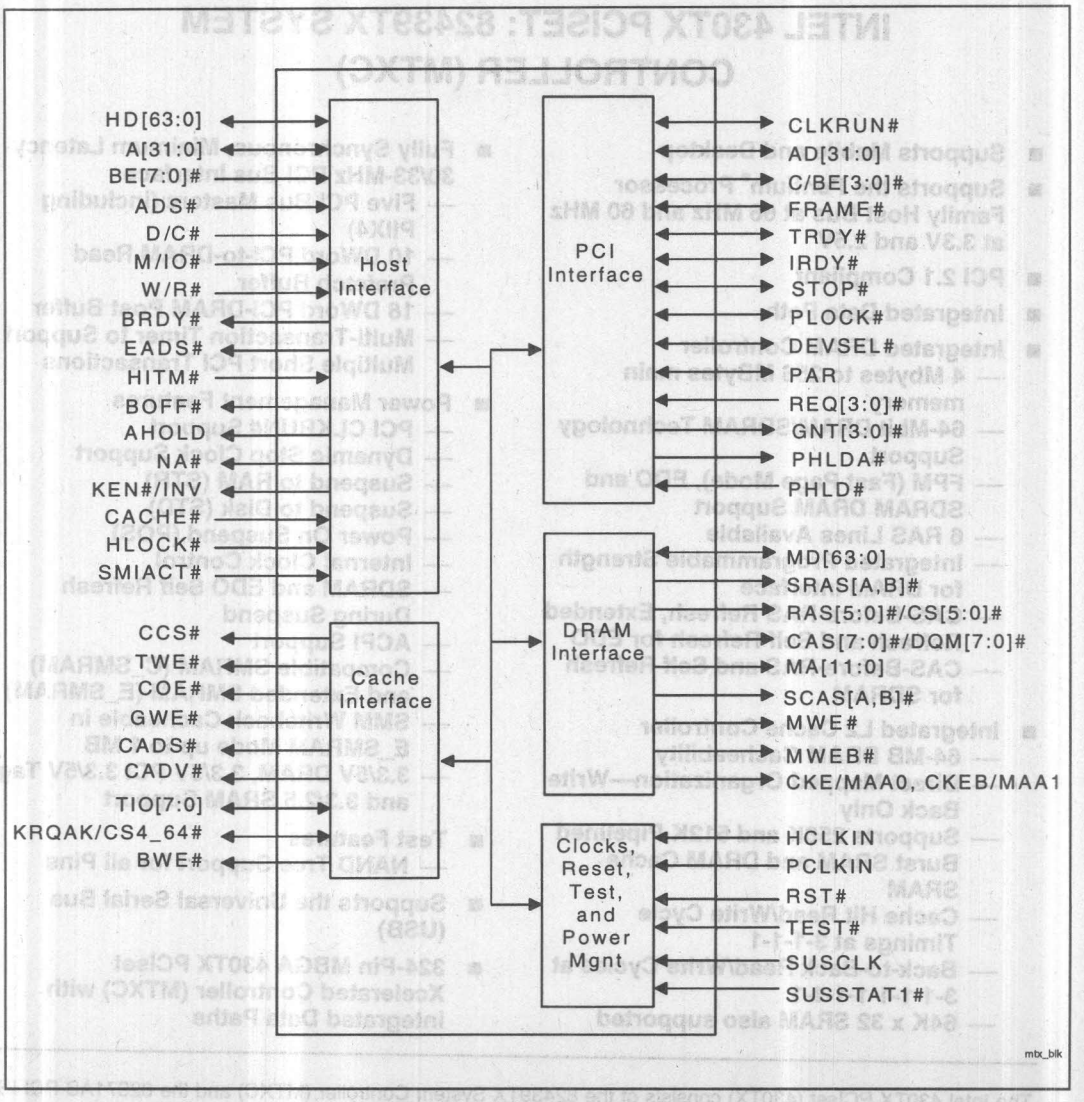
Chapter 6: Chipsets for Embedded Applications

INTEL 430TX PCISET: 82439TX SYSTEM CONTROLLER (MTXC)

- Supports Mobile and Desktop
- Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3V and 2.5V
- PCI 2.1 Compliant
- Integrated Data Path
- Integrated DRAM Controller
  - 4 Mbytes to 256 MBytes main memory
  - 64-Mbit DRAM/SDRAM Technology Support
  - FPM (Fast Page Mode), EDO and SDRAM DRAM Support
  - 6 RAS Lines Available
  - Integrated Programmable Strength for DRAM Interface
  - CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO
  - CAS-Before-RAS and Self Refresh for SDRAM
- Integrated L2 Cache Controller
  - 64-MB DRAM Cacheability
  - Direct Mapped Organization—Write Back Only
  - Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1
  - 64K x 32 SRAM also supported
- Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface
  - Five PCI Bus Masters (including PIIX4)
  - 10 DWord PCI-to-DRAM Read Prefetch Buffer
  - 18 DWord PCI-DRAM Post Buffer
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions
- Power Management Features
  - PCI CLKRUN# Support
  - Dynamic Stop Clock Support
  - Suspend to RAM (STR)
  - Suspend to Disk (STD)
  - Power On Suspend (POS)
  - Internal Clock Control
  - SDRAM and EDO Self Refresh During Suspend
  - ACPI Support
  - Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM)
  - SMM Writeback Cacheable in E_SMRAM Mode up to 1 MB
  - 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support
- Test Features
  - NAND Tree Support for all Pins
- Supports the Universal Serial Bus (USB)
- 324-Pin MBGA 430TX PCIset Xcelerated Controller (MTXC) with integrated Data Paths

The Intel 430TX PCIset (430TX) consists of the 82439TX System Controller (MTXC) and the 82371AB PCI ISA IDE Xcelerator (PIIX4). The 430TX supports both mobile and desktop architectures. The 430TX forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The MTXC integrates the cache and main memory DRAM control functions and provides bus control to transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a writeback cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with pipelined burst SRAMs or DRAM cache SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the MTXC DRAM controller, six rows are supported for up to 256 Mbytes of main memory. The MTXC is highly integrated by including the Data Path into the same BGA chip. Using the snoop ahead feature, the MTXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the MTXC integrates posted write and read prefetch buffers. The 430TX integrates many Power Management features that enable the system to save power when the system resources become idle.

February 1997 Order Number: 290559-001



MTXC Simplified Block Diagram

1.0. ARCHITECTURE OVERVIEW

The MTXC host bridge provides a completely integrated solution for the system controller and datapath components in a Pentium processor system. The MTXC Supports all Pentium family processors since P54C, it has 64-bit Host and DRAM Bus Interface, 32-bit PCI Bus Interface, Second level Cache Interface, and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus (see Figure 1).

The MTXC bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. The MTXC implements 2.5V and 3.3V drivers and 5V tolerant receivers. The MTXC connects directly to the Pentium processor 3.3V or 2.5V host bus, directly to 5V or 3.3V DRAMs, and directly to the 5V or 3.3V PCI bus. The 430TX also interfaces directly to the 3.3V or 5.0V TAGRAM and 3.3V Cache.

The MTXC works with the PCI IDE/ISA Accelerator 4 (PIIX4). The PIIX4 provides the PCI-to-ISA/EIO bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Plug-n-Play port, APIC interface, PCI 2.1 Compliance, SMBUS interface, and Universal Serial Bus Host Controller functions.

DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard (or Fast) Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 6-1-1-1 for SDRAM, 5-2-2-2 for EDO, and 6-3-3-3 for FPM.

The DRAM interface supports 4 Mbytes to 256 Mbytes with six RAS lines. The MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit DRAM and SDRAM technology, both symmetrical and asymmetrical. Parity is not supported, and for loading reasons, x32 and x64 SIMMs/DIMMs/SO-DIMMs should be used.

Second Level Cache

The second level cache is direct mapped and supports both 256-Kbyte and 512-Kbyte SRAM configuration using Pipeline Burst SRAM or DRAM Cache SRAM. The Cache performance is 3-1-1-1 for line read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cacheless configuration is also supported.

PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX4 bus master requests.

Datapath and Buffers

The MTXC contains three sets of data buffers for optimizing data flow. A five QWord deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write backs, and PCI-to-DRAM transfers. This buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides DWord merging and burst merging for CPU-to-DRAM write cycles. In addition, an extra line of buffering is provided that is combined with the DRAM Write Buffer to supply an 18 DWord deep buffer for PCI to main memory writes. A five DWord buffer is provided for CPU-to-PCI writes to help maximize the bandwidth for graphic writes to the PCI bus. Also, five QWords of prefetch buffering has been added to the PCI-to-DRAM read path that allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interfaces directly to the Host and DRAM data bus.

Power Management Features

The MTXC implements extensive power management features. The CLKRUN# feature enables controlling of the PCI clock (on/off). The MTXC supports POS, STR, STD, and Soft-off suspend states. SUSCLK and

SUSSTAT1# signals are used for implementing Suspend Logic. The MTXC supports two SMRAM modes; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). The C_SMRAM is the traditional SMRAM feature implemented in Intel PCIsets. The E_SMRAM is a new feature that supports writeback cacheable SMRAM space up to 1 Mbytes. In order to minimize the idle power, the internal clock in MTXC is turned off (gated off) when there is no activity on the Host and PCI Bus.

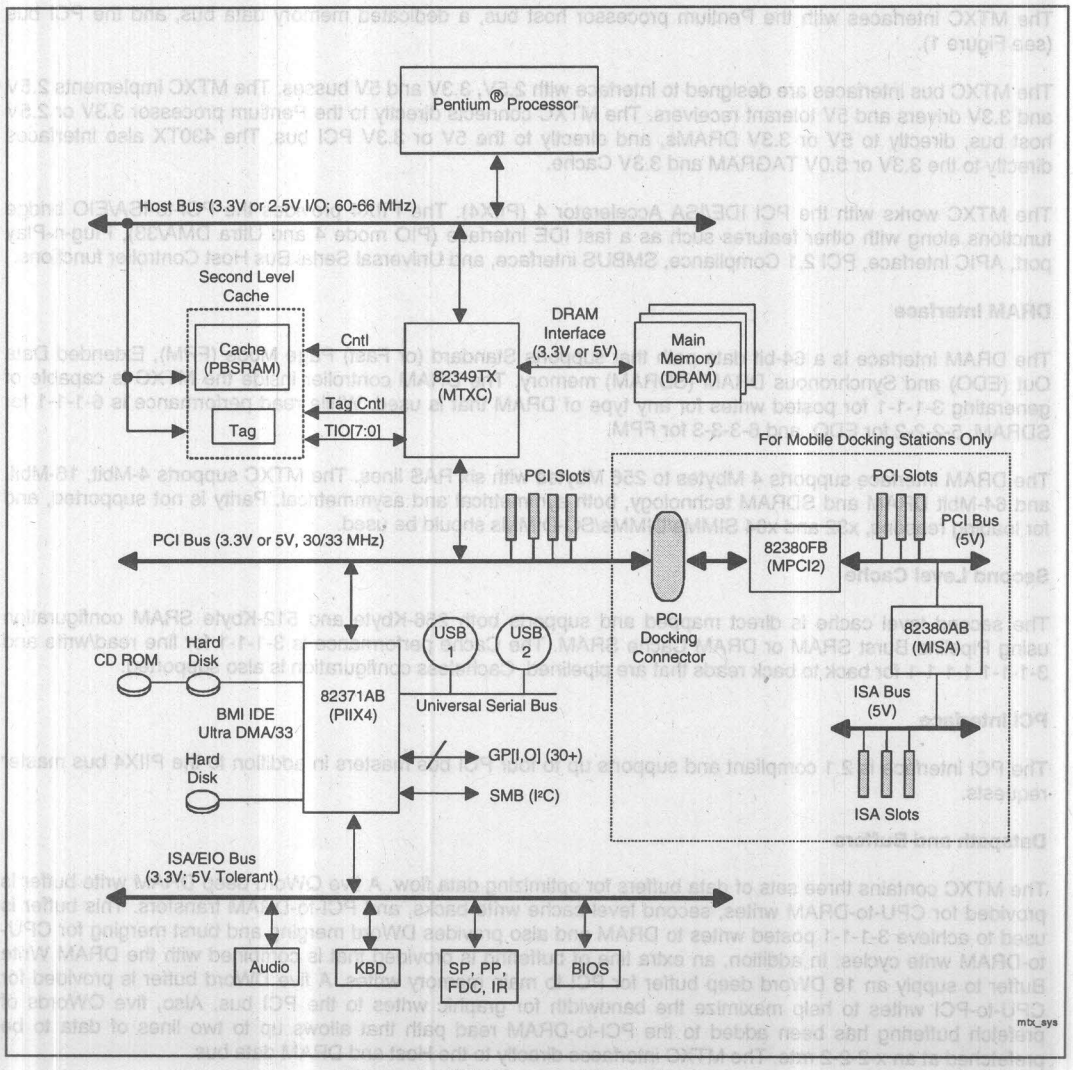


Figure 1. MTXC System Block Diagram

2.0. SIGNAL DESCRIPTION

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

The I/O buffer types are shown below:

Buffer Type	Description
I	input only signal
O	totem pole output
I/O	bi-direction, tri-state input/output pin
s/t/s	sustained tri-state
od	open drain
3.3V/2.5V	Indicates the buffer is 3.3V or 2.5V only, depending on the voltage (3.3V or 2.5V) connected to VccX pins.
3.3V/5V	Indicates that the output is 3.3V and input is 3.3V receiver with 5V tolerance.
5V	Indicates 3.3V receiver with 5V tolerance.

2.1. MTXC Signals

2.1.1. HOST INTERFACE

Name	Type	Description
A[31:3]	I/O 3.3V/2.5V	**Address Bus.** A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The MTXC drives A[31:3] during inquire cycles on behalf of PCI initiators. Bits A[31:26] act as inputs when RST# is active
BE[7:0]#	I 3.3V/2.5V	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3.3V/2.5V	**Address Status.** CPU asserts ADS# in T1 of the CPU bus cycle.
BRDY#	O 3.3V/2.5V	**Bus Ready.** The MTXC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
NA#	O 3.3V/2.5V	**Next Address.** This signal is asserted by the MTXC to indicate to the Processor that it is ready to process a second cycle.

Name	Type	Description
AHOLD	O 3.3V/2.5V	**Address Hold.** The MTXC asserts AHOLD when a PCI initiator is performing a cycle to DRAM. AHOLD is held for the duration of the PCI burst transfer. The MTXC will negate AHOLD when the completion of the PCI to DRAM read or write cycles complete and during PCI peer transfers. AHOLD is kept asserted while PHLDA# is asserted (i.e., duration of PIIX4 granting).
EADS#	O 3.3V/2.5V	**External Address Strobe.** Asserted by the MTXC to inquire the first level cache when servicing PCI master references of DRAM.
BOFF#	O 3.3V/2.5V	**Back Off.** Asserted by the MTXC when required to terminate a CPU cycle that was in progress.
HITM#	I 3.3V/2.5V	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3.3V/2.5V	**Memory/IO; Data/Control; Write/Read.** Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3.3V/2.5V	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI activity to DRAM is allowed.
CACHE#	I 3.3V/2.5V	**Cache.** Asserted by the CPU during a read cycle to indicate the CPU will perform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst writeback cycle. If CACHE# is asserted to indicate cacheability, the MTXC will assert KEN# either with the first BRDY#, or with NA# if NA# is asserted before the first BRDY#.
KEN#/INV	O 3.3V/2.5V	**Ken/Invalidate.** KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV is driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read cycle. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle. Note that KEN#/INV operation during snoop cycles is independent of the FLCE bit programming.
SMIACT#	I 3.3V/2.5V	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of an SMI. This signal must be sampled active with ADS# for the processor to access the SMM space of DRAM, located at A0000h, after SMM space has been loaded and locked by BIOS at system boot.
HD[63:0]	I/O 3.3V/2.5V	**Host Data.** These signals are connected to the CPU data bus. These signals have internal pull-down resistors.

NOTES:

All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights MTXC specific uses of these signals.

2.1.2. DRAM INTERFACE

Name	Type	Description
RAS[3:0]# or CS[3:0]#, RAS4#/CS4#/ BA1, RAS5#/CS5#/ MA13	O 3.3 V	**Row Address Strobe—RASx# (EDO/FPM).** These pins select the DRAM row. **Chip Select—CSx# (SDRAM).** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low. Note: For 64Mbit SDRAM support, BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively. When SDRAMC[bit 1]=1, BA1 and MA13 are driven out on these lines.
CAS[7:0]# or DQM[7:0]	O 3.3 V	**Column Address Strobe (EDO/FPM).** These pins select the DRAM column. **Input/Output Data Mask SDRAM).** These pins act as synchronized output enables during a read cycle and a byte mask during a write cycle. The read cycles require Tdqz clock latency before the functions are actually performed. In case of a write cycle, word mask functions are performed in the same cycle (0 cycle latency).
MA[11:0]	O 3.3 V	**Memory Address (EDO/FPM/SDRAM).** This is the row and column address for DRAM. These buffers now include programmable size selection, as controlled by the DRAMEC[MAD] bit. For 64-Mbit SDRAM support BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively.
MWEB#	O 3.3 V	**Memory Write Enable (second copy) (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
MWE#	O 3.3 V	**Memory Write Enable (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
SRAS[A,B]#	O 3.3 V	**SDRAM Row Address Strobe (SDRAM).** When asserted, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and precharge. Two copies are provided for loading purpose. These signals have programmable buffer size selection.
SCAS[A,B]#	O 3.3 V	**SDRAM Column Address Strobe (SDRAM).** When asserted, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Two copies provided for loading purpose. These signals have programmable buffer size selection.
CKE/MAA0	O 3.3 V	**SDRAM Clock Enable (SDRAM).** SDRAM clock enable pin. When this signal is negated, SDRAM enters power down mode. This signal is also muxed to provide a second copy of memory address MA0 (MAA0). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).

Name	Type	Description
CKEB/MAA1	O 3.3 V	**SDRAM Clock Enable (SDRAM) (second copy).** SDRAM clock enable pin. When this signal is negated, SDRAM enters into power down mode. Note that this signal is not implemented in the "Suspend Well" and should not be used if suspend to RAM (STR) is implemented. This signal is also muxed to provide a second copy of memory address MA1 (MAA1). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
MD[63:0]	I/O 3.3V/5V	**Memory Data.** These signals are connected to the DRAM data bus. These signals have internal pull-down resistors

2.1.3. SECONDARY CACHE INTERFACE

Name	Type	Description
CADV#	O 3.3V	**Cache Advance.** Assertion causes the PBSRAM in the secondary cache to advance to the next QWord in the cache line.
CADS#	O 3.3V	**Cache Address Strobe.** Assertion causes the PBSRAM in the secondary cache to load the PBSRAM address register from the PBSRAM address pins.
CCS#	O 3.3V	**Cache Chip Select (CCS#).** The second level cache will power up, if necessary, and perform an access if this signal is asserted when CADS# is asserted. The second level cache will power down if this signal is negated when CADS# is asserted. When CCS# is negated the second level cache will ignore ADS#. If CCS# is asserted when ADS# is asserted, the second level cache will power up, if necessary, and perform an access.
COE#	O 3.3V	**Cache Output Enable.** The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3.3V	**Global Write Enable.** GWE# assertion causes all the byte lanes to be written into the secondary cache data RAMs, if they are powered up.
BWE#	O 3.3V	**Byte Write Enable.** Asserted low with GWE#=HIGH to enable using host's BE[7:0]# to be used to control byte lanes to pipeline burst SRAM cache.
TIO[7:0]	I/O 3.3V/5V	**Tag Address.** These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. These signals have internal pull-down resistors.
TWE#	O 3.3V	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag.
KRQAK/ CS4_64#	I/O 3.3V	**KRQAK/Chip Select 4 (for 64-Mb Technology).** This pin is a dual-function signal. KRQAK is used in a DRAM Cache L2 implementation and is a bi-directional refresh request/acknowledge. The CS4_64# function is used to generate the fifth chip select line in a SDRAM L2 Cache implementation that supports five rows of 64-Mbit SDRAM. During a hard reset, this signal is sampled to determine if DRAM cache is in the system (see MTXC Strapping options). This signal has a weak internal pull-down. If SDRAMC[bit 1]=1 and DRAM cache is not present in the system (indicated by CEC[bit 5]=0, offset 53h), the CS4_64# function is selected. If DRAM cache is in the system or SDRAMC[bit 1] (offset 54h)=0, then KRQAK is used to drive the KRQAK function.

2.1.4. PCI INTERFACE

Name	Type	Description
AD[31:0]	I/O 3.3/5V	**Address/Data.** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 3.3/5V	**Command/Byte Enable.** The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks.
FRAME#	I/O 3.3/5V	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 3.3/5V	**Device Select.** This signal is driven by the MTXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 3.3/5V	**Initiator Ready.** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 3.3/5V	**Target Ready.** Asserted when the target is ready for a data transfer.
STOP#	I/O 3.3/5V	**Stop.** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 3.3/5V	**Lock.** Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 3.3/5V	**PCI Request.** PCI master requests for PCI bus.
GNT[3:0]#	O 3.3V	**PCI Grant.** Permission is given to the master to use PCI.
PHLD#	I 3.3/5V	**PCI Hold.** This signal comes from the expansion bridge. It is the bridge request for PCI. The MTXC will drain the DRAM write buffers, drain the CPU-to-PCI posting buffers, and acquire the host bus before granting via PHLDA#.
PHLDA#	O 3.3V	**PCI Hold Acknowledge.** This signal is driven by the MTXC to grant PCI to the expansion bridge. PHLDA# protocol has been modified to include support for passive release.
PAR	I/O 3.3/5V	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]. This signal should be pulled high through a weak external pull-up resistor.
CLKRUN#	I/O 3.3/5V	**CLOCK RUN.** An open drain output and also an input. MTXC requests the central resource (PIIX4) to start, or maintain the PCI clock by the assertion of CLKRUN#. MTXC will tri-state CLKRUN# upon negation of reset (since CLK is running upon negation of reset). External pull-up is required. Note: This signal should be connected to the PIIX4 CLKRUN# pin. However, if it is left as a no connect on the MTXC, it must be pulled low through a 100Ω (pull-down resistor.
RST#	I 3.3/5V	**Reset.** When asserted this signal asynchronously resets the MTXC. The PCI signals also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.

2.1.5. TEST AND CLOCK

Name	Type	Description
TEST#	I 3.3/5V	**Test In.** NAND tree mode is activated by driving this pin low. The test mode selected depends on the state of REQ[3:0]#. This pin should be pulled high with an external pull-up during normal operation.
HCLKIN	I 3.3/2.5V	**Host Clock In.** This pin receives a buffered host clock. This clock is used by all of the MTXC logic that is in the Host clock domain.
PCLKIN	I 3.3/5V	**PCI Clock In.** This pin receives a buffered divide-by-2 host clock. This clock is used by all of the MTXC logic that is in the PCI clock domain.

2.1.6. POWER MANAGEMENT

Name	Type	Description
SUSCLK	I 3.3V	**Suspend Clock.** The signal is a 32 KHz input for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh during suspend and non-suspend states is performed based on this clock. This signal has an internal pull-down resistor.
SUSSTAT1#	I 3.3V	**Suspend Status.** SUSSTAT1# indicates MTXC's power plane status during suspend mode. SUSSTAT1#, along with SUSCLK and RST#, define the suspend protocol between MTXC and PIIX4. This signal has an internal pull-up resistor.

2.1.7. POWER AND GROUND PINS

Name	Type	Description
V_{CC}	3.3V	**Main voltage supply.** These pins are the primary voltage supply for the MTXC core and I/O periphery and must be connected to 3.3V.
V_{CC} (CPU)	3.3V or 2.5V	**CPU Interface Voltage Supply.** These pins are the primary voltage supply for the MTXC Host periphery and must be connected to either 2.5V or 3.3V, depending on the voltage level of the CPU interface. Refer to the Power sequencing requirements section for additional details.
V_{CC} (SUS)	3.3V	**Suspend Well Voltage Supply.** These pins are the primary voltage supply for the MTXC suspend logic and I/O. If suspend to RAM is supported, these pins should be on an isolated power plane; otherwise, they can be connected to the same 3.3V source used for the V_{CC} pins.
V_{CC}5REF	3.3V or 5V	**Voltage Reference.** This pin is tied to 5V through a small external power sequencing circuit, if MTXC signals are required to be 5V Tolerant. In a non 5V tolerant system (i.e. 3.3V only system), this signal can be tied directly to V_{CC}. Refer to the Power sequencing requirements section for additional details.
V_{SS}	0V	**Ground.** These pins are the ground for the MTXC.

		of the host clock connected to the host clock pin and the voltage on the Vcc(CPU) pins. An external pull-down or pull-up resistor is required on this pin (pulled down for 2.5V and pulled up for 3.3V).
HFD	A27	**Frequency Detection.** BIOS can use this bit to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping is present) as described in the DRTH Register, bit 7. DRTH[bit 7] register is initialized with the inverted value of pin A27 upon reset negation. The A27 input buffer includes a weak pulldown resistor which will force DRTH[bit 7] to default to 1 if no strapping is present.

2.3. Power Planes

The MTXC has three primary internal power planes. These power planes permit parts of the MTXC to power down to conserve battery life. Table 1 shows the internal planes and their uses.

Table 1. MTXC Internal Power Planes

Power Plane	Description	Signals Powered	Vcc Pins	GND Pins
SUSPEND	Contains the logic needed to resume from the Suspend-to-RAM state. This power supply should be capable of providing a "trickle" current. The input signals attached to the SUSPEND power plane Do Not Support 5V Input Levels. These signals must not exceed Vcc (SUS).	MWE#, MWEB#, CKE, RAS[5:0]# [1], CAS[7:0]#, SUSCLK, SUSSTAT1#	Vcc (SUS)	Vss
CPU	CPU Interface signals have a separate supply so that the CPU interface can be 3.3V for existing CPUs and can be 2.5V on future CPUs.	A[31:3], BE[7:0]#, ADS#, BRDY#, NA#, AHOLD, EADS#, BOFF#, HITM#, M/IO#, D/C#, W/R#, HLOCK#, CACHE#, KEN#/INV, SMIACT#, HD[63:0], HCLKIN	Vcc (CPU)	Vss
Vcc5REF	The Vcc5REF signal provides protection for the 5V tolerant 3.3V signals.	PCI Bus Input and I/O, MD[63:0], TIO[7:0], PCLKIN, TEST#	Vcc5REF	Vss
MAIN	Contains all the rest of the MTXC logic. This plane is powered by the main system power supply.	All Other Signal Pins	Vcc	Vss

NOTES:

1. KRQAK is not part of the suspend well. When this pin is used as the 5th RAS line (CS4_64), special considerations must be taken.

2.4. Power Sequencing Requirements

The Vcc5REF signal must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, Vcc5REF must power up before or simultaneous to Vcc. It must power down after or simultaneous to Vcc. At any time, Vcc5REF should not be more than 0.6 volts below Vcc. In a non-5V tolerant system (3.3V only), this signal can be tied directly to Vcc. In this case, there are no sequencing requirements. Refer to Figure 2 for an example circuit schematic which may be used to ensure the proper Vcc5REF sequencing.

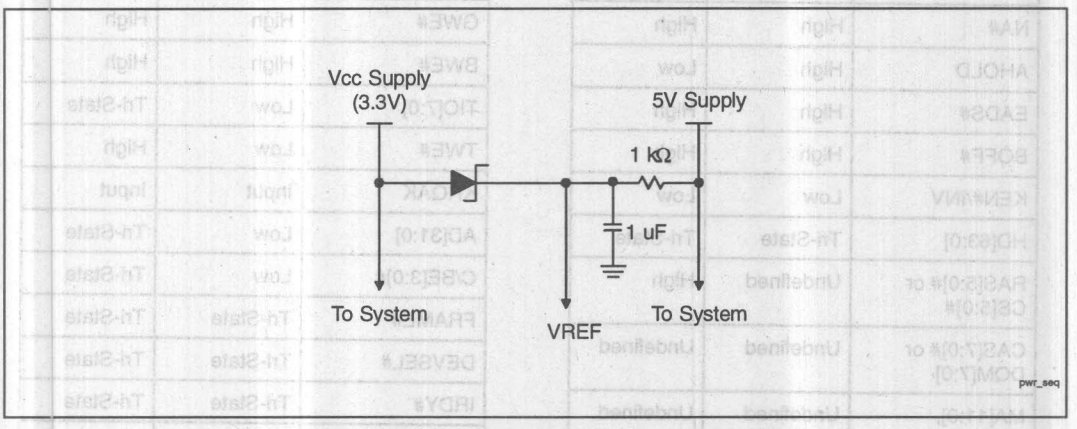


Figure 2. Example Vcc5REF Sequencing Circuit

The Vcc(CPU) power plane is tied to either 2.5 volts or 3.3 volts, depending on the voltage level of the CPU interface. In a system that ties this power plane to 2.5 volts, the Vcc(CPU) pins must power up after or simultaneous to Vcc. It must power down before or simultaneous to Vcc. At any time, Vcc should not be more than 1.2 volts below the Vcc(CPU) plane.

2.5. Signal States During And After A Hard Reset

Table 2 shows the state of all the MTXC output and bi-directional signals when RST# is asserted. An undefined state means that the signal is driven either high or low, but not tri-stated.

Table 2. Signal States During/After Reset

Name	State during RST#	State After RST#
A[31:3]	Low	Tri-State
BRDY#	High	High
NA#	High	High
AHOLD	High	Low
EADS#	High	High
BOFF#	High	High
KEN#/INV	Low	Low
HD[63:0]	Tri-State	Tri-State
RAS[5:0]# or CS[5:0]#	Undefined	High
CAS[7:0]# or DQM[7:0]	Undefined	Undefined
MA[11:0], BA1,MA13	Undefined	Undefined
MWE#, MWEB#	High	High
SRAS[A,B]#	High	High
SCAS[A,B]#	High	High
CKE,CKEB	Undefined	High
MD[63:0]	Tri-State	Tri-State
CADV#	High	High
CADS#	High	High

Table 2. Signal States During/After Reset

Name	State during RST#	State After RST#
CCS#	Low	Low
COE#	High	High
GWE#	High	High
BWE#	High	High
TIO[7:0]	Low	Tri-State
TWE#	Low	High
KRQAK	Input	Input
AD[31:0]	Low	Tri-State
C/BE[3:0]#	Low	Tri-State
FRAME#	Tri-State	Tri-State
DEVSEL#	Tri-State	Tri-State
IRDY#	Tri-State	Tri-State
TRDY#	Tri-State	Tri-State
STOP#	Tri-State	Tri-State
LOCK#	Tri-State	Tri-State
GNT[3:0]#	Tri-State	High
PHLDA#	High	High
PAR	Low	Undefined
CLKRUN#	Tri-State	Tri-State

3.0. REGISTER DESCRIPTION

The MTXC contains two sets of software accessible registers (I/O Mapped and PCI configuration registers), accessed via the Host CPU I/O address space. The I/O mapped registers control access to PCI configuration space. Configuration registers residing in PCI configuration space used to specify PCI configuration, DRAM configuration, cache configuration, operating parameters and optional system features.

The MTXC internal registers (both I/O Mapped and PCI Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes:

RO **READ ONLY**. If a register is read only, writes to this register have no effect.

R/W **READ/WRITE**. A register with this attribute can be read and written.

R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the MTXC registers described in this section contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the MTXC contains address locations in the PCI configuration space that are marked "Reserved" (Table 3). The MTXC responds to accesses to these address locations by completing the Host cycle and returning a value of zero. The registers marked as "Undefined" will return a non-zero value and are defined as read only. Software should not write to reserved or undefined MTXC configuration locations in the device-specific region (above address 3Fh).

Upon RESET, the MTXC sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the MTXC registers accordingly.

3.1. I/O Mapped Registers

The MTXC contains three registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) Register, the Configuration Data (CONFDATA) Register, and the PM2 Register Block. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1. PM2_CNTRL—PM2 REGISTER BLOCK

I/O Address: 0022h
Default Value: 00h
Access: Read/Write

Bit	Descriptions
7:1	**Reserved.**
0	**Arbiter Disable (ARB_DIS).** When ARB_DIS=1, the MTXC does not respond to any REQ# signals (including PHOLD#) going active until this bit is set back to 0. This bit is used to disable bus master accesses prior to placing the CPU in a stop clock state. This bit maintains cache coherency by preventing PCI masters from gaining access to the PCI bus and causing snoop cycle activity. MCTL[Bit 6] (offset 79h) must be set to 1 before this register is accessible.

3.1.2. CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h (Accessed as a DWord)
Default Value: 00000000h
Access: Read/Write

CONFADD is a 32-bit register accessed only when referenced as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register onto the PCI bus. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CONE).** 1=Enable. 0=Disable.
30:24	**Reserved.**
23:16	**Bus Number.** When the Bus Number is programmed to 00h the target of the Configuration Cycle is either the MTXC or the PCI Local Bus that is directly connected to the MTXC, depending on the Device Number field. A type 0 Configuration Cycle is generated on PCI if the Bus Number is programmed to 00h and the MTXC is not the target. If the Bus Number is non-zero a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one of AD[31:11] is driven to a 1. The MTXC is always Device Number 0.
10:8	**Function Number.** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The MTXC responds to configuration cycles with a function number of 000b; all other function number values attempting access to the MTXC (Device Number=0, Bus Number=0) will generate a type 0 configuration cycle onto the PCI bus with no IDSEL asserted, which will result in a master abort.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.1.3. CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write

CONFDATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFADD is 1, any I/O reference that falls in the CONFDATA I/O space is mapped to configuration space using the contents of CONFADD.

PCI CONFIGURATION SPACE MAPPED REGISTERS

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium microprocessor, configuration space is not supported. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The MTXC supports only Mechanism #1. The bus cycles used to access MTXC internal configuration registers are described later in the PCI cycle timings section.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register, a DWord I/O write cycle is used to place a value into CONFADD that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. CONFDATA then becomes a window onto four bytes of configuration space specified by the contents of CONFADD. Any read or write to CONFDATA will result in the MTXC translating CONFADD into a PCI configuration cycle.

Type 0 Access

If the Bus Number field of CONFADD is 0 a Type 0 Configuration cycle is performed on PCI. CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The MTXC is Device #0 and does not pass its configuration cycles to PCI so AD11 will never be asserted. Device #1 will assert AD12, Device #2 will assert AD13, and so forth up to Device #20 which will assert AD31. Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort.

Type 1 Access

If the Bus Number field of CONFADD is non-zero a Type 1 Configuration cycle is performed on PCI. CONFADD[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

Table 3. MTXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
PCI Specific Registers			
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	PCI Command Register	R/W
06–07h	PCISTS	PCI Status Register	RO, R/WC
08	RID	Revision Identification	RO
09–0Bh	CLASSC	Class Code	RO
0Ch	—	Reserved	—
0Dh	MLT	Master Latency Timer	R/W
0Eh	HEDT	Header Type	—
0Fh	BIST	BIST Register	R/W
10–3Fh	—	Reserved	—
MTXC Specific Registers			
40–4Eh	—	Reserved	—
4Fh	ACON	Arbitration Control	R/W
50h	PCON	PCI Control	R/W
51h	—	Reserved	—
52h	CC	Cache Control	R/W
53	CEC	Extended Cache Control	R/W
54–55h	SDRAMC	SDRAM Control	RW
56h	DRAMEC	DRAM Extended Control	R/W
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	R/W
60–65h	DRB[5:0]	DRAM Row Boundary (6 registers)	R/W
66h	—	Reserved	—
67h	DRTH	DRAM Row Type High	R/W
68h	DRTL	DRAM Row Type Low	R/W

Table 3. MTXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
69–6Ah	—	Undefined	RO
6B–6Fh	—	Reserved	—
70h	MTT	Multi-Transaction Timer	R/W
71h	ESMRAMC	Extended System Management RAM Control	R/W
72h	SMRAMC	System Management RAM Control	R/W
73h	—	Reserved	—
74h	—	Undefined	RO
76–78h	—	Reserved	—
78h	—	Undefined	RO
79	MCTL	Miscellaneous Control Register	R/W
7A–FCh	—	Reserved	—
FDh	—	Undefined	RO
FE–FFh	—	Reserved	—

3.1.5. DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 7100h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16 bit value assigned to the MTXC.

3.1.6. PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h
Default: 06h
Access: Read/Write

This 16-bit register provides basic control over the MTXC's ability to respond to PCI cycles. The PCICMD Register in the MTXC enables and disables the assertion of SERR# and PCI master accesses to main memory.

Bit	Description
15:10	**Reserved.**
9	**Fast Back-to-Back (FB2B). (Not implemented)** This bit is hardwired to 0.
8	**SERR# Enable (SERRE). (Not implemented)** This bit is hardwired to 0.
7	**Address/Data Stepping. (Not implemented)** This bit is hardwired to 0.
6	**Parity Error Enable (PERRE). (Not implemented)** This bit is hardwired to 0.
5	**Video Pallet Snooping (VPS). (Not implemented)** This bit is hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE). (Not implemented)** This bit is hardwired to 0. The MTXC will never use the Memory Write and Invalidate PCI command.
3	**Special Cycle Enable (SCE). (Not implemented)** This bit is hardwired to 0, as the MTXC does not respond to PCI special cycles.

Bit	Description
2	**Bus Master Enable (BME). (Not implemented)** This bit is hardwired to 1. The MTXC does not support disabling of its bus master capability on the PCI Bus.
1	**Memory Access Enable (MAE).** When MAE=1, the MTXC permits PCI masters to access main memory if the PCI address selects enabled DRAM space. When MAE=0, the MTXC does not respond to main memory accesses.
0	**I/O Access Enable (IOAE). (Not implemented)** The MTXC does not respond to PCI I/O cycles. This bit is hardwired to 0.

3.1.7. PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h
Default Value: 0200h
Access: Read Only, Read/Write Clear

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort. PCISTS also indicates the DEVSEL# timing that has been set by the MTXC hardware.

Bit	Description
15	**Detected Parity Error (DPE).** This bit is hardwired to 0, as PCI received parity checking is not implemented by the MTXC.
14	**Signaled System Error (SSE).** This bit is hardwired to 0 as MTXC does not support SERR#.
13	**Received Master Abort Status (RMAS).** When the MTXC terminates a Host-to-PCI transaction (MTXC is a PCI master) with an unexpected master abort, this bit is set to 1. Note that master abort is the normal and expected termination of PCI special cycles. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS).** When a MTXC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. Software resets RTAS to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS).** This bit is hardwired to 0, as the MTXC never terminates a PCI cycle with a target abort.
10:9	**DEVSEL# Timing (DEVT).** This 2-bit field indicates the timing of the DEVSEL# signal when the MTXC responds as a target, and is hardwired to the value 01b (medium) to indicate the slowest time that DEVSEL# is generated.
8	**Data Parity Detected (DPD).** This bit is hardwired to 0, as PERR# is not implemented.
7	**Fast Back-to-Back (FB2B).** This bit is hardwired to 0, as fast back to back cycle generation is not implemented.
6	**User Defined Format (UDF).** This bit is hardwired to 0. This is because the MTXC does not contain any configurations that depend on the environment, such as network frequencies.
5	**66-MHz PCI Capable (66C).** This bit is hardwired to 0. The MTXC does not interface to 66-MHz PCI.
4:0	**Reserved.**

3.1.8. RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: 01h
Access: Read Only

This register contains the revision number of the MTXC. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number.** This is an 8-bit value that indicates the revision identification number for the MTXC.

3.1.9. CLASSC—CLASS CODE REGISTER

Address Offset: 09–0Bh
Default Value: 00h
Access: Read Only

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the MTXC. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Description
23:16	**Base Class Code (BASEC).** 06=Bridge device.
15:8	**Sub-Class Code (SCC).** 00h=Host Bridge.
7:0	**Programming Interface (PI).** 00h=Hardwired as a Host-to-PCI Bridge.

3.1.10. MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write

MLT is an 8-bit register that controls the amount of time the MTXC, as a bus master, can burst data on the PCI Bus. The Count Value is an 8-bit quantity. However MLT[2:0] are reserved and assumed to 0 when determining the Count Value. MLT is used to guarantee the host CPU a minimum amount of the system resources.

The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allotted to the MTXC, after which it must surrender the bus as soon as other PCI masters request the bus. The default value of MLT is 00h or 0 PCI clocks.

Bit	Description
7:3	**Master Latency Timer Count Value**
2:0	**Reserved.** Read as 0s

3.1.11. HEDT—HEADER TYPE REGISTER

Address Offset: 0Eh
Default Value: 00h
Access: Read Only

This register contains the Header Type of the MTXC. This code is 00h indicating that the MTXC's configuration space map follows the basic format.

Bit	Description
7:0	**Device Type (DEVICET).** 00h=Indicates a basic configuration space format.

3.1.12. BIST—BIST REGISTER

Address Offset: 0Fh
Default Value: 00h
Access: Read/Write

The Built In Self Test (BIST) function is not supported by the MTXC. Writes to this register have no effect.

Bit	Description
7	**BIST Supported**. This read only bit is always set to 0, disabling the BIST function. Writes to this bit position have no effect.
6	**Start BIST**. This function is not supported and writes have no effect.
5:4	**Reserved.**
3:0	**Completion Code**. This read only field always returns 0 when read and writes have no effect.

3.1.13. ACON—ARBITRATION CONTROL REGISTER

Address Offset: 4Fh
Default Value: 00h
Access: Read/Write

The ACON Register enables and disables features related to PCI arbitration and PCI 2.1 compliance.

Bit	Description
7	**Extended CPU-to-PIIX4 PHLDA# Signaling Enable (XPLDE).** When XPLDE=1, the MTXC adds the following additional signaling to signal PHLDA# (i.e., in addition to the normal CPU/PIIX4 PHOLD/PHLDA# protocol): 1. Whenever the North bridge begins a PCI read/write transaction, it will assert PHLDA# for 1 PCLK within the address phase of the transaction. 2. If the CPU is attempting a LOCKed cycle AND LOCK has been established (i.e. PLOCK# was seen negated in address phase), the PHLDA# remains asserted for one additional clock following the address phase. This bit should be set to 1 anytime both Passive Release and Delayed Transaction are enabled in the PIIX4. Passive release and delayed transaction are enabled via bits 1 and 0 in PIIX4 register 82h (function 0). When bit 7 in this register is set to 1 (enabled), Bit 7 in PIIX4 Register, 6A (Function 0) must also be set to 1. When enabling these two bits, enable Bit 7 in the PIIX4 first, followed by bit 7 in this register. When disabling these two bits, disable Bit 7 in this register first, followed by bit 7 in the PIIX4.
6:0	**Reserved.**

3	**PCI Concurrency Enable (PCE).** 1=CPU can access DRAM and L2 while a non-PIIX4 PCI master is targeting Peer PCI devices. 0 (default)=CPU is held off of the bus during all PCI master cycles. This bit should be set to 1 by BIOS during normal operation.
2:0	**Reserved.**

3.1.15. CC—CACHE CONTROL REGISTER

Address Offset: 52h
Default Value: SSSS0010 (S=Strapping option)
Access: Read/Write

This 8-bit register defines the secondary cache operations. The CC register enables and disables the second level cache, adjusts cache size, selects the cache write policy, selects the caching policy when CACHE# is negated on reads, informs the MTXC how the SRAMs are connected, and defines the cache SRAM type. After a hard reset, CC[7:4] reflect the signal levels on the Host address lines A[31:28].

Bit	Description
7:6	**Secondary Cache Size (SCS).** This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the RESET signal. The options are: **Bits[7:6] — Secondary Cache Size** 00 — Cache not populated 01 — 256 Kbytes 10 — 512 Kbytes 11 — Reserved The RESET values can be overwritten with subsequent writes to the CC Register. **NOTE** 1. When bits[7:6]=00, the secondary cache is disabled. 2. When bits[7:6]≠00, the FLCE bit must also be set to 1 (L2 cache cannot be enabled unless the L1 cache is also enabled).

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>5:4</td><td>L2 SRAM Type (L2SRAMT). This field reflects the inverted signal level on the A[29:28] pins at the rising edge of the RESET signal. The RESET values can be overwritten with subsequent writes to the CC Register. The options are:

Bits[5:4] SRAM Type
00 Pipelined Burst SRAM
01 Reserved
10 Reserved
11 Two banks of Pipelined Burst

NOTE
When 512-KB Pipelined Burst SRAM L2 mode is selected (via SCS and SRAMT), CCS# is negated after NA# is asserted, and reasserted after a pipelined ADS# is detected. CADS# is asserted along with the final BRDY# for a cycle if a pipelined cycle is outstanding (i.e., an ADS# was detected).</td></tr>
<tr><td>3</td><td>NA Disable (NAD). 1=Disable. 0=Enable. When disabled, MTXC never asserts the NA# pin. When enabled, NA# assertion is dependent on the cache type and size selected (via SRAMT, SCS). Note that NAD must be set to 1 if the NA# pin of the MTXC is not connected to the processor. This bit should be set to 0 for normal operation in systems that connect NA# to the processor.</td></tr>
<tr><td>2</td><td>Reserved.</td></tr>
<tr><td>1</td><td>Secondary Cache Force Miss or Invalidate (SCFMI). When set to a 1, the L2 hit/miss detection is disabled, and all tag lookups result in a miss. If the L2 is enabled, then the cycle is processed as a miss (as described in Chapter 4.2). If the L2 is populated but disabled (FLCE=0), then when SCFMI is set to a 1, any CPU read cycle will invalidate the selected tag entry. When SCFMI is set to a 0, normal L2 cache hit/miss detection and cycle processing occurs.

Software can flush the cache (cause all modified lines to be written back to DRAM) by setting SCFMI to a 1 with the L2 enabled (non-zero SCS, FLCE=1), and reading all L2 cache tag address locations. See FLCE bit description for FLCE/SCFMI interaction.</td></tr>
<tr><td>0</td><td>First Level Cache Enable (FLCE). 1=Enable. 0=Disable. When FLCE=1, the MTXC responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE=0, KEN# is always negated. This prevents new cache line fills to either the first level or second level cache.

The FLCE/SCFMI interaction is summarized below. Note that “Normal L2 operation” is further dependent on the SCS field programming.

FLCE SCFMI L2 Result
0 0 L2 disabled
0 1 L2 disabled, MTXC tag invalidate on reads
1 0 Normal L2 operation (dependent on SCS)
1 1 L2 enabled, MTXC miss forced on reads/writes (Note that writes to the cache are also forced as misses, making it possible to create incoherent DRAM/L2 data.)</td></tr>
</table>

3.1.16. CEC—EXTENDED CACHE CONTROL REGISTER

Address Offset: 53h
Default Value: 14h
Access: Read/Write, Read Only

This 8-bit register defines the refresh rate (in HCLKs) for a DRAM CACHE L2 cache implementation, if enabled.

Bit	Description
7:6	**Reserved**
5	**DRAM CACHE L2 Present (ML2)—RO.** When ML2=1, an L2 DRAM CACHE is present.
4:0	**DRAM Cache L2 Refresh Timer (MCRT)—R/W.** These bits determine the time the MTXC remains idle during a DRAM cache refresh sequence. The smallest value for the MRCT must be 04h; otherwise, the MTXC will not function properly. The default value sets the timer refresh to 20 HCLKs.

3.1.17. SDRAMC—SDRAM CONTROL REGISTER

Address Offset: 54–55h
Default Value: 0000h
Access: Read/Write

Bit	Description
15:9	**Reserved.**
8:6	**Special SDRAM Mode Select (SSMS).** These bits select 1 of 4 special SDRAM modes for testing and initialization. Note that the NOP command must be programmed first before any other command can be issued. After the DRAM detection process has completed, bits[7:5] must remain at "000" during normal DRAM operation. **Bits[8:6] Mode** 000 **Normal SDRAM mode (default).** 001 **NOP Command Enable (NOPCE).** This mode forces all CPU cycles to DRAM to generate a SDRAM NOP command on the memory interface. 010 **All Banks Precharge Command Enable (ABPCE).** This setting enables a mode where all CPU cycles to DRAM are converted to an all banks precharge command on the memory interface. Used for BIOS Detection algorithm. 011 **Mode Register Command Enable (MRCE).** This setting enables a mode where all CPU cycles to DRAM are converted into MRS commands to the memory interface. The command is driven on the MA[11:0] lines. MA[2:0] needs to be always driven to 010 for burst of 4 mode. MA3 needs to be always driven to 1 for interleave wrap type mode. MA4 needs to be driven to the value in the CAS# Latency bit. MA[6:5] needs to be always driven to 01. MA[11:7] needs to be always driven to 00000. The BIOS will select an appropriate host address for each Row of memory such that the right commands are generated on the Memory Address MA[11:0] lines. The BIOS needs to be cognizant of the mapping of the Host addresses to Memory addresses. e.g. A Host address of 1D0h will set up the Mode registers in Row 0 of SDRAM with Burst length of 4, Wrap type of interleaved, and CAS latency of 3. 100 **CBR Cycle Enable (CBRC).** This setting enables a mode where all CPU cycles to DRAM are converted to SDRAM CBR refresh cycles on the memory interface. 101 **Reserved** 11X **Reserved**

Bit	Description
5	**RAS# to CAS# Override (RCO).** When set to 1, and the CL bit (CAS Latency) is 0 (CAS Latency=3), then a RAS# to CAS# delay of 2 HCLKs is provided for SDRAM. When set to 0, a RAS# to CAS# delay for SDRAM is determined by the CL bit.
4	**CAS# Latency (CL).** When set to 1, a CAS# latency of 2 is used for all SDRAM cycles. When reset to 0, CAS# latency of 3 is used for all SDRAM cycles.
3	**RAS# Timing (RT).** This bit controls RAS# precharge, RAS# active to precharge time and Refresh to RAS# active delay (in HCLKs): **Bit 3 — RAS# Precharge — RAS# act. to Precharge — Refresh to RAS# act.** 0 — 3 — 5 — 8 1 — 3 — 4 — 7
2	**Reserved.**
1	**64-Mbit Technology Enable (64MTEN).** 1=Enable. 0=Disable. When set to 0, the MTXC does not support 64-Mbit SDRAM devices. In this mode, the MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit technology for EDO/FPM systems and 4 Mbit and 16 Mbit for SDRAM systems (i.e., 64 Mbit not supported in SDRAM systems). When set to 1, the MTXC supports 4 Mbit, 16 Mbit, and 64 Mbit for both SDRAM and EDO/FPM devices. In this mode, the RAS#/CS5# signal becomes RAS#/CS5#/MA13, RAS4#/CS4# becomes RAS4#/CS4#/BA1, and KRQAK/CS4_64# becomes CS4_64#. CS4_64# (fifth row) function is provided if this signal is set to 1 and DRAM Cache is not present in the system (indicated by a 0 in bit 5, register 53h).
0	**Reserved.**

Table 4 lists the CAS# Latency, RAS# to CAS#, RAS# Precharge, RAS# Active to Precharge and Refresh to RAS# active programmable timings.

Table 4. Programming Timings

Operating Frequency	CAS Latency (CL)	RAS# to CAS# (Trcd)	RAS# Precharge (Trp)	RAS# active to Precharge (Tras)	Refresh to RAS# (Trc)	Register 54h Bits[5:3]
60/66 MHz	3 HCLKs	3 HCLKs	3 HCLKs	5 HCLKs	8 HCLKs	000
60/66 MHz	3 HCLKs	2 HCLKs	3 HCLKs	5 HCLKs	8 HCLKs	100
60/66 MHz	2 HCLKs	2 HCLKs	3 HCLKs	4 HCLKs	7 HCLKs	011

3.1.18. DRAMEC—DRAM EXTENDED CONTROL REGISTER

Address Offset: 56h
Default Value: 52h
Access: Read/Write

This 8-bit register contains additional controls for main memory DRAM operating modes and features.

Bit	Description
7	**Reserved.**
6	**Refresh RAS# Assertion(RRA).** 1=5 clocks (RAS# asserted for Refresh cycles). 0=4 clocks.
5	**Fast EDO Lead Off (FELO).** 1=Enables fast timing EDO read cycles. 0=Disable. This is valid for EDO DRAMs only (in both a synchronous cache and a Cacheless system). This result is a 1 HCLK pull-in for all read leadoff latencies for EDO DRAMs. (i.e., Page hits, Page misses, and Row Misses). This bit must be 0 if any of the DRAM rows is populated with FPM DRAMs.
4	**Speculative Lead Off (SLD).** If set to 0, the DRAM Controller read request is presented before the final memory target (Cache/DRAM/PCI) has been decoded by the MTXC. This results in a 1 HCLK pull-in for all read leadoff latencies. Note that if the cycle does not actually target DRAM, the DRAM cycle is later terminated. The SLD bit applies to EDO/FPM and SDRAM. This bit should be set to 1 in systems with a L2 cache and to 0 for systems without a L2 cache
3	**Reserved.**
2:1	**Memory Address Drive Strength (MAD).** This field controls the strength of the output buffers driving the MA, SRASx#, SCASx#, MWEx# and CKEx pins. It is recommended that series termination or undershoot and overshoot diodes be used on these lines. **Bit[2:1] MA[13,11:0], BA1 SRAS[A,B],SCAS[A,B], MWEx#, CKEx** 00 10 mA 10 mA 01 10 mA 16 mA 10 16 mA 10 mA 11 16 mA 16 mA Setting Memory Address Drive Strength: **1 Row 2 Row 3 Row 4 Row 5 Row 6 Row** 00 00 11 11 11 01* * Assuming All Rows are buffered
0	**Reserved.**

3.1.19. DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h
Default Value: 01h
Access: Read/Write

This 8-bit register controls main memory DRAM operating modes and features.

Bit	Description
7:6	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. CPU cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole will be ignored by the MTXC (no DEVSEL#). Note that a selected hole is not remapped. **Bits[7:6] — Hole Enabled** 00 — None 01 — 512 KB–640 KB (128 Kbytes) 10 — 15 MB–16 MB (1 Mbyte) 11 — 14 MB–16 MB (2 Mbytes)
5	**Reserved.**
4	**Enhanced Paging Disable (EPD).** 1=MTXC keeps page open until a page/row miss. When EPD=0, the MTXC uses additional information to keep the DRAM page open when the host may be "right back". See DRAM section for additional information. This bit should be set to 0 for normal operation.
3	**EDO Detect Mode Enable (EDME).** 1=Enables a special timing mode for BIOS to detect EDO DRAM type on a bank-by-bank basis. Once all DRAM row banks have been tested for EDO, the EDME bit should be set to 0. Otherwise, performance will be seriously impacted.
2:0	**DRAM Refresh Rate (DRR).** The DRAM refresh rate for "FPM/EDO only" DRAM subsystem is adjusted according to the value selected by this field. DRAM refresh is implemented using SUSCLK. **Bits[2:0] — DRAM Refresh Rate** 000 — Refresh Disabled (results in the eventual loss of DRAM data) 001 — 15.6 µs 010 — 31.2 µs (for EDO/FPM only memory subsystem) 011 — 64.4 µs (for EDO/FPM only memory subsystem) 100 — 125 µs (for EDO/FPM only memory subsystem) 101 — 256 µs (for EDO/FPM only memory subsystem) 110 — Reserved 111 — Reserved **NOTES** 1. If any of the row is populated with SDRAMs, this field must be set to 15.6 µs refresh rate. 2. Selecting refresh rate of 125 µs or 256 µs may violate the max RAS# active time DRAM specification. It is up to the system designer to make sure this does not happen.

3.1.20. DRAMT—DRAM TIMING REGISTER

Address Offset: 58h
Default Value: 00h
Access: Read/Write

This 8-bit register controls main memory DRAM timings. For SDRAM specific timing control, see the SDRAMC timing register definition.

Bit	Description
7	**Reserved.**
6:5	**DRAM Read Burst Timing (DRBT).** The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register. The x322 timings for EDO Burst rate should be used only when the Fast EDO Path Select (FEPS) bit is set to 1 and the timings for the EDO Burst rate for X222 have a negative margin. This forces the MXS to be negated after the leadoff; thus, selecting the fast path for the leadoff and the slow path for the burst cycles. When FEPS=1 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the fast path for both leadoff and the burst cycles. When FEPS=0 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the slow path for both leadoff and the burst cycles. **DRBT — EDO Burst Rate — FPM Burst Rate** 00 — x444 — x444 01 — x333 — x444 10 — x222 — x333 11 — Reserved — Reserved
4:3	**DRAM Write Burst Timing (DWBT).** The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. **DWBT — EDO/FPM Burst Rate — DWBT — EDO/FPM Burst Rate** 00 — x444 — 10 — x222 01 — x333 — 11 — Reserved
2	**Reserved.**

Bit	Description
1:0	**DRAM Leadoff Timing (DLT)**. The DRAM leadoff timings are controlled by the DLT bits. Slower leadoffs may be required in certain system designs to support loose layouts or slower memories. The Row Miss leadoff timings are summarized below for EDO/FPM reads and writes. Changing DLT affects the Row Miss and Page Miss timings only (e.g., DLT=01 is one clock faster than DLT=00 on Row Miss and Page Miss timings). These bit control MA setup to CAS# assertion. DLT does not affect page hit timings. Thus, DLT=00 or DLT=01 has same page hit timings for reads and writes (e.g., for reads, it would be 10-3=7 clocks for DLT=00 or DLT=01)

DLT	Read Leadoff	Write Leadoff	RAS# Precharge	RAS-to-CAS Delay
00	11	7	3	4
01	10	6	3	3
10	11	7	4	4
11	10	6	4	3

SLD and FELO bits have cumulative effect on the leadoff timings. The above leadoff represent timings with SLD=1 and FELO=0.

3.1.21. PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: 59h (PAM0) (5Fh (PAM6)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits (each register)

The MTXC allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 640-Kbytes to 1-Mbyte address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Three bits are used to specify L1 cacheability and memory attributes for each memory segment. These attributes are:

RE **Read Enable**. When RE=1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE=0, the CPU read accesses are directed to PCI.

WE **Write Enable**. When WE=1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE=0, the CPU write accesses are directed to PCI.

CE **Cache Enable**. When CE=1, the corresponding memory segment is L1 cacheable. CE must not be set to 1 when RE is reset to 0 for any particular memory segment. When CE=1 and WE=0, the corresponding memory segment is cached in the first level cache only on CPU code read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only. The characteristics for memory segments with these read/write attributes are described in Table 5.

Table 5. Attribute Definition

Read/Write Attribute	Definition
Read Only	Read cycles: CPU cycles are serviced by the DRAM in a normal manner. Write cycles: CPU initiated write cycles are ignored by the DRAM interface as well as the cache. Instead, the cycles are passed to PCI for termination. Areas marked as Read Only are L1 cacheable for Code accesses only. These regions are not cached in the second level cache.
Write Only	Read cycles: All read cycles are ignored by the DRAM interface as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. Write cycles: CPU write cycles are serviced by the DRAM and L2 cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by the DRAM and L2 cache interface.
Disabled	All read and write cycles to this area are ignored by the DRAM and cache interface. These cycles are forwarded to PCI for termination.

Each PAM Register controls two regions, typically 16 Kbytes in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 6.

PCI master access to DRAM space is also controlled by the PAM Registers. If the PAM programming indicates a region is writeable, then PCI master writes will be accepted (DEVSEL# generated). If the PAM programming indicates a region is readable, PCI master reads will be accepted. If a PCI write to a non-writeable DRAM region, or a PCI read to a non-readable DRAM region is seen, the MTXC will not accept the cycle (DEVSEL# will not be asserted). PCI master accesses to enable memory hole regions will not be accepted.

Table 6. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Cache Enable	Bits [5, 1] Write Enable	Bits [4, 0] Read Enable	Description
x	x	0	0	DRAM disabled, accesses directed to PCI
x	0	0	1	read only, DRAM write protected, non-cacheable
x	1	0	1	read only, DRAM write protected, L1 cacheable for code accesses only
x	0	1	0	write only
x	0	1	1	read/write, non-cacheable
x	1	1	1	read/write, cacheable

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process the BIOS can be shadowed in main memory to increase the system performance. When a BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The CPU then does a write of the same address, which is directed to main

memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 7. PAM Register and Associated Memory Segments

PAM Reg.	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	CE	WE	RE	0F0000h – 0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000h – 0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000h – 0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000h – 0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000h – 0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000h – 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000h – 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000h – 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000h – 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000h – 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000h – 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000h – 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000h – 0EFFFFh	BIOS Extension	5Fh

NOTES:

The CE bit should not be changed while the L2 cache is enabled.

DOS Application Area (00000h–9FFFh)

Read, write, and cacheability attributes are always enabled and are not programmable for the 0–640-Kbytes DOS application region.

Video Buffer Area (A0000h–BFFFFh)

This 128-Kbytes area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable.

Expansion Area (C0000h–DFFFFh)

This 128-Kbytes area is divided into eight 16-Kbytes segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled Memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-Kbytes area is divided into four 16-Kbytes segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64-Kbytes segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

Extended Memory Area (100000h–FFFFFFFFh)

The extended memory area can be split into several parts:

- Flash BIOS area from 4 Gbytes to 4 Gbytes–512 Kbytes (aliased on ISA at 16 Mbytes–15.5 Mbytes)
- DRAM Memory from 1 Mbytes to a maximum of 512 Mbytes
- PCI Memory space from the top of DRAM to 4 Gbytes–512 Kbytes

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 Gbytes to 4 Gbytes–512 Kbytes. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4-Gbytes range, the request is directed to PCI.

The DRAM memory space can occupy extended memory from a minimum of 1 Mbytes up to 256 Mbytes. This memory is cacheable.

PCI memory space from the top of main memory to 4 Gbytes is always non-cacheable.

3.1.22. DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: 60–65h
Default Value: 02h
Access: Read/Write

The MTXC supports 6 rows of DRAM. Each row is 64-bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 4-Mbytes granularity.

DRB0=Total amount of memory in row 0 (in 4 Mbytes)
DRB1=Total amount of memory in row 0 + row 1 (in 4 Mbytes)
DRB2=Total amount of memory in row 0 + row 1 + row 2 (in 4 Mbytes)
DRB3=Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 4 Mbytes)
DRB4=Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in 4 Mbytes)
DRB5=Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (in 4 Mbytes)

The DRAM array can be configured with 512-KB, 1-MB, 4-MB, or 16-MB deep by 32- or 36-bit wide SIMMs. Each register defines an address range that will cause a particular RAS# line to be asserted (e.g., if the first DRAM row is 8 Mbytes, accesses within the 0 to 8-Mbytes range will cause RAS0# to be asserted).

NOTE

When programming the DRB registers, the following programming consideration must be followed: When DRB3 is written, DRB4 and DRB5 are also modified with the value written into DRB3. When DRB4 is written, DRB5 is also modified with the value written into DRB4. To avoid data corruption in the DRB4 and DRB5 registers, program DRB3 first, followed by DRB4 and then DRB5. If either DRB3 or DRB4 are written, this sequence should be followed.

Bit	Description
7	**Reserved.**
6:0	**Row Boundary Address**. This 7-bit value is compared against the address lines A[28:22] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB=row size).

Row Boundary Address

These 8 bit values represent the upper address limits of the 6 rows (i.e., this row minus previous row=row size). Unpopulated rows have a value equal to the previous row (row size=0). DRB5 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB5. If DRB5 is greater than 256 Mbytes, then 256 Mbytes of DRAM are available. BIOS must make sure that the DRB registers do not reflect more than 256M of Main memory.

As an example of a general purpose configuration where 3 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured like the one shown in Figure 3. In this configuration, the MTXC drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.

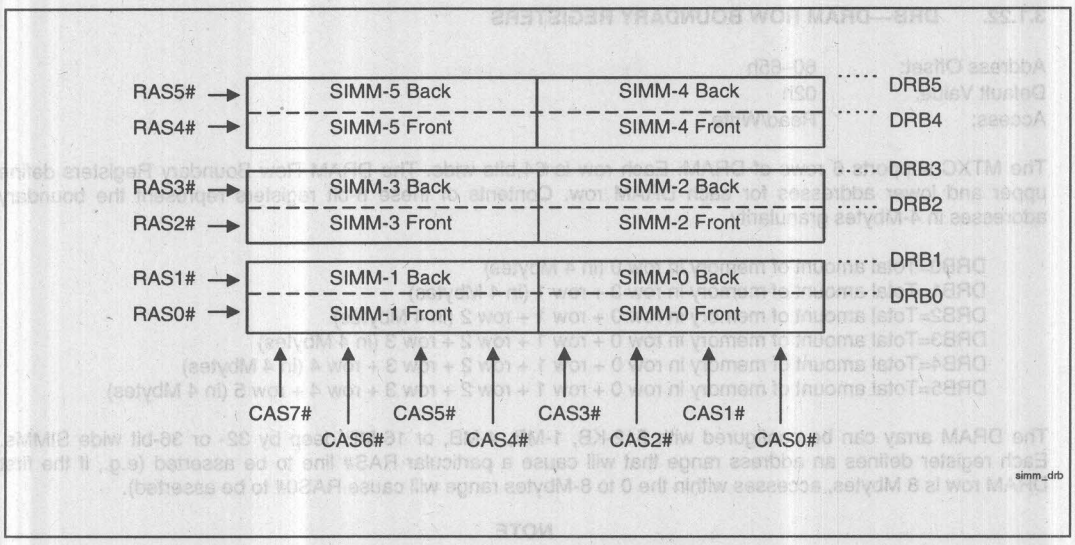


Figure 3. SIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of four 8-byte or eight 4-byte SIMM sockets.

Example #1

The memory array is populated with four single-sided 1 MB x 32 SIMMs, a total of 16 MBytes of DRAM. Two SIMMs are required for each populated row making each populated row 8 Mbytes in size.

DRB0=02h	populated (2 SIMMs, 8 Mbytes this row)
DRB1=04h	populated (2 SIMMs, 8 Mbytes this row)
DRB2=04h	empty row
DRB3=04h	empty row
DRB4=04h	empty row
DRB5=04h	empty row

Example #2

As an another example, the memory array is populated with two 2 Mbytes x 32 double-sided SIMMs (one row), and four 4 Mbytes x 32 single-sided SIMMs (two rows), yielding a total of 96 Mbytes of DRAM. The DRB Registers are programmed as follows:

DRB0=04h	populated with 16 Mbytes, 1/2 of double-sided SIMMs
DRB1=08h	the other 16 Mbytes of the double-sided SIMMs
DRB2=10h	populated with 32 Mbytes, one of the sided SIMMs
DRB3=18h	the other 32 Mbytes of single-sided SIMMs
DRB4=18h	empty row
DRB5=18h	empty row

3.1.23. DRTH—DRAM ROW TYPE REGISTER HIGH

Address Offset: 67h
Default Value: S0000000
Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO, SPM (standard page mode)), or SDRAM (synchronous DRAM) used in rows 4 and 5 and should be programmed by BIOS for optimum performance if EDO DRAMs or SDRAMs are used. The MTXC uses these bits to determine the correct cycle timing to use before a DRAM cycle is run. Bit 7 of this register is used for Host Frequency Detection (HFD). Bit 2 of this register is used to determine the muxing results of CKE/MAA0 and CKEB/MAA1.

NOTE

This register should not be written while DRAM refresh is enabled.

Bit	Description
7	**Host Frequency Detection (HFD).** 1=66 MHz. 0=60 MHz. This bit is initialized to the inverted level on the A27 signal at the rising edge of the RST#. Since A27 pin contains an internal weak pulldown, unless an external resistor exits, the field is initialized to 1, indicating 66 MHz. Subsequent writes to this field will override the reset strap value. BIOS can use the value to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping).
5:4, 1:0	**DRAM Row Type (DRT).** The DRT bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB register. **DRT Bits — DRAM Row** 5,1 — 5 4,0 — 4 **DRT — DRAM Type value definitions** 0,0 — SPM DRAM 0,1 — EDO DRAM 1,0 — SDRAM 1,1 — Reserved
6,3	**Reserved.**
2	**Memory Address Select Enable (MASELEN).** When this bit is set to 1, CKE and CKEB are used to propagate the second copy of the MA0 and MA1 lines. CKE is muxed with MAA0 and CKEB is muxed with MAA1. When this bit is set to 0, the CKE and CKEB functionality is propagated across these lines. This bit defaults to 0 and BIOS must set it to 1 to take advantage of the second copy of the MA0 and MA1 lines.

3.1.24. DRTL—DRAM ROW TYPE REGISTER LOW

Address Offset: 68h
Default Value: 00h
Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO, SPM (standard page mode)), or SDRAM (synchronous DRAM) used in rows 0 to 3 and should be programmed by BIOS for optimum performance if EDO DRAM's or SDRAMs are used. The hardware uses these bits to determine the correct cycle timing to use before a DRAM cycle is run.

Bit	Description
7:0	**DRAM Row Type (DRT).** The DRT bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB register. **DRT Bits — DRAM Row** 7,3 — 3 6,2 — 2 5,1 — 1 4,0 — 0 **DRT — DRAM Type value definitions** 0,0 — SPM DRAM 0,1 — EDO DRAM 1,0 — SDRAM 1,1 — reserved

3.1.25. MTT—MULTI-TRANSACTION TIMER REGISTER (RESERVED TEST MODE REGISTER)

Address Offset: 70h
Default Value: 20h
Access: Read/Write

MTT is an 8-bit register that controls the amount of time that the MTXC's arbiter allows a PCI initiator to perform multiple transactions on the PCI bus. The MTT guarantees the minimum time, measured in PCLKs, that the PCI agent retains the ownership of the PCI bus from the initial assertion of grant.

Bit	Description
7:2	**MTT Count value.** The number of clocks programmed in the MTT represents the guaranteed time slice (in PCLKs) allotted to the current agent, after which the MTXC will grant the bus as soon as another PCI agent requests the bus. The value of 00h disables this function. The count value should be set to multiples of 4 (i.e., 2 lsbs are ignored).
1:0	**Reserved.** Hardwired to 0. (i.e., counter has a resolution of 4 PCLKs)

3.1.26. ESMRAMC—EXTENDED SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 71h
Default Value: 00h
Access: Read/Write

The Extended SMRAM register controls the configuration of Extended SMRAM space. MTXC supports two types of SMRAM memory: Compatible and Extended. The Compatible SMRAM (C_SMRAM) memory provides an uncacheable SMRAM memory space below 1 Mbytes in the A and B segments. The Extended SMRAM (E_SMRAM) memory provides a writeback cacheable SMRAM memory space that is above 1 Mbytes. This register provides the following types of control over SMRAM space:

- Where the memory space is located (above 1 Mbytes, below 1 Mbytes)
- Enabling of SMRAM memory (TSEG, 128 Kbytes, 256 Kbytes, 512 Kbytes or 1 Mbytes of additional SMRAM memory) for Extended SMRAM space only.
- Cacheability control (for the Extended SMRAM space only)
- Protection of SMRAM space for non-SMM accesses

Bit	Description
7	**High SMRAM Enable (H_SMRAME).** 1=Enable. 0=Disable. This bit enables the high SMRAM memory space to appear in the appropriate physical address locations between 100A0000h and 100F0000h.
6	**Extended SMRAM Error (E_SMERR).** This bit is set when CPU accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit=0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	**SMRAM Cache Strategy (SM_CACHE).** Hardwired to 0. This bit determines how Extended SMRAM space is cached (writethru or writeback). Since the MTXC supports only writeback for extended SMRAM space, this bit is hardwired to 0.
4	**SMRAM_L1_EN (SM_L1).** This bit should be set to 1 if Extended SMRAM is being used and the system wishes to L1 writeback cache this memory space. Default value for this bit is 0.
3	**SMRAM_L2_EN (SM_L2).** This bit should be set to 1 if Extended SMRAM is being used, and there is less than 32 Mbytes of DRAM in the system. Setting of this bit when SM_L1 bit=1 allows the Extended SMRAM to be writeback cached in the L2. Default value for this bit is 0.
2:1	**TSEG_SZ[1-0] (T_SZ).** Selects the size of the TSEG memory block, if enabled. This memory is taken from the top of DRAM space, which is no longer claimed by the memory controller (all accesses to this space are sent to the PCI bus if TSEG_EN is set). This memory appears at the physical memory space of 256 Mbytes plus the top of memory (TOM) minus the size of TSEG. This field decodes as follows: **Bits[1,0] Description** 00 (TOM-128 KB) to TOM 01 (TOM-256 KB) to TOM 10 (TOM-512 KB) to TOM 11 (TOM-1 MB) to TOM
0	**TSEG_EN (T_EN).** When G_SMRAME=1 and T_EN=1, the TSEG is enabled to appear in the appropriate physical address space.

3.1.27. SMRAMC—SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 72h
Default Value: 02h
Access: Read/Write

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. MTXC supports two types of SMRAM memory: Compatible and Extended. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit be reset before the LOCK bit is set.

Bit	Description
7	**Reserved.**
6	**SMM Space Open (D_OPEN).** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMIACT# is negated. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 is mutually exclusive with D_CLS=1. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	**SMM Space Closed (D_CLS).** When D_CLS=1, SMM space DRAM is not accessible to data references, even if SMIACT# is asserted. Code references may still access SMM space DRAM. This will allow SMM software to reference "through" SMM space to update the display, even when SMM space is mapped over the VGA range. Software should ensure that D_OPEN=1 is mutually exclusive with D_CLS=1.
4	**SMM Space Locked (D_LCK).** When D_LCK is set to 1, D_OPEN is reset to 0 and both D_LCK and D_OPEN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRAME).** If set to a 1, then Compatible SMRAM functions is enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMIACT#). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG).** This field programs the location of SMM space. SMM DRAM is not remapped. It is simply "made visible" if the conditions are right to access SMM space; otherwise, the access is forwarded to PCI. C_BASE_SEG=010 selects the SMM space as A0000–BFFFFh. All other values are reserved. PCI initiators are not allowed to access to SMM space. These bits are hardwired to 010.

Table 8 summarizes the operation of SMRAM space cycles targeting the SMI space addresses.

Table 8. SMRAM Space Cycles

G_SMRAME	D_LCK	D_CLS	D_OPEN	SMIACT#	H_SMRAME	TSEG_EN	Code Fetch			Data Access		
0	x	x	x	x	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	0	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	0	0	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	0	0	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	0	0	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	0	x	0	1	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	0	1	x	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	0	0	1	x	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	0	0	1	x	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	0	0	1	x	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	0	1	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	1	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→PCI	S→PCI	T→PCI
1	0	1	0	0	1	0	A→DRAM	S→DRAM	T→PCI	A→PCI	S→PCI	T→PCI
1	0	1	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→PCI	T→PCI
1	0	1	1	x	x	x	Invalid			Invalid		
1	1	0	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	1	0	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	1	0	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	1	0	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	1	x	0	1	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→PCI	S→PCI	T→PCI
1	1	1	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→PCI	T→PCI

NOTES:

1. A=A Segment, S=100A0000h to 100FFFFFh, and T=T Segment. The Code Fetch and Data Access columns indicate whether the access is to the PCI bus or to main memory DRAM.

3.1.28. MCTL—MISCELLANEOUS CONTROL REGISTER

Address Offset: 79h
Default Value: 00h
Access: Read/Write

Bit	Description
7	**Reserved.**
6	**ACPI Control Register Enable (ACRE).** 0=Any CPU access to I/O address 0022h is passed on to the PCI bus. 1=Any CPU access to I/O address 0022h is processed internally in the MTXC. This bit must be set to 1 before accessing the "Arbiter Disable" bit in the PM2_CNTRL Register (0022h).
5	**Suspend Refresh Type (SRT).** 0=CBR refresh. 1=Self refresh. This bit determines what type of DRAM refresh is used during Power On Suspend (POS) or Suspend to DRAM modes. This bit applies to EDO/FPM DRAM only. SDRAM always uses self refresh, regardless of the state of this bit.
4	**Normal Refresh Enable (NREF_EN).** Setting this bit to 1 switches MTXC from suspend refresh to normal refresh. After the reset, this bit must be set by software executing out of EPROM. MTXC waits for this bit to be set before exiting out of suspend refresh mode.
3	**Reserved.**
2	**Internal Clock Control (Gated Clock) Disable (Icc).** 1=Disable. 0=Enable. This bit, when set to 0, allows the MTXC to reduce its power consumption (via turning off its internal clocks, to specific interfaces) when in chip standby mode. This bit defaults to 0.
1:0	**Reserved.**

4.0. FUNCTIONAL DESCRIPTION

4.1. Host Interface

The Host Interface of the MTXC is designed to support the Pentium microprocessor. The host interface of the MTXC supports 60-, and 66-MHz bus speeds. The Intel 430TX PCIset supports the Pentium microprocessor with a full 64-bit data bus, 32-bit address bus, and associated internal writeback cache logic. Host bus addresses are decoded by the MTXC for accesses to main memory, PCI memory, and PCI I/O. The MTXC also supports the pipelined addressing capability of the Pentium microprocessor.

4.2. Secondary Cache Interface

The MTXC integrates a high performance writeback second level cache controller using internal/external tags and provides a full first level and second level cache coherency mechanism. The second level cache is direct mapped, nonsectored, and supports a writeback, no write allocate (lines are not allocated on write misses) write policy.

The second level cache can be configured to support either a 256-KB or 512-KB cache using synchronous pipelined burst SRAM or DRAM Cache. One additional PCIset signal (KRQAK) is required to support DRAM Cache. 64-Mbytes cacheability coverage is obtained with 8Kx8 standard SRAM to store the tags for 256-KB configuration. For the 512-KB configurations, a 16Kx8 standard SRAM is used to store the tags and the valid bits for 64-MB cacheability.

A second level cache line is 32-bytes wide. In the 256-KB configurations, the second level cache contains 8K lines, while the 512-KB configurations contain 16K lines. Valid and modified status bits are kept on a per line basis. Cacheability of the entire memory space in first level cache is supported, while only the lower 64 MB of main memory is cacheable in the second level cache. Table 9 shows the tag sizes needed to support different sizes of cacheability. Only main memory controlled by the MTXC DRAM interface is cached. PCI memory is not cached.

Table 9. Cacheability

Cache Size	Tag Size	Cacheability
256 Kbytes	8K by 8 bits	64 Mbytes
512 Kbytes	16K by 8 bits (including valid bit)	64 Mbytes

The following table shows the different standard SRAM access time requirements for different host clock frequencies.

Table 10. SRAM Access Time Requirements

Host Clock Frequency (MHz)	Pipelined Burst Clock-to-Output Access Time (ns)	Tag RAM Cycle Time (ns)
60	10	15
66	8.5	15

Figure 4 and Figure 5 show the connections between the MTXC and the external tag RAM and data SRAM.

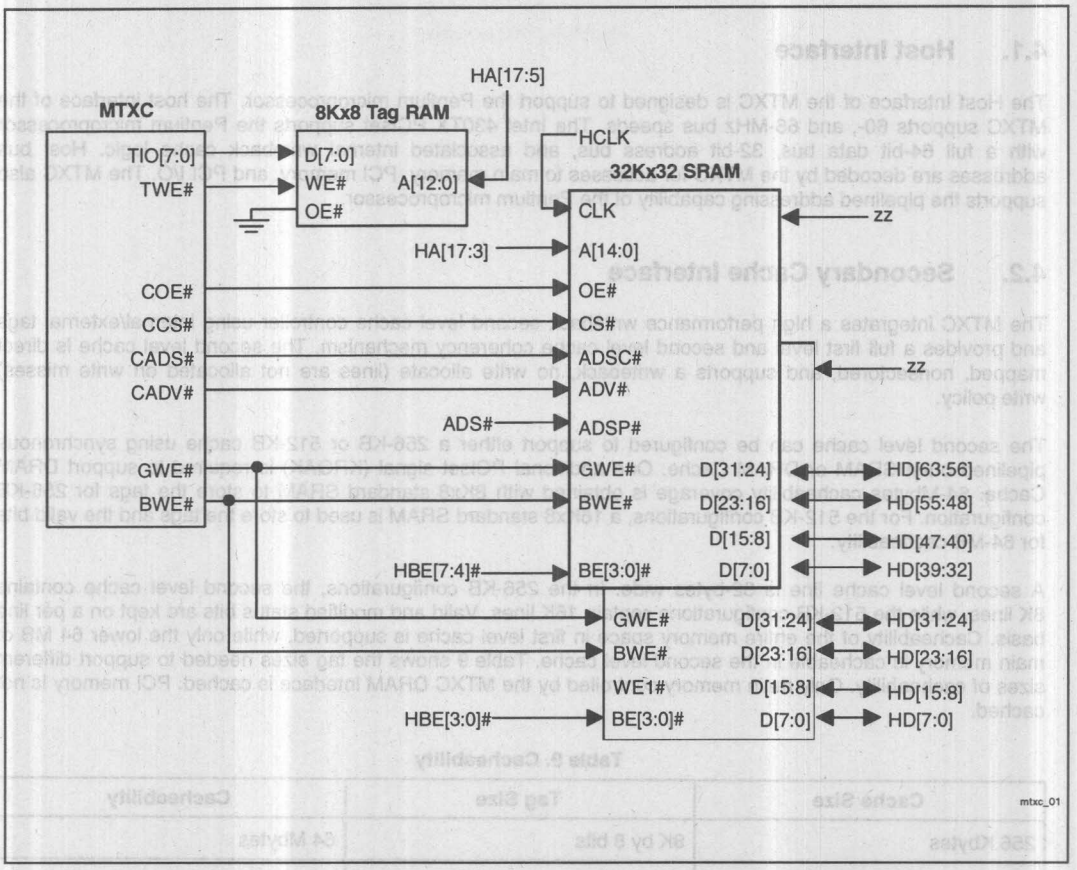


Figure 4. MTXC Connections for 256K Second Level Cache with PBSRAM

Figure 5 shows a 512-KB implementation using four 32Kx32 SRAM. Two 64Kx32 devices could also be used. In this case, HA18 would not be connected to CS2# (i.e., CS2 and CS2# should be connected to an active state). HA18 should be connected to one of the address lines on the 64Kx32 SRAM and is still required for the TAG RAM.

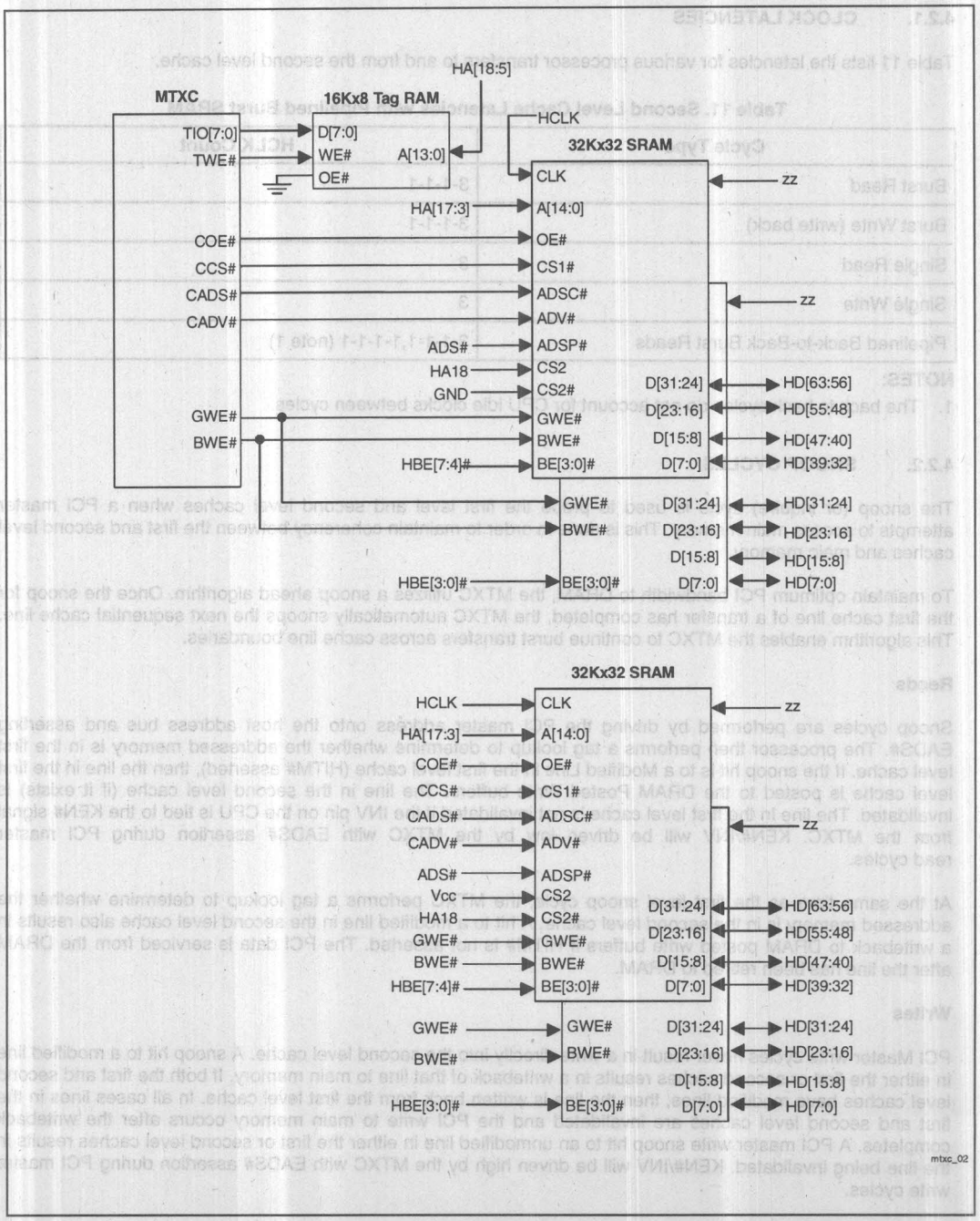


Figure 5. MTXC Connections for 512K Second Level Cache with PBSRAM

4.2.1. CLOCK LATENCIES

Table 11 lists the latencies for various processor transfers to and from the second level cache.

Table 11. Second Level Cache Latencies with Pipelined Burst SRAM

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write (write back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1,1-1-1-1 (note 1)

NOTES:
1. The back to back cycles do not account for CPU idle clocks between cycles.

4.2.2. SNOOP CYCLES

The snoop (or inquire) cycle is used to probe the first level and second level caches when a PCI master attempts to access main memory. This is done in order to maintain coherency between the first and second level caches and main memory.

To maintain optimum PCI bandwidth to DRAM, the MTXC utilizes a snoop ahead algorithm. Once the snoop for the first cache line of a transfer has completed, the MTXC automatically snoops the next sequential cache line. This algorithm enables the MTXC to continue burst transfers across cache line boundaries.

Reads

Snoop cycles are performed by driving the PCI master address onto the host address bus and asserting EADS#. The processor then performs a tag lookup to determine whether the addressed memory is in the first level cache. If the snoop hit is to a Modified Line in the first level cache (HITM# asserted), then the line in the first level cache is posted to the DRAM Posted Write buffers. The line in the second level cache (if it exists) is invalidated. The line in the first level cache is not invalidated if the INV pin on the CPU is tied to the KEN# signal from the MTXC. KEN#/INV will be driven low by the MTXC with EADS# assertion during PCI master read cycles.

At the same time as the first level snoop cycle, the MTXC performs a tag lookup to determine whether the addressed memory is in the second level cache. A hit to a modified line in the second level cache also results in a writeback to DRAM posted write buffers if HITM# is not asserted. The PCI data is serviced from the DRAM after the line has been retired to DRAM.

Writes

PCI Master write cycles never result in a write directly into the second level cache. A snoop hit to a modified line in either the first or second caches results in a writeback of that line to main memory. If both the first and second level caches have modified lines, then the line is written back from the first level cache. In all cases lines in the first and second level caches are invalidated and the PCI write to main memory occurs after the writeback completes. A PCI master write snoop hit to an unmodified line in either the first or second level caches results in the line being invalidated. KEN#/INV will be driven high by the MTXC with EADS# assertion during PCI master write cycles.

4.2.3. DRAM CACHE SECOND LEVEL CACHE MODE

DRAM Cache L2 cache implementation is similar to Pipelined Burst SRAM, except for the addition of the KRQAK bi-direct refresh handshake signal between the MTXC and L2 SRAM. A DRAM Cache type L2 is assumed present when the KRQAK pin is sampled high during the negation of the reset signal. An internal weak pull-down is used on the MTXC KRQAK pin to default to a non DRAM Cache L2 mode, if this pin is left unconnected. An external pull-up (10 kΩ) must be used on KRQAK when DRAM Cache SRAM is used. Note that there is no configuration bit associated with the L2 Pseudo SRAM mode.

The SRAM can operate in either master or slave mode via the M/S# strapping bit. In master mode, the SRAM drives the KRQAK pin to request a refresh. A slave device never drives KRQAK, but only monitors it to determine when a refresh period begins. Only one SRAM device within the L2 cache is master enabled. The other SRAM devices must be slaves.

During reset, the master SRAM and MTXC tri-state their KRQAK outputs. After the SRAM RESET pin is negated, KRQAK remains tri-stated for one whole refresh interval and is then driven high by the master SRAM. The SRAM signals a refresh request by driving KRQAK low for 1 clock, high the next clock, and then tri-states on the following clock and waits, sampling the KRQAK pin. The MTXC after sampling the SRAM's request on KRQAK and after the SRAM has tri-stated its KRQAK output, waits for a host bus dead clock and grants an L2 refresh by driving its KRQAK pin in an identical fashion to the SRAM's request signaling. When all SRAM's see the refresh grant from the MTXC, they begin their internal refresh cycle for a period of 20 clocks.

4.3. DRAM Interface

The MTXC integrates a DRAM controller that supports a 64-bit memory array from 4 Mbytes to 256 Mbytes of main memory. The MTXC supports Standard Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memories using 32-bit wide SIMM modules, 64-bit wide unbuffered DIMM modules and 64-bit wide unbuffered SO-DIMM modules. DRAM parity is not supported, and for loading reasons, parity modules should not be used. All three memory types can be mixed and matched. The MTXC generates all DRAM control signals and multiplexed addresses for the DRAM array. The address and data flows through the MTXC for all DRAM accesses. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the MTXC configuration register description. A brief overview of these registers is provided in this section.

The MTXC supports page mode DRAMs and EDO (Extended Data Out) DRAMs; otherwise known as Hyper Page mode. The twelve multiplexed address lines, MA[11:0], allow the MTXC to support 4-Mbit, 16-Mbit, and 64-Mbit memory, both symmetrical and asymmetrical addressing. The MTXC has six RAS# lines enabling the support of up to six rows of DRAM. Eight CAS# lines allow byte control over the array during write operations. The MTXC targets 60 ns (also supports 50 ns and 70 ns) DRAMs, and supports both single- and double-sided Dram modules. The MTXC provides CBR refresh and extended CBR refresh in the normal mode and self refresh or CBR (for EDOs only) during suspend mode.

The MTXC also supports SDRAMs. The fourteen multiplexed address lines, MA[13:0], allow the MTXC to support 16-Mbit and 64-Mbit SDRAM devices. The MTXC has six CS# lines (i.e. muxed onto RAS#[5:0]). Although six CS# signals are provided, due to loading concerns, 5 rows of SDRAM maximum is recommended. Eight DQM lines (i.e., muxed with CAS#[7:0]) allow byte control over the array during the write operation. Two copies of SRAS# and SCAS# signals are provided for encoded SDRAM commands. The MTXC targets 60- and 66-MHz SDRAMs and supports both single- and double-sided SDRAM modules.

The DRAM interface of the MTXC is configured by the DRAM Control Mode Register (DRAMC), DRAM Extended Control Register (DRAMEC), DRAM Timing Register (DRAMT), SDRAM Control Register (SDRAMC), six DRAM Row Boundary (DRB) Registers, and the DRAM Row Type (DRT) Registers. The DRB registers define the size of each row in the memory array.

similar manner.

4.3.1. DRAM ORGANIZATION

The MTXC integrates a DRAM controller that supports EDO, FPM, and SDRAM. SDRAM, EDO and FPM DRAM's can be mixed between rows, however, a given row must contain only one type of DRAM. When DRAM types are mixed (EDO, FPM and SDRAM) each row will run optimized for that particular type of DRAM.

The MTXC supports six rows of memory (six RAS#/CS# lines). For maximum memory flexibility and performance, it is recommended that a DRAM configuration of four rows be used. This allows 64-Mbit DRAM devices to be used as well as the mixing of SDRAM and EDO/FPM. Figure 6 shows an EDO/FPM configuration using x32 SIMM modules and Figure 7 shows a four row EDO/FPM/SDRAM configuration using x64 DIMM modules (or x64 SO-DIMM).

NOTE

It is not recommended to mix SDRAM (which are 3V devices) with 5V EDO/FPM SIMMs, unless the SDRAM and EDO/FPM are properly isolated (e.g., isolate the memory data lines with Qswitches). Mixing 5V and 3V memory is not recommend for reliability reasons. Not all SDRAMs are 5V tolerant.

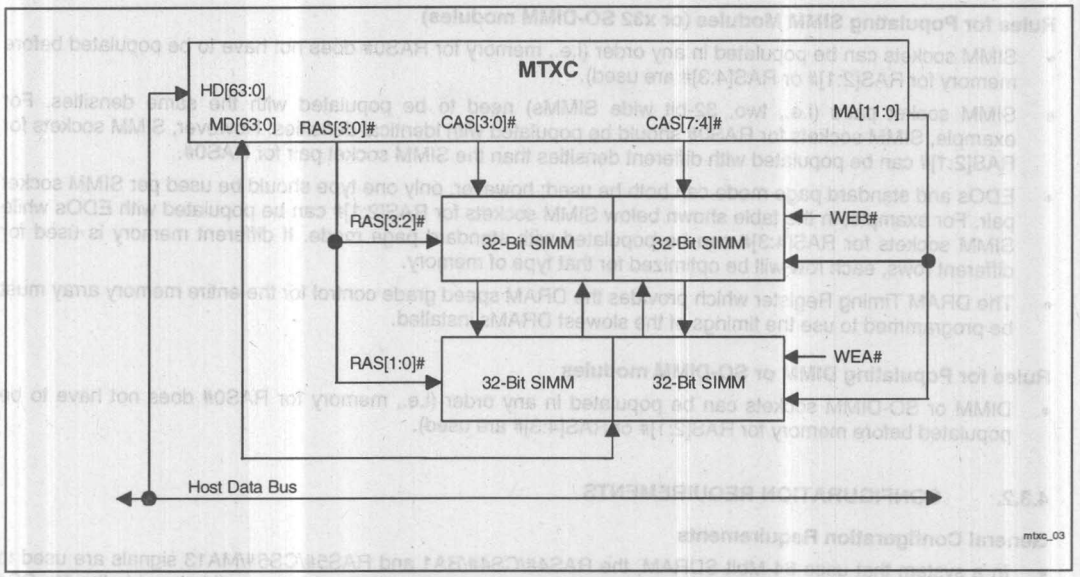
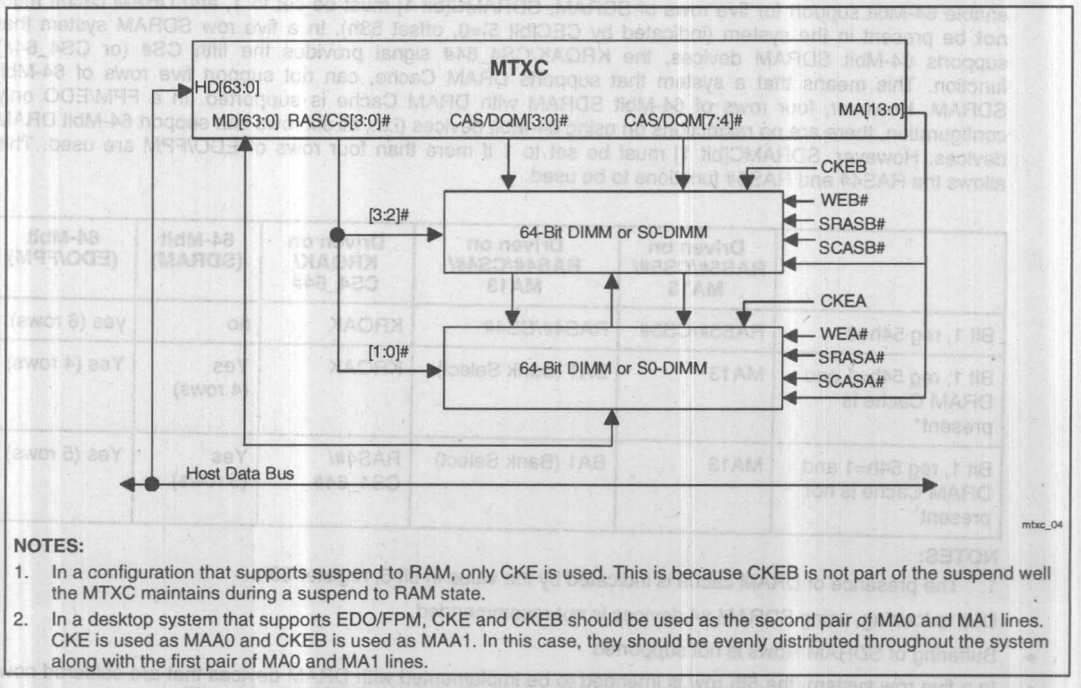


Figure 6. FPM/EDO Four Row SIMM Configuration



NOTES:

1. In a configuration that supports suspend to RAM, only CKE is used. This is because CKEB is not part of the suspend well the MTXC maintains during a suspend to RAM state.
2. In a desktop system that supports EDO/FPM, CKE and CKEB should be used as the second pair of MA0 and MA1 lines. CKE is used as MAA0 and CKEB is used as MAA1. In this case, they should be evenly distributed throughout the system along with the first pair of MA0 and MA1 lines.

Figure 7. FPM/EDO/SDRAM Four Row DIMM or SO-DIMM Configuration

Rules for Populating SIMM Modules (or x32 SO-DIMM modules)

- SIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).
- SIMM socket pairs (i.e., two, 32-bit wide SIMMs) need to be populated with the same densities. For example, SIMM sockets for RAS0# should be populated with identical densities. However, SIMM sockets for RAS[2:1]# can be populated with different densities than the SIMM socket pair for RAS0#.
- EDOs and standard page mode can both be used; however, only one type should be used per SIMM socket pair. For example, in the table shown below SIMM sockets for RAS[2:1]# can be populated with EDOs while SIMM sockets for RAS[4:3]# can be populated with standard page mode. If different memory is used for different rows, each row will be optimized for that type of memory.
- The DRAM Timing Register which provides the DRAM speed grade control for the entire memory array must be programmed to use the timings of the slowest DRAMs installed.

Rules for Populating DIMM or SO-DIMM modules

- DIMM or SO-DIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).

4.3.2. CONFIGURATION REQUIREMENTS

General Configuration Requirements

- In a system that uses 64-Mbit SDRAM, the RAS4#/CS4#/BA1 and RAS5#/CS5#/MA13 signals are used to provide two additional address lines (BA1 and MA13), and KRQAK/CS4_64# is used to provide the 5th CS# line, if required. To enable 64-Mbit support for four rows of SDRAM, set SDRAMC[bit 1] to 1 (offset 54h). To enable 64-Mbit support for five rows of SDRAM, SDRAMC[bit 1] must be set to 1, and DRAM cache must **not** be present in the system (indicated by CEC[bit 5]=0, offset 53h). In a five row SDRAM system that supports 64-Mbit SDRAM devices, the KRQAK/CS4_64# signal provides the fifth CS# (or CS4_64#) function. This means that a system that supports DRAM Cache, can not support five rows of 64-Mbit SDRAM. However, four rows of 64-Mbit SDRAM with DRAM Cache is supported. In a FPM/EDO only configuration, there are no restrictions on using 64-Mbit devices (i.e., all six rows can support 64-Mbit DRAM devices. However, SDRAMC[bit 1] must be set to 1 if more than four rows of EDO/FPM are used. This allows the RAS4# and RAS5# functions to be used.

	Driven on RAS5#/CS5#/ MA13	Driven on RAS4#/CS4#/ MA13	Driven on KRQAK/ CS4_64#	64-Mbit (SDRAM)	64-Mbit (EDO/FPM)
Bit 1, reg 54h=0	RAS5#/CS5#	RAS4#/CS4#	KRQAK	no	yes (6 rows)
Bit 1, reg 54h=1 and DRAM Cache is present*	MA13	BA1 (Bank Select)	KRQAK	Yes (4 rows)	Yes (4 rows)
Bit 1, reg 54h=1 and DRAM Cache is not present[1]	MA13	BA1 (Bank Select)	RAS4#/ CS4_64#	Yes (5 rows)	Yes (5 rows)

NOTES:

1. The presence of DRAM cache is indicated by the value in bit 5, register 53h.

- Due to loading, using SDRAM x4 devices is not recommended.
- Buffering of SDRAM Rows is not supported
- In a five row system, the 5th row is intended to be implemented with DRAM devices that are soldered down on the motherboard. If a DIMM or a SIMM is used in the 5th row, it should **not** be used as an upgrade path

by the end user; the size and type of DRAM that can be implemented in the 5th row is limited (see the bullets below).

- The total memory supported is 256 MB, even though it is possible to populate the six rows with more than 256 MB. This limit must be ensured by the system BIOS.

EDO/FPM only configuration Requirements

- If more than four rows of x4 DRAM devices + one row of x8 DRAM devices of memory is supported, it is recommended that all six rows be buffered. MA and MWE# enable signals should be buffered. In a system that only supports x8 or x16 devices (i.e., x4 devices not supported), six rows of memory can be supported without buffering.
- Maximum load supported without buffers: Four rows of x4 DRAM devices + one row of x8 DRAM devices.
- A second pair or MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, it is required that the second pair of MA lines be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

SDRAM only configuration Requirements

- Maximum rows supported; Five rows of x8 devices.

SDRAM/EDO/FPM mixing configuration Requirements

- If SDRAM and EDO/FPM are mixed in a system, the configuration is limited to a maximum of four rows (two rows of x4 EDO/FPM and two rows of x8 or x16 SDRAM). If only x8 or x16 EDO/FPM and SDRAM devices are used (i.e., not x4's), five rows can be supported.
- SDRAMs can be mixed with EDO/FPM on a row by row basis (e.g., row 0 can be populated with SDRAMs while row 3 is populated with EDO/FPM).
- A second pair or MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, it is required that the second pair of MA lines be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

Table 12 provides a summary of the characteristics of memory configurations supported by the MTXC. Minimum values listed are obtained with single-sided SIMMs or DIMMs. Maximum values are obtained with double-sided SIMMs or DIMMs. Note that, for a 64-bit wide memory array, a minimum of two 32-bit wide DRAM SIMMs are required in any specific row. The minimum values used are also the smallest upgradeable memory size. Please note that EDO/FPM can also come on x64 DIMM modules.

Table 12. Minimum (Upgradeable) and Maximum Memory Size for each configuration (DRAM)

DRAM Tech.	DRAM Density	DRAM Width	DRAM SIMM		DRAM Addressing	Address Size		DRAM Size	
			SS x32	DS x32		Row	Col	Min. (UP) (1 row)	Max. (6 rows)
4M	512K	8	512K	1M	Asymmetric	10	9	4 MB	24 MB
	1M	4	1M	2M	Symmetric	10	10	8 MB	48 MB
16M	1M	16	1M	2M	Symmetric	10	10	8 MB	48 MB
	1M	16	1M	2M	Asymmetric	12	8	8 MB	48 MB
	2M	8	2M	4M	Asymmetric	11	10	16 MB	96 MB
	4M	4	4M	8M	Symmetric	11	11	32 MB	192 MB
	4M	4	4M	8M	Asymmetric	12	10	32 MB	192 MB
64M	2M	32	2M	4M	Asymmetric	12	9	16 MB	96 MB
	4M	16	4M	8M	Symmetric	11	11	32 MB	192 MB
	4M	16	4M	8M	Asymmetric	12	10	32 MB	192 MB
	8M	8	8M	16M	Asymmetric	12	11	64 MB	256 MB
	16M	4	16M	32M	Symmetric	12	12	128 MB	256 MB

Table 13. Minimum (Upgradeable) and Maximum Memory Size for each configuration (SDRAM)

SDRAM Tech.	SDRAM Density	SDRAM Width	SDRAM DIMM		SDRAM Addressing	Address Size		SDRAM Size	
			SS x64	DS x64		Row	Column	Min. (UP) (1 row)	Max. (6 rows)
16M	1M	16	1M	2M	Asymmetric	12	8	8 MB	48 MB
	2M	8	2M	4M	Asymmetric	12	9	16 MB	96 MB
	4M	4[1]	4M	8M	Asymmetric	12	10	32 MB	192 MB
64M	2M	32	2M	4M	Asymmetric	12	9	16 MB	96 MB
	2M	32	2M	4M	Asymmetric	13	8	16 MB	96 MB
	4M	16	4M	8M	Asymmetric	14	8	32 MB	192 MB
	8M	8	8M	16M	Asymmetric	14	9	64 MB	256 MB
	16M	4[1]	16M	32M	Asymmetric	14	10	128 MB	256 MB

NOTES:

1. Functionally the 430TX supports x4 SDRAM devices. However, due to loading reasons, it is not recommended that x4 devices be used in 60-MHz and 66-MHz designs.

The memory organization shown below represents the maximum 256 MB of address space. Accesses to memory space above Top-of-DRAM (< 256 MB), video buffer, or the memory gaps (if enabled) are forwarded to PCI, and these regions are not cacheable. Below 1 MB, there are several memory segments which have selectable cacheability. None of the DRAM space occupied by the video buffer (except for SMM usage) or the memory space gaps is remapped (and is therefore "lost").

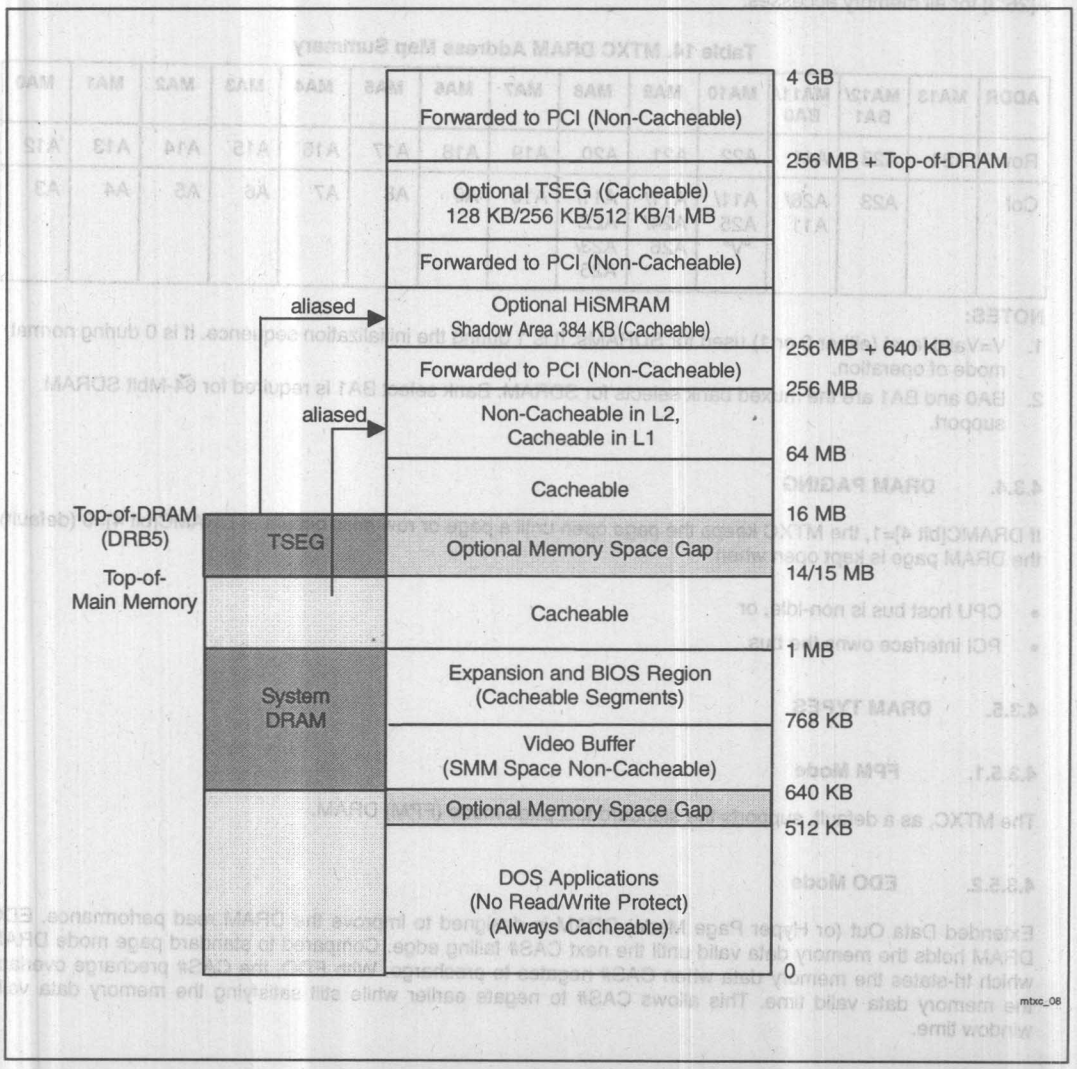


Figure 8. Memory Space Organization

4.3.3. DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by the MA[11:0] signals (MA[13:0] for SDRAM 64-Mbit support). The MA bits are derived from the host or PCI address bus as defined by the Table 14. The MTXC supports a 2K byte page size only. The MA lines are translated from the address lines A[26:3] for all memory accesses.

Table 14. MTXC DRAM Address Map Summary

ADDR	MA13	MA12/ BA1	MA11/ BA0	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	A24	A23	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		A23	A26/ A11	A11/ A25 "V"	A11/ A24/ A26	A11/ A22/ A23/ A25	A10	A9	A8	A7	A6	A5	A4	A3

NOTES:

1. V=Valid level (either 0 or 1) used for SDRAMs. It is 1 during the initialization sequence. It is 0 during normal mode of operation.
2. BA0 and BA1 are the muxed bank selects for SDRAM. Bank select BA1 is required for 64-Mbit SDRAM support.

4.3.4. DRAM PAGING

If DRAMC[bit 4]=1, the MTXC keeps the page open until a page or row miss occurs. If DRAMC[bit 4]=0 (default), the DRAM page is kept open when:

- CPU host bus is non-idle, or
- PCI interface owns the bus.

4.3.5. DRAM TYPES

4.3.5.1. FPM Mode

The MTXC, as a default, supports the standard fast page mode (FPM) DRAM.

4.3.5.2. EDO Mode

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge. Compared to standard page mode DRAM which tri-states the memory data when CAS# negates to precharge. With EDO, the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

4.3.5.3. SDRAM Mode

Synchronous DRAM (SDRAM) implements a fully synchronous interface as compared to a conventional DRAM whose timing delays are related to the rising and falling edges of the RAS#, CAS#, and WE# input signals. The 430TX supports all of the features and timings as shown in the "SDRAM PC" specification. The objective of the *SDRAM* PC Specification is to enable low cost and easily manufactureable SDRAMs for the main stream volume

desktop and Mobile PC's. There are three grade parts defined for the 430TX. All of the speed grade conform to the *SDRAM PC Specification*. For information on the performance of each of the Speed grade parts, refer to the DRAM performance section. The Three speed grade parts are shown in Table 15.

Table 15. SDRAM Speed Grade Parts

Speed Grade	CAS latency (CL)	RAS to CAS (Trcd)	System Frequency
66.67 MHz	3	3	60/66 MHz
66.67 MHz	3	2	60/66 MHz
66.67 MHz	2	2	60/66 MHz

SDRAM Command Reference

The 430TX supports the following commands:

Command
Mode Register Set (MRS)
Activate Bank (ACT)
Read Bank (RD)
Write Bank (WR)
Precharge All Banks (PALL)
Deselect Device

Command
No Operation (NOP)
Auto Refresh CBR (REFR)
Data Write/Output Enable
Data Mask/Output Disable
Self Refresh Entry
Self Refresh Exit

Table 16 MRS command (Mode Register Set) Supported by the MTXC.

Table 16. Command Fields

A11	A10	A9	A8	A7	A[6:4]	A3	A[2:0]
0	0	0	0	0	CL	WT	BL

CAS Latency Field (CL)	
Bits[6:4]	CAS Latency
010	2
011	3
All Other	X

Wrap Type Field (WT)	
Bit 3	Type
0	X
1	Interleave

The linear order addressing is not supported.

Burst Length Field (BL)	
Bits[2:0]	Burst Length
010	4
All Other	X

NOTES:

1. X=Don't Care. These Modes are Don't Care for MTXC specific implementation.

4.3.6. AUTO DETECTION

The SDRAM, FPM, and EDO detection is performed by BIOS. Note that when accessing any of the DRAM related registers (i.e., 54h–68h), refresh should be turned off via the DRAM Control register (DRAMC).

4.3.7. DRAM PERFORMANCE

The DRAM performance is controlled by the DRAM timing register, processor pipelining, and by the type of DRAM used (EDO or FPM or SDRAM). Table 17 depicts both EDO and standard page mode optimum timings. For read cycles, clocks counts are measured from ADS# to BRDY#.

For write cycles, the measurement is broken up into two parts. The first part consists of the rate of posting data in to the CPU to DRAM posted write buffers. This is measured from ADS# to BRDY#. The second part consists of the retire rate from posted write buffers to the DRAM. The leadoff for retiring is measured from the clock after BRDY# assertion to the CAS# assertion.

Table 17 lists the performance summary for 60 ns EDO/FPM DRAMs. The four row column is assuming each row is populated with a maximum of 16, x4 devices=64 DRAM devices. The five row column is assuming each of the first four rows is populated with a maximum of 16, x4 devices and the fifth row is populated with a maximum of eight, x8 devices=72 DRAM devices. The six row column assumes that each of the six rows can be populated with a maximum of 16, x4 devices.

The FELO and SLD bits are used to control the leadoff for read cycles (page hit, row miss, and page miss). Each bit removes one clock from the leadoff, when enabled. Note that FELO impacts EDO only and must be disabled for FPM. The DLT bits are used to control the base starting point for the leadoff for read/write cycles (page miss and row miss, only).

Table 17. EDO/ Standard Page Mode Performance Summary (60 ns DRAMs)

Processor Cycle Type (pipelined)	60/66 MHz w/ four rows	60/66 MHz w/ five rows	60/66 MHz w/ six rows Buffered	DRAM Type
Burst Read Page Hit	5-2-2-2	6-3-3-3	6-3-3-3	EDO
Read Row Miss[1]	8-2-2-2	9-3-3-3	10-3-3-3	EDO
Read Page Miss	11-2-2-2	12-3-3-3	13-3-3-3	EDO
Back-to-Back Burst Reads Page Hit	5-2-2-2-3-2-2-2	6-3-3-3-4-3-3-3	6-3-3-3-4-3-3-3	EDO
Burst Read Page Hit	6-3-3-3	7-4-4-4	7-4-4-4	FPM
Burst Read Row Miss[1]	9-3-3-3	9-4-4-4	9-4-4-4	FPM
Burst Read Page Miss	12-3-3-3	12-4-4-4	12-4-4-4	FPM
Back-to-Back Burst Read Page Hit	6-3-3-3-3-3-3-3	7-4-4-4-4-4-4-4	7-4-4-4-4-4-4-4	FPM
Write Page Hit[2,3,4]	3	3	3	EDO/FPM
Write Row Miss[2,3,4]	6	6	7	EDO/FPM
Write Page Miss[2,3,4]	9	9	10	EDO/FPM
Posted Write[3,4]	3-1-1-1	3-1-1-1	3-1-1-1	EDO/FPM
Write retire rate from Posted Write Buffer	-2-2-2	-3-3-3	-3-3-3	EDO/FPM
Single writes	2	2	3	EDO/FPM
Reg 56h, Bit 4 (SLD)[5]	0	0	0	EDO/FPM
Reg 56h, Bit 5 (FELO)[6]	1	1	1	EDO
Reg 56h, Bit 5 (FELO)[6]	0	0	0	FPM
Reg 58h, Bits[6:5] (DRBT)	2	1	1	EDO/FPM
Reg 58h, Bits[4:3] (DWBT)	2	1	1	EDO/FPM
Reg 58h, Bits[1:0] (DLT)	1	1	0	EDO/FPM
Reg 56h, Bit 6 (RRA)	0	0	0	EDO/FPM

NOTES:

1. The row miss cycles assume that the new page is closed from the prior cycle. Due to the MA[13:0] to RAS# setup requirements, if the page is open, 2 clocks are added to the leadoff.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write timing is measured from the clock after BRDY# is returned to the CPU up to CAS# assertion for that cycle.
4. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
5. This bit (SLD) should be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
6. When set to 1, enables fast timing for EDO timing only. Enables one HCLK pull in for page hit, page miss, and row miss cycles.

Table 18 lists the performance summary for SDRAM. The CL= 3 column represents a CAS latency of 3 part with a RAS to CAS (Trcd) of two clocks. The CL=2 column represents a CAS latency of two part. The performance numbers in Table 18 assume each row is populated with a maximum of eight, x8 devices=40 SDRAM devices.

The SLD bit (page hit, row miss, and page miss) is used to control the leadoff for read cycles. This bit removes one clock from the leadoff, when enabled.

Table 18. SDRAM Performance Summary

Processor Cycle Type	60/66 MHz CL=3 Five Rows (Max)	60/66 MHz CL=2 Five Rows (Max)
Burst Read Page Hit	7-1-1-1	6-1-1-1
Read row Miss[1]	9-1-1-16	8-1-1-1
Read Page Miss	12-1-1-16	11-1-1-1
Back-to-Back Burst Reads Page Hit	7-1-1-1 2-1-1-1	6-1-1-1 2-1-1-1
Write Page Hit[2,3]	3	3
Write Row Miss[2,3]	6	5
Write Page Miss[2,3]	9	8
Posted Write[2,3]	3-1-1-1	3-1-1-1
Write retire rate from Posted Write Buffer	-1-1-1	-1-1-1
Reg 54h, Bit 5 (RCO)[5]	1	0
Reg 54h, Bit 4 (CL)	0	1
Reg 54h, Bit 3 (RT)	0	1
Reg 56h, Bit 4 (SLD)[4]	0	0

NOTES:

1. The row miss cycle assumes that the new page is closed from the prior cycle.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
4. This bit (SLD) must be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
5. For a CL=3 part that can not meet a RAS to CAS timing (Trcd) of two HCLKs, RCO can be set to 0. This will add an HCLK to the leadoff cycle for Row miss and Page miss cycles.

4.3.8. DRAM REFRESH

MTXC supports CAS-before-RAS# (CBR) refresh and Self refresh. The refresh rate is controlled via the DRAM Refresh Rate field in the DRAM Control Register (DRAMC). When a refresh request is generated, it is placed in a four entry queue. The DRAM controller services a refresh request when the refresh queue in not empty and the controller has no other requests pending. When the refresh queue is full, refresh becomes the highest priority request and will be serviced next by the controller.

Refresh is only performed on rows that are populated (i.e., "smart refresh"). The controller determines which rows are populated by looking at the DRB registers. Note that Refresh has to be disabled before the refresh rate is changed.

Refer to bit 5 in the MCTL register (offset 79h) for suspend refresh information.

4.4. PCI CLK Control (CLKRUN#)

4.4.1. CLOCKING STATES

There are three main states in the clocking protocol:

- **Clock Running:** The clock is running and the bus is operational.
- **About to Stop:** The central resource has indicated on the CLKRUN# line that the clock is about to stop.
- **Clock Stopped:** The clock is stopped with CLKRUN# being monitored for a restart

4.4.2. OPERATION

The MTXC is a CLKRUN# Master device and behaves according to the rules for a master device. The PIIX4 companion chip controls the clocks in the system and is the CLKRUN# Central Resource. Please refer to the latest "PCI Mobile Design Guide" for more information.

4.5. SMRAM Memory Space

The MTXC supports the use of main memory as System Management RAM (SMRAM), enabling the use of System Management Mode. The MTXC supports two SMRAM options; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM).

4.5.1. COMPATIBLE SMRAM (C_SMRAM)

This is the traditional SMRAM feature supported in Intel PCIsets. When this function is enabled via C_BASE_SEG[2:0]=010 and G_SMRAME=1 of the SMRAMC register, the MTXC reserves 000A0000h through 000BFFFFh (A and B segments) of the main memory for use as Noncacheable SMRAM. CPU accesses to segments A and B while not in SMM (i.e., SMIACT# is negated) are always forwarded to the PCI bus. CPU accesses to segments A and B while in SMM (i.e., SMIACT# is asserted) are forwarded to either DRAM or PCI bus, depending on the value of bits[6:0] of the SMRAMC register. PCI masters cannot access the SMRAM area of the main memory. When a PCI master tries to access the SMRAM space, the MTXC does not respond to the PCI cycle (i.e., DEVSEL# is not asserted).

4.5.2. EXTENDED SMRAM (E_SMRAM)

This feature in the MTXC extends the SMRAM space up to 1 Mbytes and provide writeback cacheability. This feature requires that SMI handlers execute above 1 Mbytes which will require rewriting the existing code to

(memorize - TSEG) to the OS.

The two areas of memory available for SMRAM when Extended SMRAM is enabled are:

Physical Address	DRAM Address	
100A0000h to 100FFFFFh	000A0000h to 000FFFFFh	(High Mem)
10000000h plus TOM minus TSEG_SZ to 10000000h plus TOM	TOM minus TSEG_SZ to TOM	(TSEG)

Extended SMRAM option has the following DRAM memory available to it:

Table 19. Extended SMRAM DRAM memory regions

DRAM Area	Size/Availability
A Segment	64 Kbytes always available if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
B Segment	64 Kbytes always available if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
C Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
D Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
E Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
F Segment	64 Kbytes only available for suspend/resume (as defined by PAM register) if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
TSEG	128K, 256K, 512K or 1M bytes available if enabled (i.e., TSEG_EN=1 and G_SMRAME=1)

As with the Compatible SMRAM solution, MTXC does not claim any bus master access to the Extended SMRAM memory ranges defined above. The CPU can access these memory ranges by one of the following mechanisms:

- The processor generating an access to one of the defined memory ranges while in the SMM (SMIACT# is active). A processor access to any of the defined ranges while not in SMM (SMIACT# is inactive) and with the D_OPN bit reset will be forwarded to PCI bus and a status bit is set in the SMRAMC register.
- The processor generating an access to one of the defined memory ranges while the D_OPN bit is set.
- Any modified write access of the processor is allowed to write into the SMRAM space, regardless of the state of the D_OPN, D_CLS, or SMIACT# signals.

The cacheability of SMRAM space is dependent on how much physical DRAM is available in the system. If the system has less than 32 Mbytes of DRAM, the SMRAM is cached in both the L1 and L2. If the system has more than 32 Mbytes of DRAM, the SMRAM is cached in only the L1.

4.5.3. SMRAM PROGRAMMING CONSIDERATIONS

When using the Extended SMRAM configuration, the SMI handler software must be extremely careful when accessing DRAM memory in the 100A0000h to 100FFFFFh memory range. First, if this area of memory is accessed while the CPU is not in SMM mode and the D_OPN bit is not set, the MTXC will forward the cycle to PCI bus which may cause a fatal system error and system shutdown. Second, only areas within the 100A0000h to 100FFFFFh region that have been selected as SMRAM space should be accessed; otherwise, the L1 and L2 caches will become incoherent, which will cause a future system error. Any memory in normal DRAM space that is not used in OS or application space can be used as SMRAM memory.

4.6. Low Power States

MTXC supports five types of low power states: Chip Standby, Power On Suspend (POS), Suspend to RAM (STR), Suspend to Disk (STD), and dynamic stop clock. The Table 20 summarizes the various MTXC's Low power states.

Table 20. 430TX Low Power State Summary

PM Mode	Description	Exit Latency Target
Chip Standby	When MTXC's CPU and PCI busses are both idle, MTXC enters this state.	No delay
Dynamic Stop Clock	MTXC provides provisions that enable transitioning the CPU in and out of the stop clock state in an active system. This includes the ability to disable the system arbiter and transition the memory controller in and out of the suspend refresh state.	<10 ms
Powered On Suspend (POS)	System PLLs are powered down, only running clock is the RTC clock and the SUSCLK. MTXC maintains DRAM refresh using SUSCLK.	<10 ms
Suspend to RAM (STR)	CPU complex (CPU and L2) and PCI interface are powered off. Only the RTC clock and SUSCLK are running. MTXC maintains DRAM refresh using SUSCLK.	~1 sec
Suspend to Disk(STD)	CPU complex (CPU and L2), DRAM and PCI interface are powered off.	~30 sec

The 430TX system maintains a very low power CPU complex by utilizing the different power down features available from the CPU, cache data RAMs and utilizing leading edge low power design techniques in the 430TX system components. The 430TX components work in unison to dynamically control the CPU complexes power state without adversely affecting performance. The following gives a brief description of how the 430TX system components achieve these low power states.

The MTXC and PIIX4 work in unison to maintain a very low power L2 subsystem without adversely affecting peak performance.

NOTE

There are some system restrictions when DRAM Cache is implemented in a system that supports STP_CLK, POS, and STR power management modes. Since KRQAK is not implemented in the "Suspend Well," the correct operation of KRQAK is not guaranteed when the system enters the above mentioned power management modes. To avoid data corruption in the L2 cache, a system that implements the STP_CLK, POS, and STR modes must abide by the following rules:

1. Before entering these power management modes, the DRAM cache must be flushed so that all modified lines end up in system memory.
2. After exiting these power management modes, the DRAM Cache must be reinitialized.

4.6.1. CHIP STANDBY

The MTXC also supports a chip standby mode. When the MTXC determines that both its CPU interface and PCI interface are idle, it will dynamically place itself into a very low power state. While in chip standby state the MTXC is able to respond to new CPU or PCI bus master accesses with no performance penalty. This provides very optimized power/performance characteristics because the CPU interface are idle for large periods of time. The MTXC enters Chip Standby mode when the following conditions are true:

- Host Bus idle
- PCI bus Idle
- Normal Mode (i.e., not Test Mode)
- Not in RESET state
- Internal operations idle

Entering the Chip Standby state is not dependent on any timer expiration. When the above conditions are met, the MTXC can enter the chip standby state as soon as it can.

4.6.2. SUSPEND/RESUME

The MTXC supports POS, STR, STD and SOFF (Soft Off) suspend states. The MTXC supports the POS mode by maintaining all of its power planes when in the suspend state. The MTXC supports the STR modes by isolating its CPU and PCI interfaces, and only maintaining the DRAM refresh off the SUSCLK signal. When exiting the STR modes, the MTXC's core well is reset and its context is lost (the power management context is not lost however). The MTXC supports the STD and SOFF modes by being totally powered off.

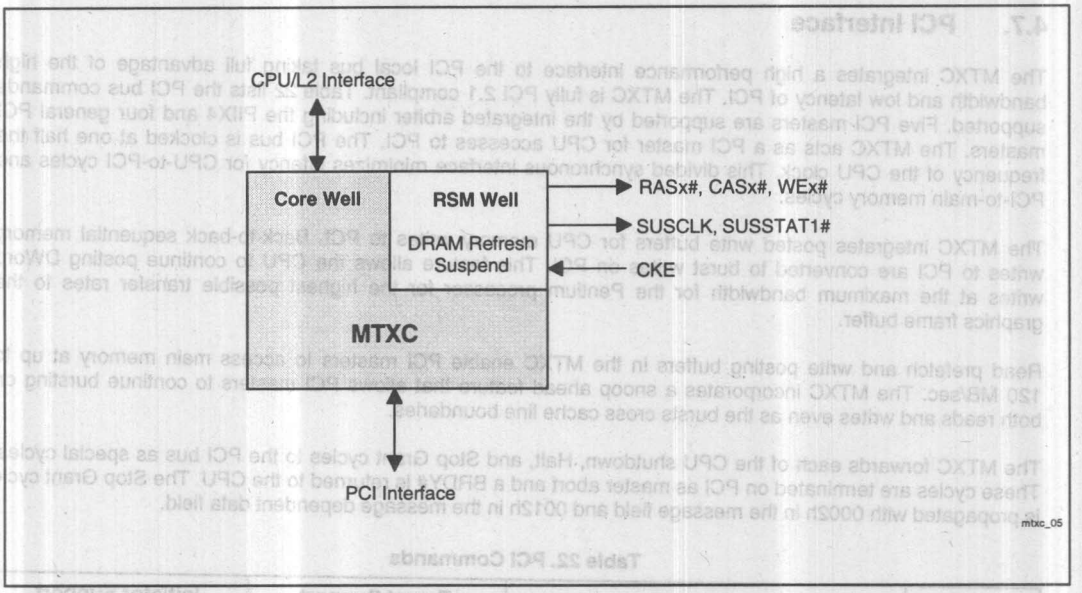


Figure 9. MTXC Power Planes

4.6.2.1. Power Transition Changes

The MTXC supports several suspend modes that support the PIIX4 system suspend states. Table 21 illustrates what suspend mode the MTXC enters upon the appropriate PIIX4 suspend mode.

Table 21. Power Transition States

PIIX4 Suspend State	MTXC Suspend State	MTXC Description
POS	PonS	All interfaces enabled, clocks stopped.
STR	PoffS	CPU, L2, PCI interfaces disabled
STD	Off	Chip is off.
Off/Soft Off	Off	Chip is off.

The core logic should be reset when the PCI bus is reset. This means that the refresh logic and power sequencing logic is not reset during resumes (part of the resume well).

4.7. PCI Interface

The MTXC integrates a high performance interface to the PCI local bus taking full advantage of the high bandwidth and low latency of PCI. The MTXC is fully PCI 2.1 compliant. Table 22 lists the PCI bus commands supported. Five PCI masters are supported by the integrated arbiter including the PIIX4 and four general PCI masters. The MTXC acts as a PCI master for CPU accesses to PCI. The PCI bus is clocked at one half the frequency of the CPU clock. This divided synchronous interface minimizes latency for CPU-to-PCI cycles and PCI-to-main memory cycles.

The MTXC integrates posted write buffers for CPU memory writes to PCI. Back-to-back sequential memory writes to PCI are converted to burst writes on PCI. This feature allows the CPU to continue posting DWord writes at the maximum bandwidth for the Pentium processor for the highest possible transfer rates to the graphics frame buffer.

Read prefetch and write posting buffers in the MTXC enable PCI masters to access main memory at up to 120 MB/sec. The MTXC incorporates a snoop ahead feature that allows PCI masters to continue bursting on both reads and writes even as the bursts cross cache line boundaries.

The MTXC forwards each of the CPU shutdown, Halt, and Stop Grant cycles to the PCI bus as special cycles. These cycles are terminated on PCI as master abort and a BRDY# is returned to the CPU. The Stop Grant cycle is propagated with 0002h in the message field and 0012h in the message dependent data field.

Table 22. PCI Commands

C/BE#	Command	Target Support	Initiator Support
0000	Interrupt Acknowledge	NO	YES
0001	Special cycle	NO	YES
0010	I/O read	YES	YES
0011	I/O write	YES	YES
0100	reserved	NO	NO
0101	reserved	NO	NO
0110	Memory read	YES	YES
0111	Memory write	YES	YES
1000	reserved	NO	NO
1001	reserved	NO	NO
1010	Configuration Read	NO	YES
1011	Configuration Write	NO	YES
1100	Memory Read Multiple	As Memory Read	NO
1101	Dual Address Cycle	NO	NO
1110	Memory Read Line	As Memory Read	NO
1111	Memory Write and Invalidate	As Memory Write	NO

4.8. System Arbitration

The MTXC's PCI Bus Arbiter allows PCI peer-to-peer traffic concurrent with CPU main memory/second level cache cycles. The arbiter supports five PCI masters. REQ[3:0]#/GNT[3:0]# are used by PCI masters other than the PCI-to-ISA expansion bridge (PIIX4). PHLD#/PHLDA# are the arbitration request/grant signals for the PIIX4 and provide guaranteed access time capability for ISA masters. PHLD#/PHLDA# also optimize system performance based on the PIIX4 known policies.

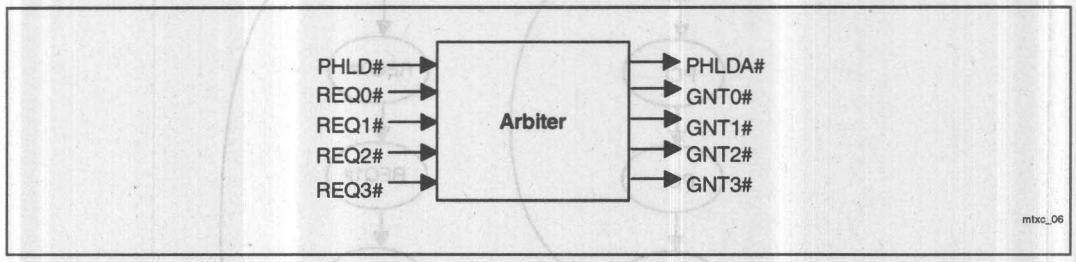
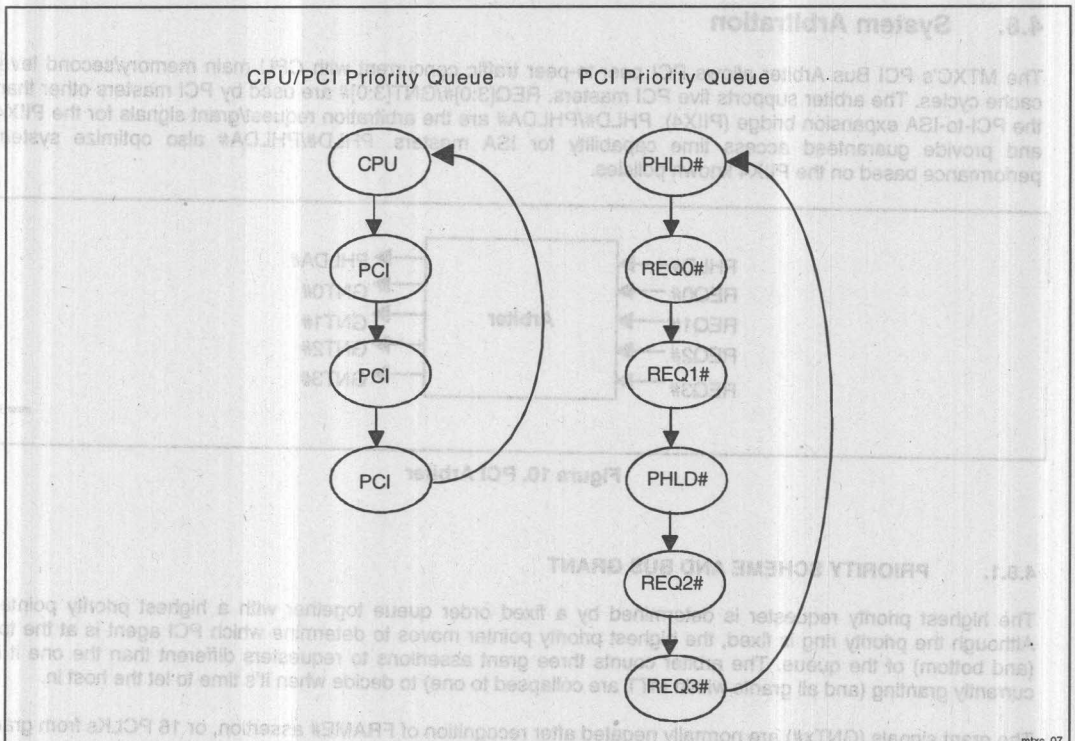


Figure 10. PCI Arbiter

4.8.1. PRIORITY SCHEME AND BUS GRANT

The highest priority requester is determined by a fixed order queue together with a highest priority pointer. Although the priority ring is fixed, the highest priority pointer moves to determine which PCI agent is at the top (and bottom) of the queue. The arbiter counts three grant assertions to requesters different than the one it is currently granting (and all grants within MTT are collapsed to one) to decide when it's time to let the host in.

The grant signals (GNTx#) are normally negated after recognition of FRAME# assertion, or 16 PCLKs from grant assertion, if no cycle has started.



NOTES:

1. In the PCI Priority Queue, the last agent granted is always dropped to the bottom of the queue for the next arbitration cycle, but the order of the chain is always preserved.
2. In the PCI Priority Queue, if PHLD is at the bottom of the queue, the upper PHLD slot is masked. This prevents back-to-back PHLD grants, if other PCI request are pending.
3. In the CPU/PCI priority Queue, the CPU is granted high priority status after 3 consecutive PCI grants. If three consecutive PCI grants have not been counted down, then the CPU can be granted the bus as the low priority agent.

Figure 11. Arbitration Priority Rotation

Multi-Transaction Timer (MTT)

The priority chain algorithm has been enhanced by the Multi-Transaction Timer (MTT) mechanism. Once a PCI agent is granted, the MTT is started. This timer then counts down in PCI clocks from its preset value to zero. Until the timer expires, that agent will be promoted to being the highest priority PCI agent for the next grant event.

4.8.2. CPU POLICIES

The CPU never explicitly requests the bus. Instead, the arbiter grants the bus to the CPU when:

- The CPU is the highest priority
- PCI agents do not require main memory (peer-to-peer transfers or bus idle) and the PCI bus is not currently locked by a PCI master

When the CPU is granted as highest priority, the MLT timer is used to guarantee a minimum amount of system resources to the CPU before another requesting PCI agent is granted.

5.0. CLOCKS AND RESET

5.1. Clock Generation and distribution

The MTXC and CPU should be clocked from one clock driver output to minimize skew between the CPU & MTXC.

5.2. RESET Sequencing

The MTXC is asynchronously reset when the RST# signal is asserted.

The MTXC arbiter includes support for PCI central resource functions. These functions include driving the AD[31:0],C/BE[3:0]#, and the PAR signals when no one is granted the PCI bus and the PCI bus is idle. The MTXC drives 0's on these signals during these times, plus during RESET.

6.0. PINOUT INFORMATION



Figure 12. MTXC Pinout (Top View)

Table 23. MTXC Alphabetical Pin List

Pin	Ball
A10	Y07
A11	W07
A12	U07
A13	Y06
A14	V06
A15	W06
A16	U06
A17	Y05
A18	W05
A19	V05
A20	U05
A21	V09
A22	U10
A23	U09
A24	W10
A25	W09
A26	V10
A27	Y09
A28	Y10
A29	U11
A3	V11
A30	W11
A31	W08
A4	Y11
A5	U08
A6	T11
A7	Y08
A8	V08
A9	V07

Table 23. MTXC Alphabetical Pin List

Pin	Ball
AD0	A15
AD1	A14
AD10	B10
AD11	A10
AD12	C09
AD13	B09
AD14	A09
AD15	C08
AD16	C07
AD17	B07
AD18	A07
AD19	C06
AD2	B13
AD20	B06
AD21	A06
AD22	C05
AD23	B05
AD24	D06
AD25	C04
AD26	B04
AD27	A04
AD28	B03
AD29	A03
AD3	A13
AD30	B02
AD31	A02
AD4	C12
AD5	B12
AD6	A12

Table 23. MTXC Alphabetical Pin List

Pin	Ball
AD7	C11
AD8	A11
AD9	C10
ADS#	T05
AHOLD	L05
BE0#	K02
BE1#	K03
BE2#	K04
BE3#	L01
BE4#	L02
BE5#	L03
BE6#	L04
BE7#	M01
BOFF#	P05
BRDY#	M05
BWE#	Y12
C/BE0#	B11
C/BE1#	B08
C/BE2#	A08
C/BE3#	A05
CACHE#	J05
CADS#	U12
CADV#	W12
CAS0#/DQM0#	U18
CAS1#/DQM1#	W20
CAS2#/DQM2#	V20
CAS3#/DQM3#	T17
CAS4#/DQM4#	T19
CAS5#/DQM5#	U19

Table 23. MTXC Alphabetical Pin List

Pin	Ball
CAS6#/DQM6#	P17
CAS7#/DQM7#	T18
CCS#	W13
CKE/MAA0	U20
CKEB/MAA1	W16
CLKRUN#	C13
COE#	V12
D/C#	T07
DEVSEL#	E09
EADS#	R05
FRAME#	E06
GNT0#	D08
GNT1#	D10
GNT2#	D12
GNT3#	D14
GWE#	V13
HCLKIN	K16
HD0	Y01
HD1	Y03
HD10	V03
HD11	W04
HD12	T01
HD13	V04
HD14	U03
HD15	V02
HD16	U04
HD17	T02
HD18	U02
HD19	R03

Table 23. MTXC Alphabetical Pin List

Pin	Ball
HD2	Y02
HD20	T04
HD21	R02
HD22	T03
HD23	P01
HD24	R04
HD25	P03
HD26	P02
HD27	N01
HD28	P04
HD29	N03
HD3	Y04
HD30	N02
HD31	N04
HD32	M03
HD33	M02
HD34	K01
HD35	M04
HD36	J02
HD37	J01
HD38	J04
HD39	H01
HD4	W01
HD40	H02
HD41	G02
HD42	J03
HD43	G04
HD44	H04
HD45	G01

Table 23. MTXC Alphabetical Pin List

Pin	Ball
HD46	H03
HD47	F02
HD48	F01
HD49	G03
HD5	W02
HD50	F04
HD51	F03
HD52	E01
HD53	E04
HD54	E02
HD55	D01
HD56	E03
HD57	D03
HD58	D02
HD59	C01
HD6	V01
HD60	C02
HD61	C03
HD62	B01
HD63	A01
HD7	R01
HD8	U01
HD9	W03
HITM#	T08
HLOCK#	G05
IRDY#	E07
KEN#	K05
KRQAK/ CS4_64#	V17
LOCK#	E05

Table 23. MTXC Alphabetical Pin List

Pin	Ball
M/IO#	H05
MA0	V15
MA1	V16
MA10	U16
MA11/BA0	Y19
MA2	Y17
MA3	T14
MA4	U15
MA5	Y16
MA6	W18
MA7	Y18
MA8	W19
MA9	U17
MD0	H17
MD1	J16
MD10	C19
MD11	R20
MD12	B18
MD13	B16
MD14	B15
MD15	E13
MD16	H16
MD17	H20
MD18	G18
MD19	F20
MD2	J17
MD20	M19
MD21	N19
MD22	M20

Table 23. MTXC Alphabetical Pin List

Pin	Ball
MD23	J20
MD24	E19
MD25	E17
MD26	D18
MD27	A19
MD28	C17
MD29	A17
MD3	L17
MD30	D16
MD31	B14
MD32	G17
MD33	F17
MD34	K17
MD35	G16
MD36	G19
MD37	L18
MD38	L19
MD39	K18
MD4	H18
MD40	F19
MD41	E18
MD42	C20
MD43	A20
MD44	D17
MD45	C16
MD46	D15
MD47	C14
MD48	F16
MD49	E16

Table 23. MTXC Alphabetical Pin List

Pin	Ball
MD5	H19
MD50	G20
MD51	N20
MD52	J18
MD53	M17
MD54	K20
MD55	J19
MD56	E20
MD57	D19
MD58	B20
MD59	B19
MD6	L20
MD60	A18
MD61	B17
MD62	C18
MD63	C15
MD7	K19
MD8	F18
MD9	D20
MWE#	R18
MWEB#	V18
NA#	N05
PAR	A16
PCLKIN	E10
PHLD#	D04
PHLDA#	D05
RAS0#/CS0#	Y20
RAS1#/CS1#	P18
RAS2#/CS2/#	R17

Table 23. MTXC Alphabetical Pin List

Pin	Ball
RAS3#/CS3#	N17
RAS4#/CS4#/ BA1	V19
RAS5#/CS5#/ MA13	M16
REQ0#	D07
REQ1#	D09
REQ2#	D11
REQ3#	D13
RST#	T15
SCASA#	P19
SCASB#	M18
SMIACT#	T10
SRASA#	N18
SRASB#	P20
STOP#	E11
SUSCLK	T20
SUSSTAT1#	R19

Table 23. MTXC Alphabetical Pin List

Pin	Ball
TEST#	W17
TIO0	U14
TIO1	Y14
TIO2	V14
TIO3	T12
TIO4	W15
TIO5	Y15
TIO6	U13
TIO7	W14
TRDY#	E08
TWE#	Y13
W/R#	T09
Vcc	F05, L16, R15, F15, E12, P15, F14, T13

Table 23. MTXC Alphabetical Pin List

Pin	Ball
Vcc (CPU)	F06, G06, R07, R06
Vcc (SUS)	R16, N16, P16
Vcc5REF	E14
Vss	E15, J9, J10 J11, J12, K09, K10, K11, K12, L09, L10, L11, L12, M09, M10, M11, M12, T06, T16

7.0. MTXC PACKAGE INFORMATION

This specification outlines the mechanical dimensions for the MTXC. The package is a 324 pin ball grid array (BGA).

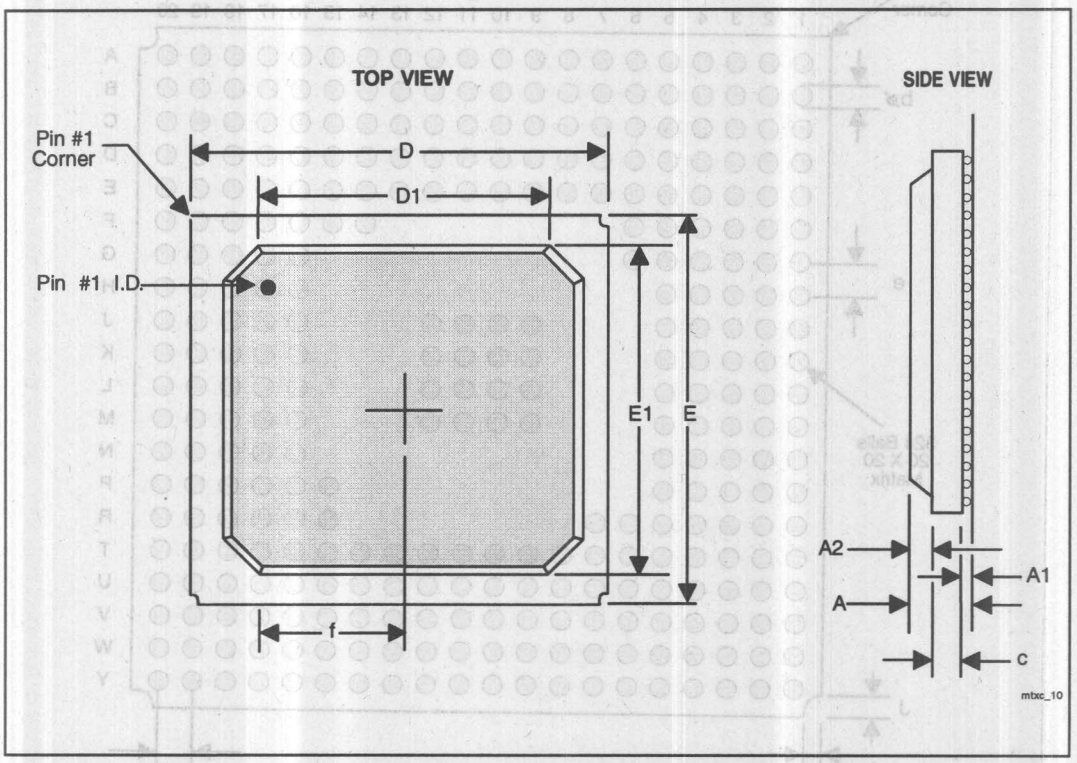


Figure 13. MTXC 324-pin Ball Grid Array (BGA)

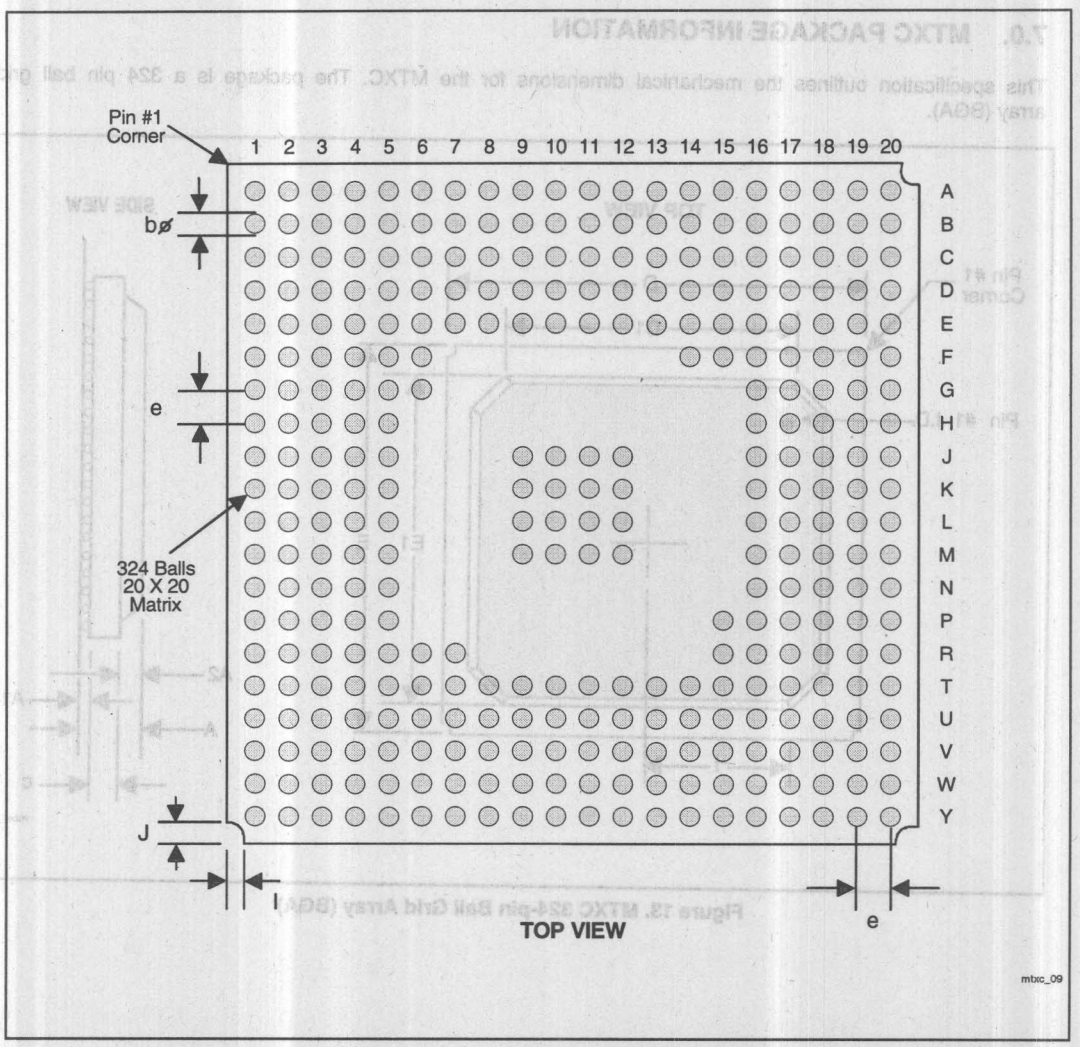


Figure 14. MTXC 324-pin Ball Grid Array (BGA) Ball Pattern

Table 24. MTXC 324-pin Ball Grid Array (BGA)

Symbol	e=1.27 (solder ball pitch)		
	Min[1]	Nominal[1]	Max[1]
A	1.95	2.13	2.28
A1	0.50	0.60	0.70
A2	1.12	1.17	1.22
D	26.80	27.00	27.20
D1	24.00		24.70
E	26.80	27.00	27.20
E1	24.00		24.70
I	1.44 REF.		
J	1.44 REF.		
M[2]	20 (Depopulated)		
N[3]	324		
b	0.60	0.76	0.90
c	0.32	0.36	0.40
f	8.05 REF.		
Remark	2 Layer		

NOTES:

1. All dimensions are in millimeters.
2. 'M' represents the maximum solder ball matrix size.
3. 'N' represents the maximum allowable number of solder balls.

8.0. TESTABILITY

8.1. NAND Tree Mode

A NAND tree mode is provided for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to set the connectivity of each of the MTXC's signal pins. In Mobile/desktop mode, the NAND tree mode is activated by driving the test pin TEST# low when REQx# pins are at 0010. If TEST# is negated at any time, the test mode is deactivated and the MTXC goes back to normal operation. There is no guarantee that upon re-entering normal operation the chip will function properly, if the test mode was entered while the MTXC was not in a completely idle state.

The MTXC has several test modes to improve board manufacturing. If the TEST# signal is asserted (driven low), the value on the REQ[3:0]# indicates the test mode to enable. The test mode enabled at the falling edge of TEST# will remain enabled until TEST# is negated.

Table 25 shows each test mode and the value of REQ#[3:0] required to enable it. All other values of REQ[3:0]# while TEST# is active, are reserved and should not be asserted by the customer.

Table 25. Test Modes

REQ[3:0]#	TEST#	PHLD#	TEST Mode	Description
0010	0	x	NAND Chain	Float outputs, enable NAND chains on GNT[3:0]#
1110	0	1	ID/REV code	Drives Device ID on AD[31:16] and revision ID on AD[7:0]
1110	0	0	MID Code	Drives Manufacture ID on AD[31:0]
1111	0	x	Disable test mode[1]	Disables any active test mode, puts MTXC back into normal mode

NOTES:

1. It is recommended to assert RST# if this mode is used, to guarantee pins and PCIset will function normally.

8.2. NAND Chain Mode

In NAND Tree mode, all outputs are tri-stated, except for GNT#[3:0]. These pins contain the NAND Chain. Note, also, that the internal pull-ups and pull-downs are still active. Because of the 282 pins in the NAND Chain, it must be separated into 4 chains. Two chains contain 72 pins each, 1 chain contains 70 pins, and 1 chain contains 68 pins. The MTXC remains in this mode until a new test mode is selected or RST# is asserted. The HCLK and PCLK are part of the NAND Chain and *must* be deactivated during this test.

HCLK and PCLK need to run for a few clocks in the beginning to put the MTXC in the NAND chain mode. During the testing of chains 2 and 3, SUSSTAT# will be held high throughout the test. RST#, TEST#, and SUSSTAT1# are not part of the NAND chain. The following tables show the pin order for each chain:

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
A25	CH0_00
A7	CH0_01
A10	CH0_02
A21	CH0_03
A23	CH0_04
SMIACT#	CH0_05
A31	CH0_06
A18	CH0_07
HD3	CH0_08
A12	CH0_09
A14	CH0_10
HD11	CH0_11
A19	CH0_12
A16	CH0_13
HITM#	CH0_14
HD13	CH0_15
D/C#	CH0_16
HD0	CH0_17
HD10	CH0_18
HD16	CH0_19
HD6	CH0_20
HD14	CH0_21
BOFF#	CH0_22
HD18	CH0_23

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
HD24	CH0_24
HD8	CH0_25
HD19	CH0_26
HD7	CH0_27
HD31	CH0_28
HD26	CH0_29
HD27	CH0_30
HD33	CH0_31
AHOLD	CH0_32
BE5#	CH0_33
BE6#	CH0_34
HD34	CH0_35
BE2#	CH0_36
BE0#	CH0_37
HD37	CH0_38
BE1#	CH0_39
HD36	CH0_40
HD41	CH0_41
HD52	CH0_42
CACHE#	CH0_43
HD47	CH0_44
HD44	CH0_45
HD49	CH0_46
HD54	CH0_47

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
HD55	CH0_48
HD57	CH0_49
HLOCK#	CH0_50
HD53	CH0_51
HD60	CH0_52
HD62	CH0_53
HD61	CH0_54
AD30	CH0_55
AD25	CH0_56
AD22	CH0_57
AD24	CH0_58
AD27	CH0_59
AD19	CH0_60
C/BE3#	CH0_61
REQ0#	CH0_62
AD20	CH0_63
AD21	CH0_64
TRDY#	CH0_65
AD16	CH0_66
C/BE2#	CH0_67
C/BE1#	CH0_68
AD14	CH0_69
AD12	CH0_70
AD13	CH0_71

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
A24	CH1_00
A27	CH1_01
A26	CH1_02
A13	CH1_03
A8	CH1_04
W/R#	CH1_05
A11	CH1_06
A17	CH1_07
A15	CH1_08
A5	CH1_09
A9	CH1_10
HD1	CH1_11
HD9	CH1_12
A20	CH1_13
HD2	CH1_14
HD5	CH1_15
HD4	CH1_16
ADS#	CH1_17
HD15	CH1_18
EADS#	CH1_19
HD20	CH1_20
HD17	CH1_21
HD22	CH1_22
HD12	CH1_23

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
HD28	CH1_24
HD21	CH1_25
NA#	CH1_26
HD25	CH1_27
BRDY#	CH1_28
HD23	CH1_29
HD35	CH1_30
HD29	CH1_31
HD30	CH1_32
BE7#	CH1_33
HD32	CH1_34
BE3#	CH1_35
BE4#	CH1_36
HD39	CH1_37
HD45	CH1_38
HD42	CH1_39
HD38	CH1_40
HD40	CH1_41
HD48	CH1_42
KEN#	CH1_43
HD46	CH1_44
HD43	CH1_45
HD51	CH1_46
HD58	CH1_47

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
HD56	CH1_48
HD50	CH1_49
M/IO#	CH1_50
HD59	CH1_51
HD63	CH1_52
PHLD#	CH1_53
AD31	CH1_54
LOCK#	CH1_55
AD28	CH1_56
FRAME#	CH1_57
AD29	CH1_58
PHLDA#	CH1_59
IRDY#	CH1_60
AD26	CH1_61
AD23	CH1_62
AD17	CH1_63
DEVSEL#	CH1_64
AD18	CH1_65
REQ1#	CH1_66
AD15	CH1_67
PCLKIN	CH1_68
AD11	CH1_69
AD10	CH1_70
AD9	CH1_71

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
A28	CH2_00
A29	CH2_01
A3	CH2_02
A30	CH2_03
A4	CH2_04
COE#	CH2_05
BWE#	CH2_06
CCS#	CH2_07
MA5	CH2_08
MA10	CH2_09
KRQAK/ CS4_64#	CH2_10
MA7	CH2_11
MA11	CH2_12
MA6	CH2_13
MA9	CH2_14
MWEB#	CH2_15
RAS0#	CH2_16
RAS4#	CH2_17
RAS2#	CH2_18
CAS7#	CH2_19
CAS5#	CH2_20
CAS6#	CH2_21
CKE/MAA0	CH2_22

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
CAS4#	CH2_23
SUSCLK	CH2_24
SRASA	CH2_25
MD11	CH2_26
MD53	CH2_27
SCASB#	CH2_28
MD22	CH2_29
MD6	CH2_30
MD34	CH2_31
MD39	CH2_32
MD7	CH2_33
MD54	CH2_34
HCLKIN	CH2_35
MD55	CH2_36
MD5	CH2_37
MD17	CH2_38
MD2	CH2_39
MD50	CH2_40
MD1	CH2_41
MD0	CH2_42
MD18	CH2_43
MD16	CH2_44
MD19	CH2_45
MD40	CH2_46

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
MD32	CH2_47
MD25	CH2_48
MD26	CH2_49
MD42	CH2_50
MD48	CH2_51
MD49	CH2_52
MD59	CH2_53
MD43	CH2_54
MD30	CH2_55
MD27	CH2_56
MD28	CH2_57
MD12	CH2_58
MD60	CH2_59
CLKRUN#	CH2_60
AD0	CH2_61
AD2	CH2_62
STOP#	CH2_63
AD4	CH2_64
AD3	CH2_65
AD5	CH2_66
AD7	CH2_67
AD6	CH2_68
REQ2#	CH2_69

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
A22	CH3_00
CADV#	CH3_01
A6	CH3_02
TWE#	CH3_03
GWE#	CH3_04
CADS#	CH3_05
TIO1	CH3_06
TIO3	CH3_07
TIO7	CH3_08
TIO6	CH3_09
TIO2	CH3_10
TIO5	CH3_11
TIO4	CH3_12
TIO0	CH3_13
MA0	CH3_14
MA2	CH3_15
MA4	CH3_16
CKEB/ MAA1	CH3_17
MA1	CH3_18
MA3	CH3_19
MA8	CH3_20
CAS1#	CH3_21
CAS3#	CH3_22

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
CAS0#	CH3_23
CAS2#	CH3_24
MWEB#	CH3_25
RAS1#	CH3_26
RAS3#	CH3_27
RAS5#	CH3_28
SCASA	CH3_29
MD21	CH3_30
SRASB#	CH3_31
MD51	CH3_32
MD20	CH3_33
MD37	CH3_34
MD38	CH3_35
MD3	CH3_36
MD52	CH3_37
MD23	CH3_38
MD4	CH3_39
MD36	CH3_40
MD56	CH3_41
MD8	CH3_42
MD9	CH3_43
MD33	CH3_44
MD24	CH3_45

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
MD41	CH3_46
MD57	CH3_47
MD35	CH3_48
MD58	CH3_49
MD10	CH3_50
MD44	CH3_51
MD62	CH3_52
MD15	CH3_53
MD46	CH3_54
MD45	CH3_55
MD61	CH3_56
MD63	CH3_57
MD29	CH3_58
MD13	CH3_59
MD47	CH3_60
REQ3#	CH3_61
MD14	CH3_62
PAR	CH3_63
MD31	CH3_64
AD1	CH3_65
C/BE0#	CH3_66
AD8	CH3_67

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DATASHEET
ADDENDUM

Intel 430TX PCIset System Controller (MTXC) Timing Specification

273134-001
October, 1997

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DATASHEET
ADDENDUM

Intel 430TX PCIset
System Controller (MTXC)
Timing Specification

27734-001
October 1997

82439TX System Controller (MTXC) Features

- Supports Mobile and Desktop
- Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3 V and 2.5 V
- PCI 2.1 Compliant
- Integrated Data Path
- Integrated DRAM Controller
  - 4 Mbytes to 256 Mbytes main memory
  - 64-Mbit DRAM/SDRAM Technology Support
  - FPM (Fast Page Mode), EDO and SDRAM DRAM Support
  - 6 RAS Lines Available
  - Integrated Programmable Strength for DRAM Interface
  - CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO
  - CAS-Before-RAS and Self Refresh for SDRAM
- Integrated L2 Cache Controller
  - 64-MB DRAM Cacheability
  - Direct Mapped Organization—Write Back Only
  - Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1
  - 64K x 32 SRAM Also Supported
- Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface
  - Five PCI Bus Masters (including PIIX4)
  - 10 DWord PCI-to-DRAM Read Prefetch Buffer
  - 18 DWord PCI-DRAM Post Buffer
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions
- Power Management Features
  - PCI CLKRUN# Support
  - Dynamic Stop Clock Support
  - Suspend to RAM (STR)
  - Suspend to Disk (STD)
  - Power On Suspend (POS)
  - Internal Clock Control
  - SDRAM and EDO Self Refresh During Suspend
  - ACPI Support
  - Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM)
  - SMM Writeback Cacheable in E_SMRAM Mode up to 1 Mbyte
  - 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support
- Test Features
  - NAND Tree Support for all Pins
- Supports the Universal Serial Bus (USB)
- 324-Pin mBGA 430TX PCIset Xcelerated Controller (MTXC) with Integrated Data Paths

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 82439TX System Controller (MTXC). Please refer to the standard package datasheet (order number 290559) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

82439TX System Controller (MTXC) Features

- Supports Mobile and Desktop
- Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3 V and 2.5 V
- PCI 2.1 Compliant
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- Integrated DRAM Controller
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  - SMM Writeback Cacheable in E_SMRAM Mode up to 1 Mbyte
  - 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support
- Test Features
  - NAND Tree Support for all Pins
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REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 82439TX System Controller (MTXC). Please refer to the standard package datasheet (order number 290559) for product information and specifications not found in this document.

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1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Case Temperature under Bias ..... 0°C to +85°C
Storage Temperature ..... -55°C to +150°C

Voltage on 5 V tolerant pins with respect to ground ..... -0.3 to $V_{CC}5REF$ + 0.3
Voltage on 3.3 V pins with respect to ground ..... -0.3 to V_{CC} + 0.3
Supply Voltage with respect to V_{SS} ..... -0.3 to +3.6 V
(2.5 V CPU) Supply Voltage with respect to V_{SS} ..... -0.2 to +2.7 V

Maximum Power Dissipation ..... 1.0 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1.2 Thermal Characteristics

The MTXC is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the MTXC are provided in Table 1.

Table 1. MTXC Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/Watt)	34	26
θ_{jc} (°C/Watt)	8	

					V_{CC} =3.135 V
V_{IL2}	Input Low Voltage	-0.3	0.7	V	Note 1 V_{CC}(CPU) = 2.375 V
V_{IH1}	Input High Voltage (3.3 V signals)	2.2	V_{CC} + 0.3	V	Notes 1, 2, 3 V_{CC} = 3.6 V
V_{IH2}	Input High Voltage (2.5 V signals)	1.7	V_{CC} + 0.3	V	Note 1 V_{CC} = 2.7 V
V_{IH3}	Input High Voltage (5 V signals)	2.2	VREF + 0.3	V	Note 2 VREF = 5.25 V
V_{OL1}	Output Low Voltage IOL = 1 mA (all signals except as noted below) IOL = 3 mA (Note 4) IOL = 6 mA (Note 5)		0.4	V	3.3 V signals (Note 7)
V_{OL2}	Output Low Voltage IOL = 100 µA IOL = 1 mA IOL = 2 mA		 0.2 0.3 0.4	V	2.5 V Signals Note 1

NOTES:

1. These signals are CPU V_{CC} (3.3 V or 2.5 V):
   A[31:3], BE[7:0]#, BRDY#, NA#, AHOLD, EADS#, HD[63:0], KEN#/INV, HLOCK#, M/IO#,D/C#, W/R#, ADS#, HITM#, CACHE#, SMIACT#, HCLKIN, V_{CC}(CPU)
2. These signals are 3.3 V with 5.0 V tolerance:
   TIO[7:0], AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, REQ[3:0]#, PCLKIN, PHLD#, MD[63:0], TESTIN#, PCLKIN, VREF, LOCK#, PHLDA#, CLKRUN#, RST#
3. These signals are 3.3 V:
   KRQAK, TWE#, BWE#, GWE#, COE#, CCS#, CADS#, CADV#, CKEB, CKE, SCAS[A,B]#, MWE#, MWEB#, MA[11:0], CAS[7:0]# or DQM[7:0], RAS[5:0]# or CS[5:0]#, V_{CC}(SUS), V_{CC}, SUSTAT1#, SUSCLK, GNT[3:0]#
4. I_{OL} and I_{OH} apply to the following signals: AD[31:0], C/BE[3:0]#, PAR
5. I_{OL} and I_{OH} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#
6. I_{IL} applies to the following signals: HD[63:0], MD[63:0], KRQAK, TIO[7:0], A27. These signals have internal pulldown resistors.
7. All signals from note 1 when the CPU V_{CC} is 3.3 V; All signals from notes 2 and 3.
8. Threshold voltage for all delay and pulse width measurements.

Table 2. MTXC DC Characteristics (Sheet 2 of 2)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{OH1}	Output High Voltage IOH = -1 mA (all signals except as noted below) IOH = -2 mA (Notes 4,5)	2.4		V	3.3 V signals (Note 7)
V_{OH2}	Output High Voltage IOH = -100 µA IOH = -1 mA IOH = -2 mA	 2.1 1.9 1.7		V	2.5 V Signals Note 1
V_{T1}	Threshold Voltage (3.3 V Signals)	1.5	1.5	V	Note 8
V_{T2}	Threshold Voltage (2.5 V Signals)	1.25	1.25	V	Note 8
I_{IL1}	Input Leakage Current		±10	µA	0 V<Vin<V_{CC}
I_{IL2}	Input Leakage Current		±300	µA	Note 6 0 V<Vin<V_{CC}
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. These signals are CPU V_{CC} (3.3 V or 2.5 V):
   A[31:3], BE[7:0]#, BRDY#, NA#, AHOLD, EADS#, HD[63:0], KEN#/INV, HLOCK#, M/IO#,D/C#, W/R#, ADS#, HITM#, CACHE#, SMIACT#, HCLKIN, V_{CC}(CPU)
2. These signals are 3.3 V with 5.0 V tolerance:
   TIO[7:0], AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, REQ[3:0]#, PCLKIN, PHLD#, MD[63:0], TESTIN#, PCLKIN, VREF, LOCK#, PHLDA#, CLKRUN#, RST#
3. These signals are 3.3 V:
   KRQAK, TWE#, BWE#, GWE#, COE#, CCS#, CADS#, CADV#, CKEB, CKE, SCAS[A,B]#, MWE#, MWEB#, MA[11:0], CAS[7:0]# or DQM[7:0], RAS[5:0]# or CS[5:0]#, V_{CC}(SUS), V_{CC}, SUSTAT1#, SUSCLK, GNT[3:0]#
4. I_{OL} and I_{OH} apply to the following signals: AD[31:0], C/BE[3:0]#, PAR
5. I_{OL} and I_{OH} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#
6. I_{IL} applies to the following signals: HD[63:0], MD[63:0], KRQAK, TIO[7:0], A27. These signals have internal pulldown resistors.
7. All signals from note 1 when the CPU V_{CC} is 3.3 V; All signals from notes 2 and 3.
8. Threshold voltage for all delay and pulse width measurements.

Table 3. MTXC Pin States in Various System Modes (Sheet 1 of 2)

MTXC Signals		Power Plane	Type	Buffer[1]	During Reset	After Reset	Max	Chip Standby	During POS	During STR
Host Interface	A[31:3]	V_{CC}(CPU)	I/O	3.3/2.5 V	Low[2]	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	BE[7:0]#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	ADS#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	BRDY#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	NA#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	AHOLD	V_{CC}(CPU)	O	3.3/2.5 V	High	Low	Toggling	Low	Low	Pwrdn
	EADS#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	BOFF#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	HITM#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	W/R#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	HLOCK#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	CACHE#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	KEN#/INV	V_{CC}(CPU)	O	3.3/2.5 V	Low	Low	Toggling	Low	Low	Pwrdn
	SMIACT#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	HD[63:0]	V_{CC}(CPU)	I/O	3.3/2.5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
DRAM Interface	RAS[5:0]#/ CS[5:0]#	V_{CC}(SUS)	O	3.3 V	Undef	High	Toggling	Toggling	Toggling	Toggling
	CAS[7:0]#/ DQM[7:0]	V_{CC}(SUS)	O	3.3 V	Undef	Undef	Toggling	Toggling	Toggling	Toggling
	MA[11:0]	V_{CC}	O	3.3 V	Undef	Undef	Toggling	Low	Low	Pwrdn
	MWE# MWEB#	V_{CC}(SUS)	O	3.3 V	High	High	Toggling	High	High	High
	SRAS[A,B]#	V_{CC}	O	3.3 V	High	High	Toggling	Toggling	Low	Pwrdn
	SCAS[A,B]#	V_{CC}	O	3.3 V	High	High	Toggling	Toggling	Low	Pwrdn
	CKE	V_{CC}(SUS)	O	3.3 V	Undef	High	High	High	Low	Low
	CKEB	V_{CC}	O	3.3 V	Undef	High	High	High	Low	Pwrdn
	MD[63:0]	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn

NOTES:

1. 3.3/2.5 V indicates the buffer is 3.3 V or 2.5 V only, depending upon the V_{CC}(CPU) voltage. 3.3/5 V indicates that the output is 3.3 V, and input is 3.3 V with 5 V tolerance. 5 V indicates 3.3 V input with 5 V tolerance.
2. A[31:26] are inputs during Reset.

Table 3. MTXC Pin States in Various System Modes (Sheet 2 of 2)

MTXC Signals		Power Plane	Type	Buffer[1]	During Reset	After Reset	Max	Chip Standby	During POS	During STR
L2 Cache Interface	CADV#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	CADS#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	CCS#	V_{CC}	O	3.3 V	Low	Low	Low	Low	Low	Pwrdn
	COE#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	GWE#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	BWE#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	TIO[7:0]	V_{CC}	I/O	3.3 V	Low	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	TWE#	V_{CC}	O	3.3 V	Low	High	Toggling	High	High	Pwrdn
	KRQAK / CS4_64#	V_{CC}	I/O	3.3 V	Input	Input	Toggling	Input	Input	Pwrdn
PCI Interface	AD[31:0]	V_{CC}	I/O	3.3/5 V	Low	Hi-Z	Toggling	Last	Last	Pwrdn
	C/BE[3:0]#	V_{CC}	I/O	3.3/5 V	Low	Hi-Z	Toggling	Last	Last	Pwrdn
	FRAME#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	DEVSEL#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	IRDY#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	TRDY#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	STOP#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	LOCK#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	REQ[3:0]#	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
	GNT[3:0]#	V_{CC}	O	3.3 V	Hi-Z	High	Toggling	High	High	Pwrdn
	PHLD#	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
	PHLDA#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	PAR	V_{CC}	I/O	3.3/5 V	Low	Undef	Toggling	Undef	Undef	Pwrdn
	CLKRUN#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Low	Low	High	Pwrdn
	RST#	V_{CC}	I	3.3/5 V	Input	Input	High	Input	Input	Pwrdn
Test / Clock Signals	TEST#	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
	HCLKIN	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Input	Input	Input	Pwrdn
	PCLKIN	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
Power Management	SUSCLK	V_{CC}(SUS)	I	3.3 V	Input	Input	Input	Input	Input	Input
	SUSSTAT1#	V_{CC}(SUS)	I	3.3 V	Input	Input	Input	Input	Input	Input

NOTES:

1. 3.3/2.5 V indicates the buffer is 3.3 V or 2.5 V only, depending upon the V_{CC}(CPU) voltage. 3.3/5 V indicates that the output is 3.3 V, and input is 3.3 V with 5 V tolerance. 5 V indicates 3.3 V input with 5 V tolerance.
2. A[31:26] are inputs during Reset.

For the Standby State, the following assumptions are made:

- Host bus is idle
- PCI bus is idle
- DRAM bus is idle except for DRAM refresh cycles
- All external clocks are running: HCLK (66 MHz), PCLOCK (33 MHz), SUSCLK (32 KHz)
- Not in any suspend state
- No PCI activity

For the MAX state, the following assumptions are made:

- Host Bus cycle in progress
- PCI bus cycle in progress
- DRAM bus cycle in progress

1.4 MTXC AC Characteristics

All timings are in nanoseconds (ns) unless otherwise specified.

Table 4. Host Clock Timing: 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t1	HCLKIN Period	15.0	20.0	1	
t1s	HCLKIN Period Stability		±250		pS
t1H	HCLKIN High Time	5.5		1	
t1L	HCLKIN Low Time	5.5		1	
t1r	HCLKIN Rise Time		1.5	1	
t1f	HCLKIN Fall Time		1.5	1	

Table 5. CPU Interface Timing: 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t2	ADS# Setup Time to HCLKIN Rising	5.0		4	
t3	W/R# Setup Time to HCLKIN Rising	5.7		4	
t4	BE[7:0]# Setup Time to HCLKIN Rising	3.4		4	
t5	HITM# Setup Time to HCLKIN Rising	5.3		4	
t6	CACHE# Setup Time to HCLKIN Rising	5.0		4	
t7	M/IO# Setup Time to HCLKIN Rising	5.3		4	
t8	D/C# Setup Time to HCLKIN Rising	5.0		4	
t9	HLOCK#, SMIACT# Setup Time to HCLKIN Rising	4.0		4	
t11	ADS#, HITM#, W/R#, M/IO#, D/C#, BE[7:0]#, HLOCK#, CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.0		4	
t12	A[31:0] Setup Time to HCLKIN Rising	3.5		4	
t13	A[31:0] Hold Time from HCLKIN Rising	1.0		4	
t14	A[31:0] Valid Delay from HCLKIN Rising	2.0	13.0	3	0 pF
t15	A[31:0] Output Enable From HCLKIN Rising	0.0	13.0	8	
t16	A[31:0] Float Delay from HCLKIN Rising	0.0	13.0		
t17	HD(63:0) Setup Time to HCLK Rising	3.75			
t18	HD(63:0) Hold Time from HCLK Rising	1.0			
t19	HD(63:0) Valid Delay from HCLK Rising	1.5	7.0		0 pF
t20	HD(63:0) Flow Through Delay from MD[63:0], 66 MHz, 5-2-2-2	1.5	6.0		0 pF
t21	BRDY# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pF
t22	NA# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pF
t23	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t24	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t25	EADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t26	KEN#/INV Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF

Table 6. Second-Level Cache Timing: 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t27	COE# Valid Delay from HCLKIN Rising	2.0	8.0	3	0 pF
t28	GWE# Valid Delay from HCLKIN Rising	2.0	9.5	3	0 pF
t29	BWE# Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pF
t30	KRQAK Valid Delay from HCLKIN	1.5	7.0		0 pF
t31	KRQAK setup time to HCLKIN	2.8			
t32	KRQAK Hold Time from HCLKIN	1.0			
t33	TIO[7:0] Valid Delay from HCLKIN Rising	2.0	8.0	3	0 pF
t34	TIO[7:0] Setup time to HCLKIN Rising	2.2		4	
t35	TIO[7:0] Hold time to HCLKIN Rising	2.0		4	
t36	CCS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t37	CADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t38	CADV# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t39	TWE# Valid Delay	2.0	9.0	3	0 pF

Table 7. EDO/FPM DRAM Interface Timing; 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		Fig.	Notes
		Min	Max		
t40	RAS[5:0]# Valid Delay from HCLK Rising	1.5	7.0	3	0 pF
t41	CAS[7:0]# Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pF
t42	MWE#, MWEB# Valid Delay From HCLKIN Rising	1.5	19.0	3	0 pF
t43	MA[13:0] Flow Through Delay from HA (read col addr)	2.0	8.0		0 pF
t44	MA[13:0] Valid Delay from HCLK Rising (read row addr)	2.0	9.0		0 pF
t45	MA[11:0] Valid Delay from HCLK Rising (read col addr burst cycles)	2.0	6.5		0 pF (Also applies when CKE pins are used as copies of MA[1:0])
t46	MA[1:0] Valid Delay from HCLK Rising (Write Row and Col Addr)	2.0	10.0		0 pF
t48	MD[63:0] set up to HCLK Rising	1.1			
t49	MD[63:0] hold time from HCLK Rising	4.0			
t50	MD[63:0] Valid delay from HCLK Rising	2.0	8.0		0 pF
SDRAM Interface Timing					
t51	SRAS[B:A]# Valid Delay from HCLKIN Rising (two clock path)	5.0	19.0		0 pF
t52	SCAS[B:A]# Valid Delay from HCLKIN Rising (two clock path)	5.0	19.0		0 pF
t56	MWE#,MWEB# Valid delay from HCLKIN Rising (Two Clock Path)	5.0	19.0	3	0 pF
t57	CKE, CKEB Valid Delay from HCLKIN Rising	1.5	6.0		0 pF
t58	CS[5:0]# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t59	DQM[7:0] Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pF
t60	MA[11:0] Valid Delay from HCLKIN Rising	2.0	16.0	3	0 pF
t61	MD[63:0] set up to HCLK Rising	3.5			0 pF
t62	MD[63:0] hold time from HCLK Rising	1.0			0 pF
t62a	MD[63:0] Valid Delay from HCLK Rising	2.0	8.0		0 pF

Table 8. PCI Clock Timing; 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figure	Notes
		Min	Max		
PM and TEST Timing					
t63	SUSSTAT1# Setup Time	7			
t64	SUSSTAT1# Hold Time	2			
t64s	SUSCLK	Async			
t64t	TESTIN#	Async			
PCI Clocks					
t65	PCLKIN High Time	12.0		1	
t66	PCLKIN Low Time	12.0		1	
t66r	PCLKIN Rise Time		3.0	1	
t66f	PCLKIN Fall Time		3.0	1	

Table 9. PCI Interface Timing; 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t67	AD[31:0] Valid Delay	2	11	3	
t68	AD[31:0] Setup Time	7		4	
t63	AD[31:0] Hold Time from PCLKIN	0		4	
t70	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Valid Delay from PCLKIN Rising	2.0	11.0	3	
t71	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Output Enable Delay from PCLKIN Rising	2.0	11.0	8	
t72	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Float Delay from PCLKIN Rising	2.0	11.0	5	
t73	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Setup Time to PCLKIN Rising	7.0		4	
t74	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Hold Time from PCLKIN Rising	0.0		4	
t75	PHLDA# Valid Delay from PCLKIN Rising	2	9.0	3	
t76	GNT[3:0] # Valid Delay from PCLKIN Rising	2	9.0		
t77	REQx#, PHLD# Setup Time from PCLKIN Rising	12.0			
t78	REQx#, PHLD# Hold Time from PCLKIN Rising	0.0			
t79	RST# Low Pulse Width	1 ms		7	
t80	CLKRUN#	Async			

2.0 MTXC Timing Diagrams

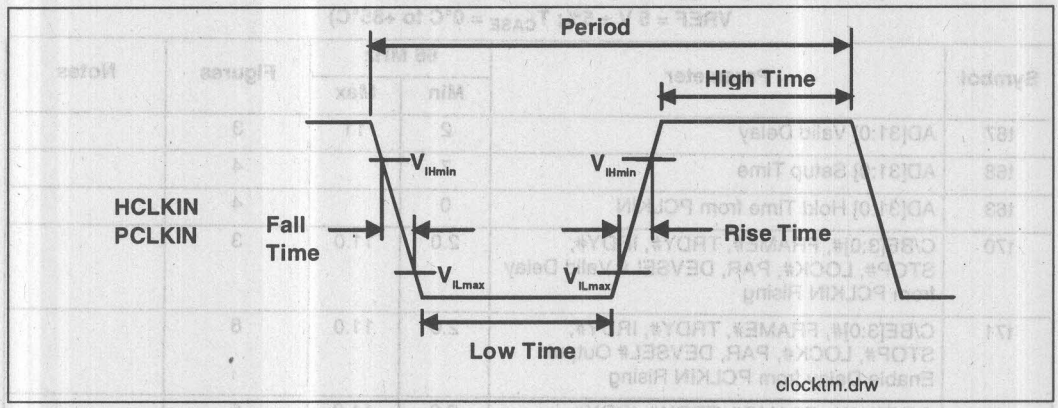


Figure 1. Clock Timing

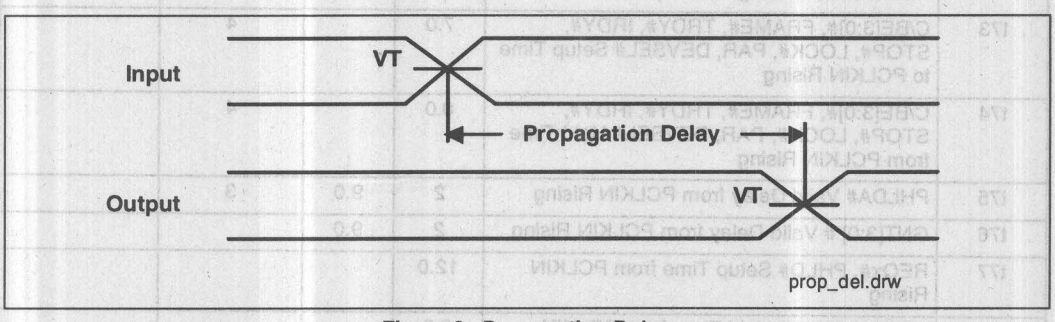


Figure 2. Propagation Delay

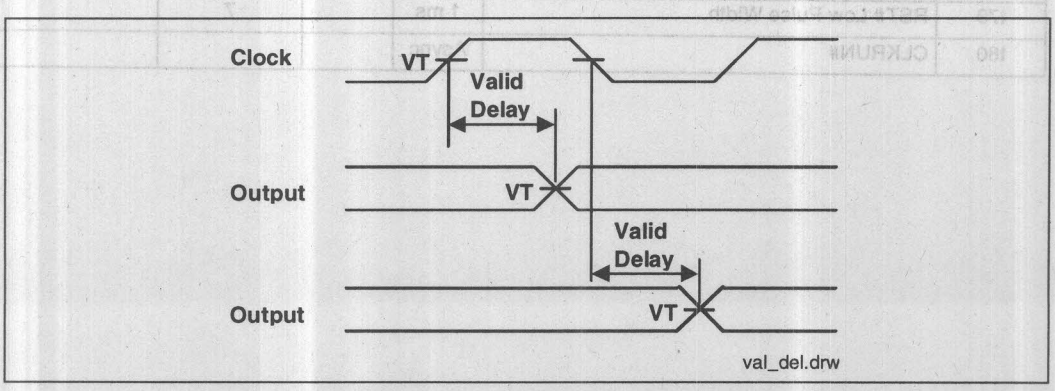


Figure 3. Valid Delay From Rising Clock Edge

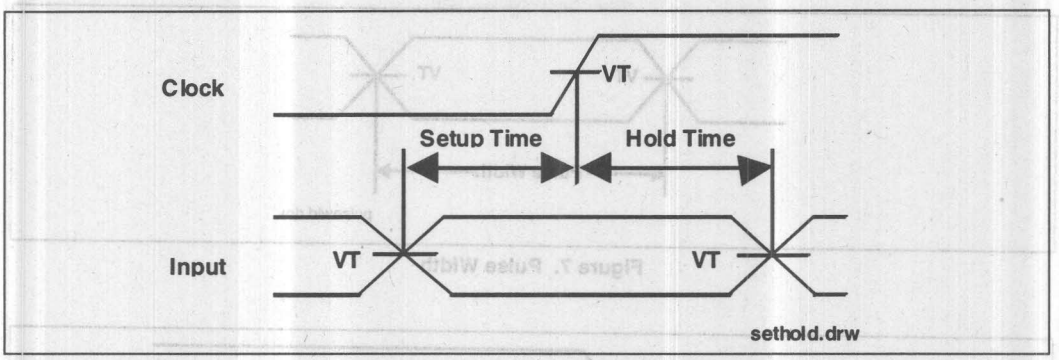


Figure 4. Setup and Hold Times

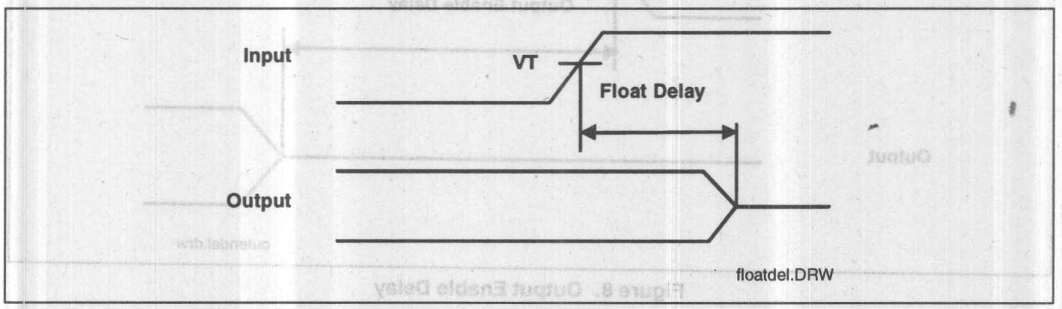
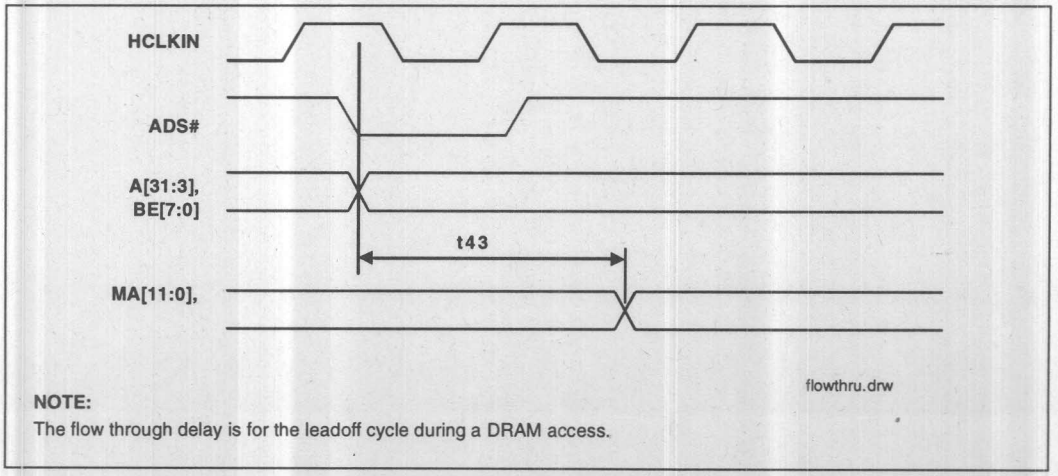


Figure 5. Float Delay



NOTE:
The flow through delay is for the leadoff cycle during a DRAM access.

Figure 6. Flow Through Delay

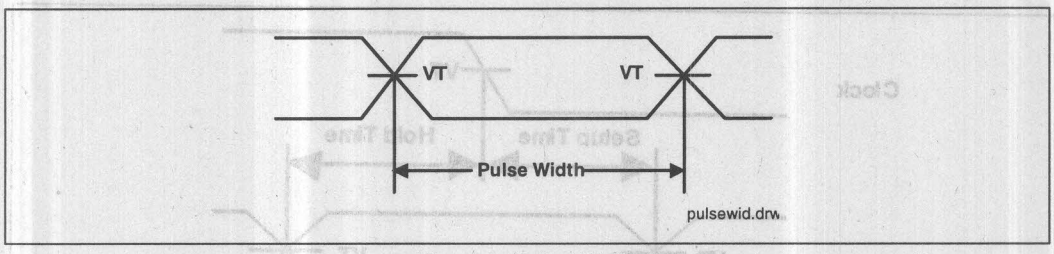


Figure 7. Pulse Width

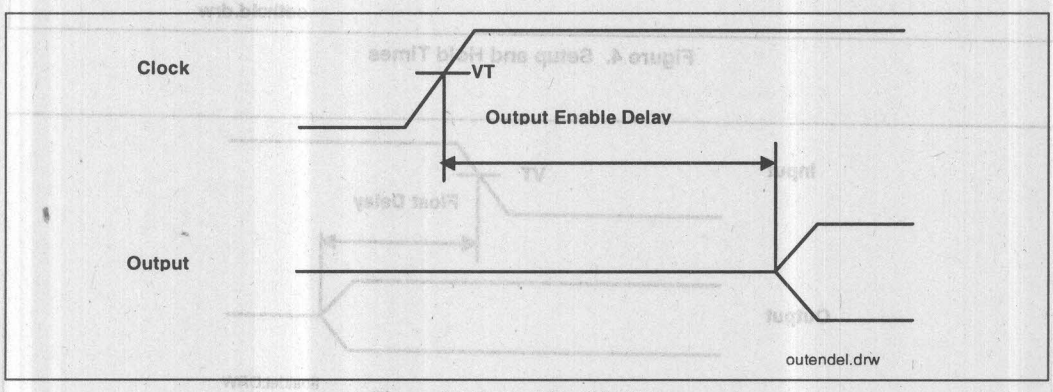


Figure 8. Output Enable Delay

82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4)

- Supported Kits for both Pentium® and Pentium® II Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA and EIO at 1/4 of PCI Frequency
- Supports both Mobile and Desktop Deep Green Environments
  - 3.3V Operation with 5V Tolerant Buffers
  - Ultra-low Power for Mobile Environments Support
  - Power-On Suspend, Suspend to RAM, Suspend to Disk, and Soft-OFF System States
  - All Registers Readable and Restorable for Proper Resume from 0.V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend and Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power Management
- Integrated IDE Controller
  - Independent Timing of up to 4 Drives
  - PIO Mode 4 and Bus Master IDE Transfers up to 14 Mbytes/sec
  - Supports "Ultra DMA/33" Synchronous DMA Mode Transfers up to 33 Mbytes/sec
  - Integrated 16 x 32-bit Buffer for IDE PCI Burst Transfers
  - Supports Glue-less "Swap-Bay" Option with Full Electrical Isolation
- Enhanced DMA Controller
  - Two 82C37 DMA Controllers
  - Supports PCI DMA with 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Interrupt Controller Based on Two 82C59
  - 15 Interrupt Support
  - Independently Programmable for Edge/Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers Based on 82C54
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/sec
  - Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse
  - Supports UHCI Design Guide
- SMBus
  - Host Interface Allows CPU to Communicate Via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock
  - 256-byte Battery-Back CMOS SRAM
  - Includes Date Alarm
  - Two 8-byte Lockout Ranges
- Microsoft Win95* Compliant
- 324 mBGA Package

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The 82371AB PCI ISA IDE Xcelerator (PIIX4) is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. As a PCI-to-ISA bridge, PIIX4 integrates many common I/O functions found in ISA-based PC systems—two 82C37 DMA Controllers, two 82C59 Interrupt Controllers, an 82C54 Timer/Counter, and a Real Time Clock. In addition to compatible transfers, each DMA channel supports Type F transfers. PIIX4 also contains full support for both PC/PCI and Distributed DMA protocols implementing PCI-based DMA. The Interrupt Controller has Edge or Level sensitive programmable inputs and fully supports the use of an external I/O Advanced Programmable Interrupt Controller (APIC) and Serial Interrupts. Chip select decoding is provided for BIOS, Real Time Clock, Keyboard Controller, second external microcontroller, as well as two Programmable Chip Selects. PIIX4 provides full Plug and Play compatibility. PIIX4 can be configured as a Subtractive Decode bridge or as a Positive Decode bridge. This allows the use of a subtractive decode PCI-to-PCI bridge such as the Intel 380FB PCIset which implements a PCI/ISA docking station environment.

PIIX4 supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. Up to four IDE devices can be supported in Bus Master mode. PIIX4 contains support for "Ultra DMA/33" synchronous DMA compatible devices.

PIIX4 contains a Universal Serial Bus (USB) Host Controller that is Universal Host Controller Interface (UHCI) compatible. The Host Controller's root hub has two programmable USB ports.

PIIX4 supports Enhanced Power Management, including full Clock Control, Device Management for up to 14 devices, and Suspend and Resume logic with Power On Suspend, Suspend to RAM or Suspend to Disk. It fully supports Operating System Directed Power Management via the Advanced Configuration and Power Interface (ACPI) specification. PIIX4 integrates both a System Management Bus (SMBus) Host and Slave interface for serial communication with other devices.

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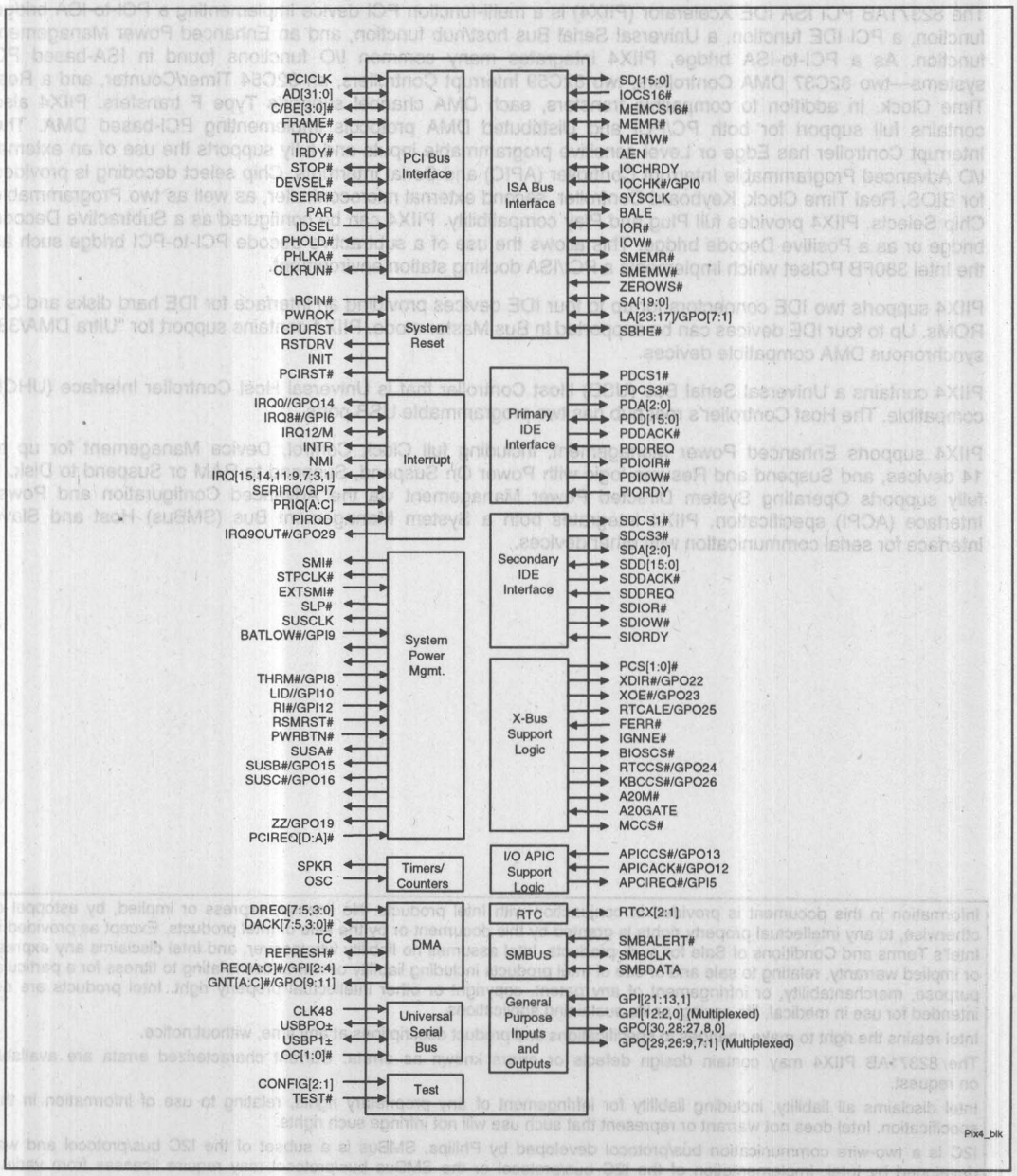
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DATASHEET ADDENDUM

Intel 82371AB PCI ISA IDE Xcelerator (PIIX4)

Timing Specification

273135-001

October, 1997

Intel 82371AB PCI ISA IDE Xcelerator (PIIX4)

Timing Specification

273135-001

October, 1997

82371AB PCI ISA IDE Xcelerator (PIIX4) Features

- Supported Kits for both Pentium® and Pentium® Pro Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA/EIO at 1/4 of PCI Frequency
- Supports Both Mobile and Desktop Deep Green Environments
  - 3.3 V Operation With 5 V Tolerant Buffers
  - Ultra-Low Power for Mobile Environments
  - Power-On Suspend and Soft-OFF for Desktop Environment
  - All Registers Readable/Restorable for Proper Resume From 0 V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend/Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Specification and OS Directed Power Management
- Enhanced DMA Controller
  - Two 82C37 DMA Controllers
  - Supports PCI DMA With 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Integrated IDE Controller
  - Independent Timing of Up to 4 Drives
  - PIO Mode 4 Transfers Up to 14 Mbytes/s
  - Supports "Ultra DMA/33" Synchronous DMA Mode Transfers Up to 33 Mbytes/s
  - Integrated 8 x 32-Bit Buffer for IDE PCI Burst Transfers
  - Supports Glue-Less "Swap-Bay" Option With Full Electrical Isolation
- Interrupt Controller Based on Two 82C59
  - 15 interrupt support
  - Independently Programmable for Edge/Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers based on 82C54
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/s
  - Supports Legacy Keyboard and Mouse Software With USB-Based Keyboard and Mouse
  - Supports UHCI Design Guide Revision 1.1 Interface
- SMBus
  - Host interface Allows CPU to Communicate via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock
  - 256-Byte Battery-Back CMOS SRAM
  - Includes Date Alarm
  - Two 8-Byte Lockout Ranges
- Microsoft* Windows 95* Compliant
- 324 mBGA Package

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 82371AB (PIIX4) PCI ISA IDE Xcelerator. Please refer to the standard package datasheet (order number 290562 for the PIIX4) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

82371AB PCI ISA IDE Xcelerator (PIIX4) Features

- Supported Kits for both Pentium® and Pentium® Pro Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA/EIO at 1/4 of PCI Frequency
- Supports Both Mobile and Desktop Deep Green Environments
  - 3.3 V Operation With 5 V Tolerant Buffers
  - Ultra-Low Power for Mobile Environments
  - Power-On Suspend and Soft-OFF for Desktop Environment
  - All Registers Readable/Restorable for Proper Resume From 0 V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend/Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Specification and OS Directed Power Management
- Enhanced DMA Controller
  - Two 8237 DMA Controllers
  - Supports PCI DMA With 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Integrated IDE Controller
  - Independent Timing of Up to 4 Drives
  - PIO Mode 4 Transfers Up to 14 Mbytes/s
  - Supports "Ultra DMA/33" Synchronous DMA Mode Transfers Up to 33 Mbytes/s
  - Integrated 8 x 32-Bit Buffer for PCI Burst Transfers
  - Supports Glue-Less "Swap-Bay" Option With Full Electrical Isolation
- Interrupt Controller Based on Two 8259
  - 15 Interrupt support
  - Independently Programmable for Edge/Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers based on 8254
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/s
  - Supports Legacy Keyboard and Mouse Software With USB-Based Keyboard and Mouse
  - Supports UHCI Design Guide Revision 1.1 Interface
- SMBus
  - Host Interface Allows CPU to Communicate via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock
  - 256-Byte Battery-Back CMOS SRAM
  - Includes Date Alarm
  - Two 8-Byte Lockout Ranges
- Microsoft® Windows 95® Compliant
- 324 mBGA Package

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 82371AB (PIIX4) PCI ISA IDE Xcelerator. Please refer to the standard package datasheet (order number 290562 for the PIIX4) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

1.0 Introduction

This document contains the electrical and the thermal specifications for the 82371AB (PIIX4). PIIX4 is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus Host/Hub function, and a Power Management function.

The contents of this document are based on simulation and parametric data. This information may be modified as more data is available.

1.1 References

The reader should be familiar with the following documents:

- *82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet
- Universal Serial Bus Specification
- *Universal Host Controller Interface (UHCI) Design Guide*
- System Management Bus Specification
- Serialized IRQ Support for PCI Systems Specification
- Distributed DMA Support for PCI Systems Specification

2.0 Electrical Characteristics

2.1 Absolute Maximum Ratings

Case temperature under bias ..... 0° C to +85° C
Storage temperature ..... -55° C to +150° C
Voltage on any pin with respect to ground ..... -0.3 to V_{CC} +0.3 V
3.3 V supply voltage with respect to V_{SS} ..... -0.3 to +4.6 V
5.0 V supply voltage with respect to V_{SS} (VREF) ..... -0.3 to +5.5 V
Maximum Power Dissipation ..... 1.0 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

The 82371AB PIIX4 (BGA) is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the package are given in Table 1.

Table 1. Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/Watt)	29	24.5
θ_{jc} (°C/Watt)	9.0	

2.2 D.C. Characteristics

Table 2. DC Characteristics (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}(RTC)	Battery Voltage	2.0	3.6	V	
V_{CC}(SUS)	Standby Voltage	3.0	3.6	V	
V_{IL1}	Input Low Voltage	-0.5	0.3 V_{CC}	V	1
V_{IH1}	Input High Voltage	0.5 V_{CC}	V_{CC} + 0.5	V	1
V_{IL2}	Input Low Voltage	-0.3	0.6	V	1
V_{IH2}	Input High Voltage	1.4	V_{CC} + 0.3	V	1
V_{IL3}	Input Low Voltage	-0.5	0.8	V	1
V_{IH3}	Input High Voltage	2.0	VCC5 + 0.5	V	1
V_{OL1}	Output Low Voltage		0.4	V	1
V_{OH1}	Output High Voltage	V_{CC} - 0.5		V	1
V_{OL2}	Output Low Voltage		0.3	V	1, 2
V_{OH2}	Output High Voltage	2.8	3.6	V	1, 2
V_{OL3}	Output Low Voltage		0.5	V	1
V_{OH3}	Output High Voltage	V_{CC} - 0.5		V	1
V_{OL4}	Output Low Voltage		0.45	V	1
V_{OH4}	Output High Voltage	V_{CC} - 0.5		V	1
V_{DI}	Differential Input Sensitivity	0.2		V	I(USBPx+, USBPx-)I
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Includes V_{DI}
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	
I_{OL1}	Output Low Current		4	mA	1, @ V_{OL1}
I_{OH1}	Output High Current	-1		mA	1, @ V_{OH1}
I_{OL2}	Output Low Current		10	mA	1, @ V_{OL4}
I_{OH2}	Output High Current	-3		mA	1, @ V_{OH4}
I_{OL3}	Output Low Current		3	mA	1, @ V_{OL1}
I_{OH3}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL4}	Output Low Current		6	mA	1, @ V_{OL1}
I_{OH4}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL5}	Output Low Current		2	mA	1, @ V_{OL2}

NOTES:

1. Refer to Table 3 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 KΩ to 3.6 V and V_{OH2} assumes R_L of 15 KΩ to GND.

Table 2. DC Characteristics (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
I_{OH5}	Output High Current	-0.25		mA	1, @ V_{OH2}
I_{OL6}	Output Low Current		6	mA	1, @ V_{OL1}
I_{OH6}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL7}	Output Low Current		7	mA	1, @ V_{OL1}
I_{OH7}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL8}	Output Low Current		11	mA	1, @ V_{OL3}
I_{OH8}	Output High Current	-2		mA	1, @ V_{OH3}
I_{LI1}	Input Leakage Current		± 1	µA	
I_{LI2}	Hi-Z State Data Line Leakage	-10	+10	µA	(0 V< V_{IN}< 3.3 V)
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz
C_L	Crystal Load Capacitance	7.5	15	pF	

NOTES:

1. Refer to Table 3 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 KΩ to 3.6 V and V_{OH2} assumes R_L of 15 KΩ to GND.

Table 3. DC Characteristic Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
V_{IL1} / V_{IH1}	**V_{REF}=5.0 V:** (all 3.3 V only inputs except SMBCLK & SMBDATA) PWROK, RSMRST#, RTCX1, TEST, BATLOW#, CONFIG[1:2], EXTSMI#, GPI[1], IRQ8#, LID, RI#, SMBALERT#, PWRBTN#, USBP[1:0]+, USBP[1:0]-, FERR# **V_{REF}=3.3 V:** (all inputs except SMBCLK & SMBDATA) PWROK, RSMRST#, RTCX1, TEST, BATLOW#, CONFIG[1:2], EXTSMI#, GPI[1], IRQ8#, LID, RI#, SMBALERT#, PWRBTN#, USBP[1:0]+, USBP[1:0]-, FERR#, AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IDSEL, IRDY#, PHLDA#, SERR#, STOP#, TRDY#, IOCHK#, IOCHRDY, IOCS16#, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, SA[19:0], SBHE#, SD[15:0], ZEROWS#, A20GATE, RCIN#, DREQ[0:3, 5:7], REQ[A:C]#, APICREQ#, IRQ[1, 3:7, 9:12, 14:15], PIRQ[A:D], SERIRQ, CLK48, PCICLK, OSC, PDD[15:0], PDDREQ, PIORDY, SDD[15:0], SDDREQ, SIORDY, OC[1:0]#, PCIREQ[A:D],THRM#
V_{IL2} / V_{IH2}	SMBCLK, SMBDATA
V_{IL3} / V_{IH3}	**V_{REF}=5.0 V:** (all 5 V tolerant inputs) AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IDSEL, IRDY#, PHLDA#, SERR#, STOP#, TRDY#, IOCHK#, IOCHRDY, IOCS16#, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, SA[19:0], SBHE#, SD[15:0], ZEROWS#, A20GATE, RCIN#, DREQ[0:3, 5:7], REQ[A:C]#, APICREQ#, IRQ[1, 3:7, 9:12, 14:15], PIRQ[A:D], SERIRQ, CLK48, PCICLK, OSC, PDD[15:0], PDDREQ, PIORDY, SDD[15:0], SDDREQ, SIORDY, OC[1:0]#, PCIREQ[A:D],THRM#
V_{OL1} / V_{OH1}	PDA[2:0], PDCS1#, PDCS3#, PDD[15:0], PDDACK#, PDIOR#, PDIOW#, SDA[2:0], SDCS1#, SDCS3#, SDD[15:0], SDDACK#, SDIOR#, SDIOW#, CPU_STP#, EXTSMI#, ZZ, GPO8, PCI_STP#, SMBCLK, SMBDATA, SUS[A:C]#, SUS_STAT[1:2]#, A20M#, CPURST, IGNNE#, INIT, INTR, NMI, SMI#, STPCLK#, BIOSCS#, KBCCS#, MCCS#, PCS0#, PCS1#, RTCALE, RTCCS#, XDIR#, XOE#, SUSCLK, RTCX2, SMBCLK, SMBDATA, APICACK#, APICCS#, IRQ[0, 8], SPKR, GNT[A:C], GPO[0, 8, 27, 28, 30], IRQ9OUT#, AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IRDY#, PAR, PCIRST#, PHOLD#, SERR#, STOP#, TRDY#, SERIRQ
V_{OL2} / V_{OH2}	USBP[1:0]+, USBP[1:0]-
V_{OL3} / V_{OH3}	SLP#
V_{OL4} / V_{OH4}	**ISA/EIO Output Signals:** AEN, BALE, IOCHRDY, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, RSTDRV, SA[19:0], SBHE#, SD[15:0], SMEMR#, SMEMW#, SYSCLK, DACK[0:3, 5:7]#, TC
I_{OL1} / I_{OH1}	**IDE Output Signals:** PDA[2:0], PDCS1#, PDCS3#, PDD[15:0], PDDACK#, PDIOR#, PDIOW#, SDA[2:0], SDCS1#, SDCS3#, SDD[15:0], SDDACK#, SDIOR#, SDIOW#
I_{OL2} / I_{OH2}	**ISA/EIO Output Signals:** AEN, BALE, IOCHRDY, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, RSTDRV, SA[19:0], SBHE#, SD[15:0], SMEMR#, SMEMW#, SYSCLK, DACK[0:3, 5:7]#, TC

Table 3. DC Characteristic Signal Association (Sheet 2 of 2)

Symbol	Associated Signals
I_{OL3} / I_{OH3}	**Power Management Signals:** CPU_STP#, EXTSMI#, ZZ, GPO8, PCI_STP#, SMBCLK, SMBDATA, SUS[A:C]#, SUS_STAT[1:2]# **CPU Interface Signals:** A20M#, CPURST, IGNNE#, INTR, NMI **X-Bus Interface Signals:** BIOSCS#, KBCCS#, MCCS#, PCS0#, PCS1#, RTCALE, RTCCS#, XDIR#, XOE#, SUSCLK, RTCX2 **Other Signals:** SMBCLK, SMBDATA, APICACK#, APICCS#, IRQ[0, 8], SPKR, GNT[A:C], GPO[0, 8, 27, 28, 30], IRQ9OUT#
I_{OL4} / I_{OH4}	**PCI Bus Signals:** AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IRDY#, PAR, PCIRST#, PHOLD#, SERR#, STOP#, TRDY#, SERIRQ
I_{OL5} / I_{OH5}	**USB Signals:** USBP[1:0]+, USBP[1:0]-
I_{OL6} / I_{OH6}	SMI#, STPCLK#
I_{OL7} / I_{OH7}	INIT#
I_{OL8} / I_{OH8}	SLP#

Table 4. DC Current Characteristics

Functional Operating Range (V_{REF} = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Typ	Max	Unit	Notes
I_{CC}(3 V)	V_{CC} Supply Current	110	155	mA	
I_{CC}(SUS) ON	Suspend Well Supply Current - Full On	3	5	mA	
I_{CC}(SUS) POS/STR	Suspend Well Supply Current - Power On Suspend or Suspend to RAM	30	150	µA	
I_{CC}(SUS) STD/Soff	Suspend Well Supply Current - Suspend to Disk or Soft Off	9	150	µA	
I_{CC}(RTC)	Battery Standby Current	6	8	µA	V_{CC}(RTC) = 3.0 V Mech Off State

2.3 A.C. Characteristics

Table 5. CLOCK/RESET TIMINGS (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figures
PCI Clock Timings						
PCICLK						
t1a	Period	30	33.3	ns		2
t1b	High Time	12.0		ns		2
t1c	Low Time	12.0		ns		2
t1c	Rise Time		3.0	ns		2
t1d	Fall Time		3.0	ns		2
ISA Clock Timings						
SYSCLK						
t1f	Period	120	133.3	ns		2
t1g	High Time	49		ns		2
t1h	Low time	49		ns		2
t1i	RiseTime		4	ns		2
t1j	Fall time		4	ns		2
Oscillator Clock Timings						
OSC						
t1l	OSC Period	67	70	ns		2
t1m	High Time	20				2
t1n	Low time	20		ns		2
USB Clock Timings						
f_{clk48}	Operating Frequency	48		MHz		
t1p	Frequency Tolerance		±2500	ppm	1	2
t1q	High Time	7		ns		2
t1r	Low time	7		ns		2
t1s	Rise Time		1.2	ns		2
t1t	Fall Time		1.2	ns		2
Suspend Clock Timings						

NOTES:

1. The USBCLK is a 48 MHz clock; it expects a 40/60% duty cycle.
2. The maximum high time (t2b Max) provides a simple guaranteed method for devices to detect bus idle conditions.
3. t2j is measured as a transition time through the threshold region V_{ol}=0.8 V and V_{oh}=2.0 V.

Table 5. CLOCK/RESET TIMINGS (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figures
f_{susclk}	SUSCLK Operating Frequency	32		KHz		
t1v	High time	10		µs		
t1w	Low Time	10		µs		
SMBus Clock						
f_{smb}	SMCLK Operating Frequency	10	16	KHz		
t2b	High time	4.0	50	µs	2	40
t2c	Low time	4.7		µs		40
t2d	Clock/Data Rise time		1000	ns		40
t2e	Clock /Data Fall time		300	ns		40
RESET TIMINGS						
t2f	PCIRST#, RSTDRV Driven Inactive After SUS_STATx# is Driven Inactive.		1	RTCCLK		3
t2g	CPURST, PCIRST#, RSTDRV Active Pulse Width. Initiated via the RC Register.	1		ms		4
t2h	CPURST Driven Inactive After PCIRST# is Driven Inactive.		1	RTCCLK		3
t2i	CPURST Valid Delay from PCICLK Rising	2	25	ns		29
t2j	PWROK, RSMRST# Rise time		10	ns	3	
SMI#						
t3a	Valid Delay from PCICLK	2	25	ns		7
t3b	Active Pulse Width	3		PCICLK		5
t3c	Inactive Pulse Width	4		PCICLK		5
EXTSMI#						
t3d	Active Pulse Width	2		PCICLK		5
t3e	Inactive Pulse Width	4		PCICLK		5
t3f	Valid Setup to PCICLK	10		ns		6
t3g	Valid Hold from PCICLK	4		ns		6
STPCLK#						
t3h	Valid Delay from PCICLK	2	25	ns		7
t3i	STPCLK# Inactive Pulse Width	5		PCICLK		5

NOTES:

1. The USBCLK is a 48 MHz clock; it expects a 40/60% duty cycle.
2. The maximum high time (t2b Max) provides a simple guaranteed method for devices to detect bus idle conditions.
3. t2j is measured as a transition time through the threshold region V_{ol}=0.8 V and V_{oh}=2.0 V.

Table 6. PIIX4 as Master Timings (Sheet 1 of 3)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
BALE								
t4a	BALE Pulse Width	50		ns	M,I/O	8,16		8,9,10, 11
t4b	BALE Driven Active from MEMx#, Iox# Inactive	44		ns	M,I/O	8,16		8,9,10, 11
LA[23:17]								
t5a	LA[23:17] Valid Setup to BALE Inactive	150		ns	M	8,16	1	8,9
t5b	LA[23:17] Valid Hold from BALE Inactive	26		ns	M	8,16		8,9
t5c	LA[23:17] Valid Setup to MEMx# Active	150		ns	M	16		9
t5d	LA[23:17] Valid Setup to MEMx# Active	173		ns	M	8		8
t5e	LA[23:17] Invalid from MEMx# Active	39		ns	M	16		9
t5f	LA[23:17] Invalid from MEMx# Active	39		ns	M	8		8
SA[19:0], SBHE#								
t6a	SA[19:0], SBHE# Valid Setup to MEMx# Active	34		ns	M	16	2,3	9
t6b	SA[19:0], SBHE# Valid Setup to Iox# Active	100		ns	I/O	16		11
t6c	SA[19:0], SBHE# Setup to MEMx#, Iox# Active	100		ns	M,I/O	8		8, 10
t6d	SA[19:0], SBHE# Valid Setup to BALE Inactive	37		ns	M,I/O	8,16	2,3	8,9,10, 11
t6e	SA[19:0], SBHE# Valid Hold from MEMx#, Iox# Inactive	41		ns	M,I/O	8,16		8,9,10, 11
MEMR#, MEMW#, IOR# and IOW#								
t7a	MEMx# Active Pulse Width (std)	225		ns	M	16		9
t7b	Iox# Active Pulse Width (std)	160		ns	I/O	16		11
t7c	MEMx# Active Pulse Width (nws)	105		ns	M	16	4	9
t7d	MEMx# or Iox# Active Pulse Width (std)	520		ns	M,I/O	8		8,10
t7e	MEMx# or Iox# Active Pulse Width (nws)	160		ns	M,I/O	8	4	8,10
t7f	MEMx# Inactive Pulse Width	103		ns	M	16		9
t7g	MEMx# Inactive Pulse Width	163		ns	M	8		8
t7h	Iox# Inactive Pulse Width	163		ns	I/O	8,16		10,11

NOTES:

1. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
2. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices should not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
3. For back-to-back "sub cycles" generated as a result of byte assembly or disassembly, this specification is 34 ns.
4. No-wait-state (ZEROWS#) asserted.

Table 6. PIIX4 as Master Timings (Sheet 2 of 3)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
t7i	MEMx#, Iox# Driven Inactive from IOCHRDY Active	120		ns	M,I/O	8,16		8,9,10, 11
SMEMR# and SMEMW#								
t8a	SMEMR# & SMEMW# Propagation Delay from MEMR# and MEMW#		16	ns	M	8,16		8,9
Read Data								
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O	8,16		8,9,10, 11
t9b	Read Data Valid Setup to MEMR#, IOR#	24		ns	M,I/O	8,16		8,9,10, 11
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		8,9,10, 11
t9d	Read Data three stated from MEMR# and IOR# Inactive		41	ns	M,I/O	8,16		8,9,10, 11
Write Data								
t10a	Write Data Valid Setup to MEMW# Active	-40		ns	M,I/O	8,16		8,9,10, 11
	Write Data Valid Setup to IOW# Active	-40		ns	M,I/O	8		
	Write Data Valid Setup to IOW# Active	+23		ns	M,I/O	16		
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O	8,16		8,9,10, 11
t10c	Write Data three stated from MEMW#, IOW# Inactive		105	ns	M,I/O	8,16		8,9,10, 11
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O	8,16		8,9,10, 11
MEMCS16#								
t11a	MEMCS16# Driven Active from LA[23:17] Valid		94	ns	M	16		9
t11b	MEMCS16# Inactive from LA[23:17] Valid		91	ns	M	8		8
t11c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		9
t11d	MEMCS16# Driven Active from SA[19:2] Valid		35	ns	M	16		9
IOCS16#								
t12a	IOCS16# Driven Active from Valid SA[19:0]		123	ns	I/O	16		11
t12b	IOCS16# Inactive from Valid SA[19:0]		91	ns	I/O	8		10

NOTES:

1. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
2. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices should not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
3. For back-to-back "sub cycles" generated as a result of byte assembly or disassembly, this specification is 34 ns.
4. No-wait-state (ZEROWS#) asserted.

Table 6. PIIX4 as Master Timings (Sheet 3 of 3)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
t12c	IOCS16# Valid Hold from SA[19:0] Invalid	0		ns	I/O	16		11
t12d	IOCS16# Driven Active from Iox Active		80	ns	I/O	16		11
ZEROWS#								
t13a	ZEROWS# Driven Active from MEMx# Active		16	ns	M	16		9
t13b	ZEROWS# Driven Active from MEMx#, Iox# Active		80	ns	M,I/O	8		8, 10
t13c	ZEROWS# Driven Active from LA[23:17] Valid		180	ns	M	16		9
t13d	ZEROWS# Driven Active from LA[23:17] Valid		300	ns	M	8		8
ZEROWS#								
t13e	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		80	ns	M	16		9
t13f	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		200	ns	M,I/O	8		8,10
AEN								
t14a	AEN Valid Setup to Iox# Driven Active	111		ns	I/O	8,16		10,11
t14b	AEN Valid Setup to BALE Driven Inactive	111		ns	I/O	8,16		10,11
t14c	AEN Valid Hold from Iox# Driven Inactive	41		ns	I/O	8,16		10,11
IOCHRDY								
t15a	IOCHRDY Driven Valid from MEMx#, Iox# Active		78	ns	M,I/O	16		9,11
t15b	IOCHRDY Driven Valid from MEMx#, Iox# Active		366	ns	M,I/O	8		8,10
t15e	IOCHRDY Inactive Pulse Width	0.12	15.6	µs	M,I/O	8,16		8,9,10, 11

NOTES:

1. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
2. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices should not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
3. For back-to-back "sub cycles" generated as a result of byte assembly or disassembly, this specification is 34 ns.
4. No-wait-state (ZEROWS#) asserted.

Table 7. PIIX4 as Slave Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
LA[23:17]								
t16a	LA[23:17] Valid Setup to MEMx# Active	23		ns	M	16		12
SA[19:0],SBHE#								
t17a	SA[19:0],SBHE# Setup to MEMx# Active	23		ns	M	16		12
t17b	SA[19:0],SBHE# Setup to Iox# Active	89		ns	I/O	8		13
t17c	SA[19:0],SBHE# Valid Hold from MEMx#, Iox# Inactive	30		ns	M,I/O	8,16		12,13
MEMR#, MEMW#, IOR#, IOW#								
t18a	MEMx# Active Pulse Width	214		ns	M	16		12
t18b	Iox# Active Pulse Width	509		ns	I/O	8		13
t18c	MEMx# Inactive Pulse Width	92		ns	M	16		12
t18d	Iox# Inactive Pulse Width	152		ns	I/O	8		13
Read Data								
t19a	Read Data Valid from IOCHRDY Active		69	ns	M,I/O	8,16		12,13
t19b	Read Data Valid from IOR# Active		69	ns	I/O	8	1	13
t19c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		12,13
t19d	Read Data Three State from MEMR#, IOR# Inactive		55	ns	M,I/O	8,16		12,13
Write Data								
t20a	Write Data Valid Setup to MEMW#, IOW# Active	-54		ns	M,I/O	8,16		12,13
t20b	Write Data Valid Hold from MEMW#, IOW# Inactive	14		ns	M,I/O	8,16		12,13
MEMCS16#								
t21a	MEMCS16# Driven Active from Valid LA[23:17]		65	ns	M	16		12
t21b	MEMCS16# Float from Valid LA[23:17]		31	ns	M	16		12
t21c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		12
IOCHRDY								
t22a	IOCHRDY Inactive from MEMx#, Iox# Active		50	ns	M,I/O	8,16		12,13
t22b	IOCHRDY Float from IOCHRDY Rising		85	ns	M,I/O	8,16	2	12,13
t22c	IOCHRDY Inactive Pulse Width	0.12	2.5	µs	M,I/O	8,16		12,13

NOTES:

1. This applies to the PIIX4 cycles that IOCHRDY is not driven low.
2. This specification includes both the time the PIIX4 drives IOCHRDY active and the time it takes the PIIX4 to float IOCHRDY.

Table 8. Interrupt and NMI Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Figure
NMI Timing					
t23a	SERR#, IOCHK# Active to NMI Driven Active		200	ns	14
Interrupt Timing					
t24a	IRQx Inactive Pulse Width	100		ns	15

Table 9. ISA Bus Master Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
DACK#						
t26a	DACK#, Inactive from DREQ Inactive	240		ns		16
Three Stating and Driving the Bus						
t27a	PIIX4 Three States Address, Data, and Control Signals from DACK#, Active		30	ns		16
t27b	PIIX4 Drives Address, Data, and Control Signals from DACK#, Inactive	71		ns		16
SMEMR# and SMEMW#						
t28a	SMEMR# and SMEMW# Active (falling edge) from MEMR# and MEMW# Active (falling edge)		25	ns		16
t28b	SMEMR# and SMEMW# Inactive (rising edge) from MEMR# and MEMW# Inactive (rising edge)		35	ns		16
Data Swap Logic Timing (ISA Master to ISA slave)						
t29a	SD[7:0] to SD[15:8] Propagation Delay		26	ns		17
t29b	SD[15:8] to SD[7:0] Propagation Delay		26	ns		17
t29c	PIIX4 Drives Data Bus from IOR#, IOW#, MEMR# or MEMW# Active		26	ns	1	17
t29d	PIIX4 Three States Bus from IOR#, MEMR#, or SMEMR# Inactive	2	55	ns	1,2	17
t29e	PIIX4 Three States Bus from IOW#, MEMW#, or SMEMW# Inactive	2	60	ns	1,2	17

NOTES:

1. This applies to the byte lane that the data has been swapped to.
2. Data is three stated from the standard memory commands (SMEMR# or SMEMW#), when they are generated.

Table 10. DMA Compatible Timings (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
DREQ						
t30a	DREQ Active Hold from IOR# Active		558	ns	1	19
t30b	DREQ Active Hold from IOW# Active		315	ns	1	18
DACK#						
t31a	DACK# Active to IOR# Active	73		ns		19
t31b	DACK# Active to IOW# Active	312		ns		18
t31c	DACK# Active Hold from IOR# Inactive	100		ns		19
t31d	DACK# Active Hold from IOW# Inactive	155		ns		18
AEN and BALE						
t32a	AEN Active to Iox# Active	111		ns		18,19
t32b	AEN and BALE Inactive from Iox# Inactive	41		ns		18,19
LA[23:19], SA[19:0], SBHE#						
t33a	LA[23:19],SA[19:0], SBHE# Valid Setup to MEMx# Active	99		ns		18,19
t33b	LA[23:19],SA[19:0], SBHE# Valid Hold from MEMx# Inactive	51		ns		18,19
MEMR#, MEMW#, IOR#, IOW#						
t34a	IOW# and MEMW# Active Pulse Width	465		ns		18,19
t34b	MEMR# Active Pulse Width	495		ns		18
t34c	IOR# Active Pulse Width	760		ns		19
t34d	IOW# Inactive Pulse Width (continuous)	465		ns		18
t34e	IOR# Inactive Pulse Width (continuous)	160		ns		19
t34f	IOR# Active to MEMW# Active	230		ns		19
t34g	MEMR# Active to IOW# Active	-26		ns		18
t34h	MEMR# Active Hold from IOW# Inactive	40		ns		18
t34i	IOR# Active Hold from MEMW# Inactive	40		ns		19
t34j	MEMx# Active Hold from IOCHRDY Active	120		ns		18,19
SMEMR# & SMEMW#						
t35a	SMEMR# & SMEMW# Valid from MEMR# and MEMW# Valid		15	ns		18,19
Read Data						
t36a	Read Data Valid from IOR# Active		237	ns		19
t36b	Read Data Valid Hold from IOR# Inactive	0		ns		19
t36c	Read Data Float from IOR# Inactive		61	ns		19
Write Data						

NOTES:

1. This applies to the last cycle of a demand mode DMA transfer.
2. This applies to the byte lane that the data has been swapped to.
3. Output from PIIX4.

Table 10. DMA Compatible Timings (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
t37a	Write Data Valid Setup to IOW# Inactive	225		ns		18
t37b	Write Data Valid Hold from IOW# Inactive	36		ns		18
Data Swap Logic Timing (ISA to ISA Transaction)						
t38a	SD[7:0] to SD[15:8] Propagation Delay		26	ns		20
t38b	SD[15:8] to SD[7:0] Propagation Delay		26	ns		20
t38c	PIIX4 Drives Data Bus from IOR# or MEMR# Active		26	ns	2	20
t38d	PIIX4 Three States Bus from IOR# or MEMR# Inactive		55	ns	2	20
TC						
t39a	TC Active Setup to Iox# Inactive	511		ns	3	18,19
t39b	TC Active Hold from Iox# Inactive	71		ns	3	18,19
t39h	TC Pulse Width	700		ns		18,19
IOCHRDY						
t40b	IOCHRDY Valid from MEMx# Active		315	ns		18,19
t40c	IOCHRDY Inactive Pulse Width	125		ns		18,19

NOTES:

1. This applies to the last cycle of a demand mode DMA transfer.
2. This applies to the byte lane that the data has been swapped to.
3. Output from PIIX4.

Table 11. DMA Type "F" Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
DREQ						
t55a	DREQ Active Hold from IOR# Active		82	ns	1, 2	21
t55b	DREQ Active Hold from IOW# Active		82	ns	1, 2	21
DACK#						
t56a	DACK# Active to IOR# Active	77		ns	2	21
t56b	DACK# Active to IOW# Active	77		ns	2	21
t56c	DACK# Active Hold from IOR# Inactive	30		ns	2	21
t56d	DACK# Active Hold from IOW# Inactive	30		ns	2	21
AEN and BALE						
t57a	AEN Active to Iox# Active	111		ns		21
t57b	AEN and BALE Inactive from Iox# Inactive	41		ns		21
IOR# and IOW#						
t58a	IOR# Active Pulse Width	110		ns		21
t58b	IOW# Active Pulse Width	110		ns		21
t58c	IOR# Inactive Pulse Width (Continuous)	115		ns		21
t58d	IOW# Inactive Pulse Width (Continuous)	115		ns		21
Read Data						
t59a	Read Data Valid from IOR# Active		96	ns		21
t59b	Read Data Valid Hold from IOR# Inactive	2		ns		21
t59c	Read Data Float from IOR# Inactive		61	ns		21
Write Data						
t60a	Write Data Valid Setup to IOW# Inactive	70		ns		21
t60b	Write Data Valid Hold from IOW# Inactive	31		ns		21
TC						
t61a	TC Active Setup to IOR# Inactive	40		ns	3	21
t61b	TC Active Setup to IOW# Inactive	40		ns	3	21
t61c	TC Active Hold from Iox# Inactive	0		ns	3	21

NOTES:

1. This applies to the last cycle of a demand mode DMA transfer.
2. Type F transfers are selected via the MBDMAX Register.
3. Output from PIIX4.

Table 12. ISA Refresh Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
REFRESH#						
t62a	REFRESH# Active Setup to MEMR# Active	120		ns		22,23
t62b	REFRESH# Active Hold from MEMR# Inactive	31	260	ns		22,23
t62c	REFRESH# Driven Active to SA[15:0] Valid	11		ns		22,23
t62d	REFRESH# Active Hold from SA[15:0] Invalid	11		ns		22,23
AEN						
t63a	AEN Driven Active to MEMR# Active	11		ns		22,23
t63b	AEN Hold from MEMR# Inactive	11		ns		22,23
SA[15:0]						
t64a	SA[15:0] Valid Setup to MEMR# Active	72		ns		22,23
t64b	SA[15:0] Valid Hold from MEMR# Inactive	35		ns		22,23
t64c	SA[15:0] Valid Float from MEMR# Inactive	46	120	ns	1	23
MEMR#, SMEMR#						
t65a	MEMR# Active Pulse Width	225		ns		22,23
t65b	MEMR# Three state from MEMR# Inactive	36	120	ns		22,23
t65c	MEMR# Driven Inactive from IOCHRDY Active	120		ns		22,23
t65d	SMEMR# Propagation Delay from MEMR#		25	ns		22,23
IOCHRDY						
t66a	IOCHRDY Inactive from MEMR# Active		76	ns		22,23
t66b	IOCHRDY Valid from MEMR# Active		76	ns		22,23
t66c	IOCHRDY Inactive Pulse Width	120		ns		22,23
PIIX4 Driving Bus From REFRESH#						
t67a	PIIX4 Drives Control and Address from REFRESH# Active	5		ns	1	23

NOTE:

1. This applies to ISA Master initiated refresh only.

Table 13. PIIX4 and ISA Master Accesses to the X-Bus

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
BIOSCS#, KBCCS#, RTCCS#, AND PCS0#, PCS1#, MCCS#						
t68a	CS# Driven Active from SA[19:0], LA[23:17] Valid (except BIOSCS#)		35	ns		24
t68b	CS# Driven Inactive from SA[16:0], LA[23:17] Invalid (except BIOSCS#)		35	ns		24
XDIR# and XOE#						
t69a	XDIR# Active from IOR#, MEMR# Active					24
	- PCI-Initiated Access		25	ns		
	- ISA-Initiated Access		30	ns		
t69b	BIOSCS#, XOE# Active from Iox#, MEMx# Active		29	ns		24
t69c	XDIR# Active Setup to XOE# Active	2	12	ns		24
t69d	BIOSCS#, XOE# Inactive from Iox#, MEMx# Inactive	35	60	ns	1	24
t69f	BIOSCS#, XOE# Setup to XDIR# Inactive	2	15	ns	1	24
t69g	XOE# Inactive from IOR#, MEMR# Inactive	2	140	ns	2	24
t69i	XOE# Inactive Setup to XDIR# Inactive	2	12	ns	2	24

NOTES:
1. PIIX4 as a master cycles only.
2. ISA master cycles only.

Table 14. Miscellaneous X-Bus Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
Mouse Timing Support						
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns		25
Coprocessor Error Support						
t73a	IGNNE# Active from IOW# Active from Port F0H Access		220	ns		25
t73b	IGNNE# Inactive from FERR# Inactive		230	ns		25
Real Time Clock Timing (RTCALE)						
t75a	RTCALE Pulse Width	200	300	ns		26
t75b	RTCALE Active from IOW# Active					26
	- PCI-Initiated Access		85	ns		
	- ISA-Initiated Access		156	ns		
Speaker Timing						
t76a	SPKR Valid Delay from OSC Rising		200	ns		27

Table 15. PCI Interface Timing

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
t77	AD[31:0] Valid Delay	2	11	ns	Min: 0 pF Max: 50 pF	29
t78	AD[31:0] Setup Time	7		ns		30
t79	AD[31:0] Hold Time	0		ns		30
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# CLOCKRUN#, GNT[A:C]# Valid Delay from PCICLK Rising	2	11	ns	Min: 0 pF Max: 50 pF	29
t81	C/Bes[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# CLOCKRUN#, GNT[A:C]# Output Enable Delay from PCICLK Rising	2		ns		33
t82	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# CLOCKRUN#, Float Delay from PCICLK Rising	2	28	ns		31
t83	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# CLOCKRUN#, REQ[A:C]# Setup Time to PCICLK Rising	7		ns		30
t84	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# CLOCKRUN#, REQ[A:C]#, Hold Time from PCLKIN Rising	0		ns		30
t85	PHLD# Valid Delay from PCICLK Rising	2	12	ns	0 pF	29
t86	PHLDA# Setup Time to PCICLK Rising	10		ns		30
t87	PHLDA# Hold Time from PCICLK Rising	0		ns		30
t91	PIRQ[D:A]# Setup Time to PCICLK Rising				1	30
t92	PIRQ[D:A]# Hold Time From PCICLK Rising				1	30
t96	RST# Low Pulse Width	1		ms		32

NOTE:

1. This signal is internally synchronized.

t106	PDA[2:0] Valid Delay From PCICLK Rising	2	30	ns		34
t107	PDCS1#, PDCS3# Active From PCICLK Rising	2	30	ns		34
t108	PDCS1#, PDCS3# Inactive From PCICLK Rising	2	30	ns		
t113	PDDACK# Active From PCICLK Rising	2	20	ns		35
t114	PDDACK# Inactive From PCICLK Rising	2	20	ns		
t114a	PDDREQ Setup Time to PCICLK Rising	7		ns		35
t114b	PDDREQ Hold From PCICLK Rising	7		ns		35
t115	PDD[15:0] Valid Delay From PCICLK Rising	2	30	ns		34,35
t115a	PDD[15:0] Setup Time to PCICLK Rising	10		ns		34,35
t115b	PDD[15:0] Hold From PCICLK Rising	8		ns		34,35
t116	PIORDY Setup Time to PCICLK Rising	7		ns	1	34
t117	PIORDY Hold From PCICLK Rising	7		ns	1	34
t117a	PIORDY Inactive Pulse Width	48		ns		34
t118	PIORDY Sample Point From DIOx# Assertion			PCICLK	2, 3	34
t119	PDIOx# Active Pulse Width			PCICLK	2, 3	34,35
t120	PDIOx# Inactive Pulse Width			PCICLK	3, 4	34,35
Secondary IDE Timing						
t102	SDIOW# Active From PCICLK Rising	2	20	ns		35
t103	SDIOW# Inactive From PCICLK Rising	2	20	ns		34,35
t104	SDIOR# Active From PCICLK Rising	2	20	ns		35
t105	SDIOR# Inactive From PCICLK Rising	2	20	ns		34,35
t106	SDA[2:0] Valid Delay From PCICLK Rising	2	30	ns		34

NOTES:

1. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
2. This parameter is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register.
3. The cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. This parameter is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 16. PCI Bus IDE Timing (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

t107	SDCS1#, PDCS3# Active From PCICLK Rising	2	30	ns		34
t108	SDCS1#, PDCS3# Inactive From PCICLK Rising	2	30	ns		
t113	SDDACK# Active From PCICLK Rising	2	20	ns		35
t114	SDDACK# Inactive From PCICLK Rising	2	20	ns		
t114a	SDDREQ Setup Time to PCICLK Rising	7		ns		35
t114b	SDDREQ Hold From PCICLK Rising	7		ns		35
t115	SDD[15:0] Valid Delay From PCICLK Rising	2	30	ns		34,35
t115a	SDD[15:0] Setup Time to PCICLK Rising	10		ns		34,35
t115b	SDD[15:0] Hold From PCICLK Rising	8		ns		34,35
t116	SIORDY Setup Time to PCICLK Rising	7		ns	1	34
t117	SIORDY Hold From PCICLK Rising	7		ns	1	34
t117a	PIORDY Inactive Pulse Width	48		ns		34
t118	SIORDY Sample Point From DIOx# Assertion			PCICLK	2, 3	34
t119	SDIOx# Active Pulse Width			PCICLK	2, 3	34,35
t120	SDIOx# Inactive Pulse Width			PCICLK	3, 4	34,35

NOTES:

1. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
2. This parameter is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register.
3. The cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. This parameter is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 17. Universal Serial Bus Timings (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
Full Speed Source (Note 7)						
t122	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	36
t123	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	36
t124	Source Differential Driver Jitter				2, 3	37
	- To Next Transition	-2	2	ns		
	- For Paired Transitions	-1	1	ns		
t125	Source EOP Width	160	175	ns	4	38
t126	Differential to SE0 Transition Skew	-2	5	ns	5	
t127	Receiver Data Jitter Tolerance				3	37
	- To Next Transition	-20	20	ns		
	- For Paired Transitions	-10	10	ns		
t128	EOP Width				4	38
	- Must reject as EOP	40		ns		
	- Must accept as EOP	85		ns		
t126	Differential to SE0 Transition Skew	-2	5	ns	5	
Low Speed Source (Note 8)						
t127	USBPx+, USBPx- Driver Rise Time	75		ns	1, 6 = 50 pF	36
			300	ns	C_L = 350 pF	
t128	USBPx+, USBPx- Driver Fall Time	75		ns	1, 6	36
			300	ns	C_L = 50 pF C_L = 350 pF	
t129	Source Differential Driver Jitter				2, 3	37
	- To Next Transition	-2	2	ns		
	- For Paired Transitions	-1	1	ns		

NOTES:

1. Driver output resistance under steady state drive is specified at 28 ohms at minimum and 43 ohms at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

	- For Paired Transitions	-10	10	ns		
t133	EOP Width			4		38
	- Must reject as EOP	40		ns		
	- Must accept as EOP	85		ns		
t134	Differential to SE0 Transition Skew	-2	5	ns	5	

NOTES:

1. Driver output resistance under steady state drive is specified at 28 ohms at minimum and 43 ohms at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

Table 18. IOAPIC Bus Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t136	APICCS# Setup to MEMx#	2		PCICLK	1	39
t137	SA[19:0] Setup to APICCS#	2		PCICLK	1	39
t138	APICACK# Valid Delay from PCICLK	2.0	12.0	ns		29
t139	APICREQ# Valid Setup to PCICLK	10.0		ns		30
t140	APICREQ# Valid Hold from PCICLK	0.0		ns		30

NOTE:

1. With these exceptions, the APIC configuration cycles conform to the 8-bit ISA Memory Slave Timing where PIIX4 is the master.

Table 19. SMBUS Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t141	Bus free time between Stop and Start Condition	4.7		µs		40
t142	Hold time after (repeated) Start Condition. After this period, the first clock is generated	4.0		µs		40
t143	Repeated Start Condition setup time	4.7		µs		40
t144	Stop Condition setup time	4.0		µs		40
t145	Data hold time	300		ns		40
t146	Data setup time	250		ns		40
t147	Device time out	25	35	ms	1	
t148	Cumulative clock low extend time (slave device)		25	ms	2	41
t149	Cumulative clock low extend time (master device)		10	ms	3	41

NOTES:

1. A device will timeout when any clock low exceeds this value.
2. t148 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t149 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-acknowledge, acknowledge-to-acknowledge, or acknowledge-to-stop.

Table 20. Serial IRQ Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t151	SERIRQ Setup Time to PCICLK Rising	7		ns		30
t152	SERIRQ Hold Time from PCICLK Rising	0		ns		30

Table 21. ULTRADMA/33 Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

		Mode 0 (ns)		Mode 1 (ns)		Mode 2 (ns)		
Sym	Parameter (Note 1)	Min	Max	Min	Max	Min	Max	Figure
t154	Cycle Time (Tcyc) (Note 2)	114		75		55		43
t155	Two Cycle Time (T2cyc)	235		156		117		43
t156	Data Setup Time (Tds)	15		10		7		43
t157	Data Hold Time (Tdh)	5		5		5		43
t158	Data Valid Setup Time (Tdvs)	70		48		34		43
t159	Data Valid Hold Time (Tdvh)	6		6		6		43
t160	Limited Interlock Time (Tli)	0	150	0	150	0	150	45
t161	Interlock Time w/ Minimum (Tmli)	20		20		20		45
t162	Envelope Time (Tenv)	20	70	20	70	20	70	42
t163	Ready to pause Time (Trp)	160		125		100		44
t164	DMACK setup/hold Time (Tack)	20		20		20		42,45

NOTES:

1. The specification symbols in parenthesis correspond to the Ultra DMA/33 specification name.
2. These cycle timings are based on the STOBE period as indicated in Figure 44. However, Table 13 in the PIIX4 datasheet refers to cycle time strobe periods as 120 ns, 90 ns and 60 ns for mode 0, 1, and 2 respectively. The datasheet timings are different because they are based on the number of PCI clocks per cycle, not the actual period between the rise and fall of STROBE.

Table 22. AC Test Loads

Capacitive Load	Signals
120 pf	REFRESH#, TC, SD[15:0], SA[19:0], SBHE#, LA[23:17], I0CS16#, MEMCS16#, MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW#, AEN, BALE, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK
50 pf	DACK#[7:5,3:0], SPKR, INTR, NMI, BIOSCS#, KBCCS#, RTCCS#, PCS[1:0]#, MCCS#, RTCALE, XDIR#, XOE#, IGNNE#, PDD[15:0], SDD[15:0], APICCS#, DIOR#, DIOW#, PDDACK#, SDDACK#, #, PDCS1# PDCS3#, SDCS1#, SDCS3##, PDA[2:0], SDA[2:0].

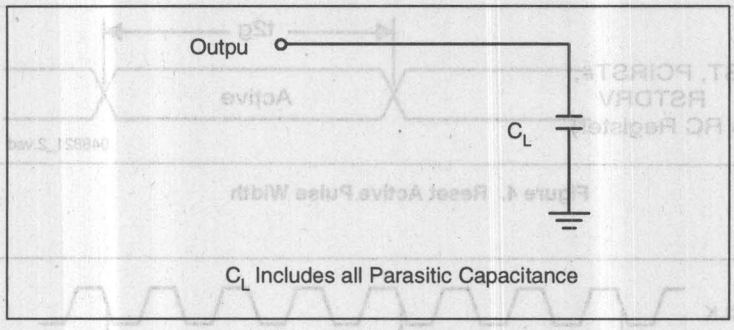


Figure 1. Test Load

2.4 Clock, Reset, ISA Bus, X-Bus, and Host Timing Diagrams

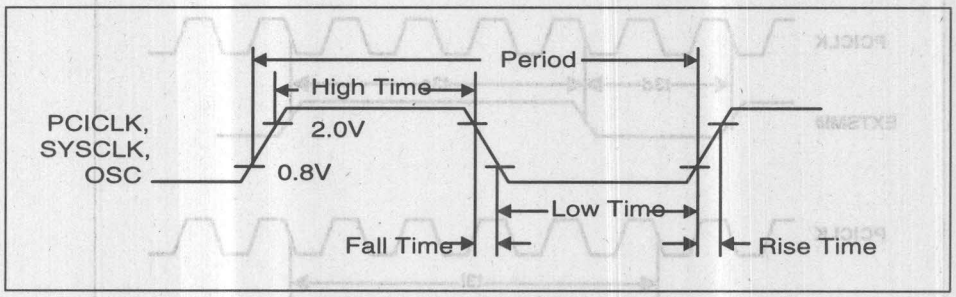


Figure 2. Clock Timing

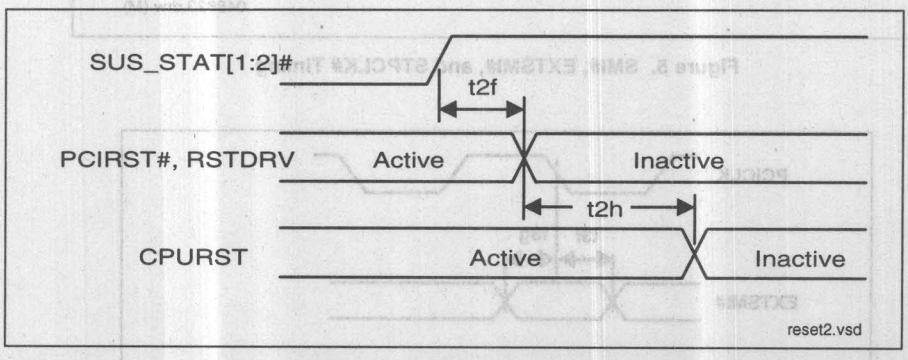


Figure 3. Reset Inactive Timing

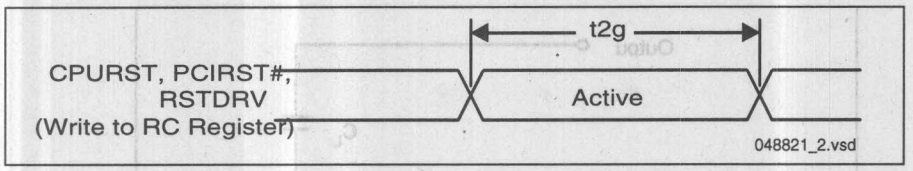


Figure 4. Reset Active Pulse Width

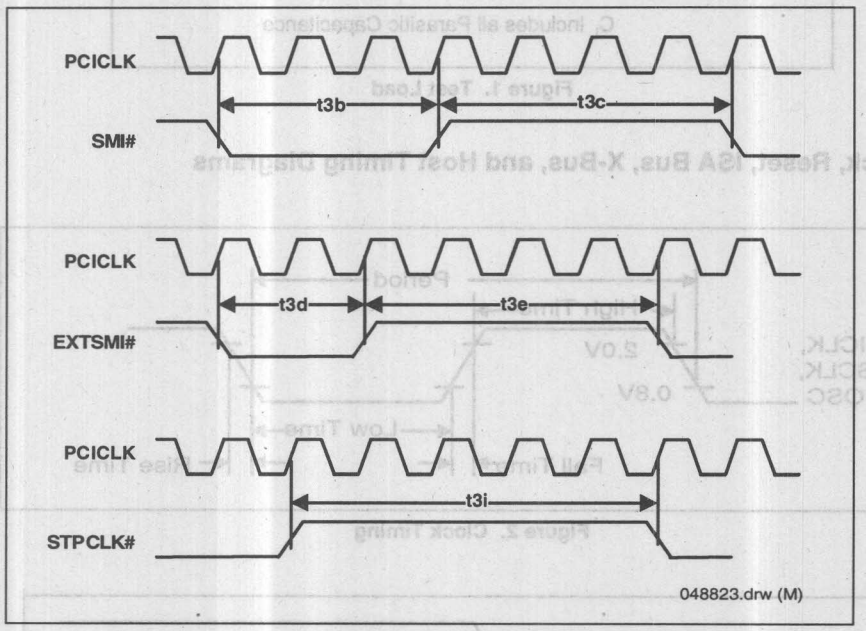


Figure 5. SMI#, EXTSMI#, and STPCLK# Timing

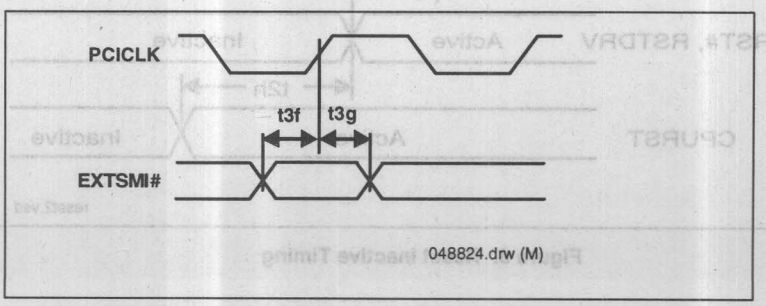


Figure 6. Input to PCICLK Setup/Hold Times

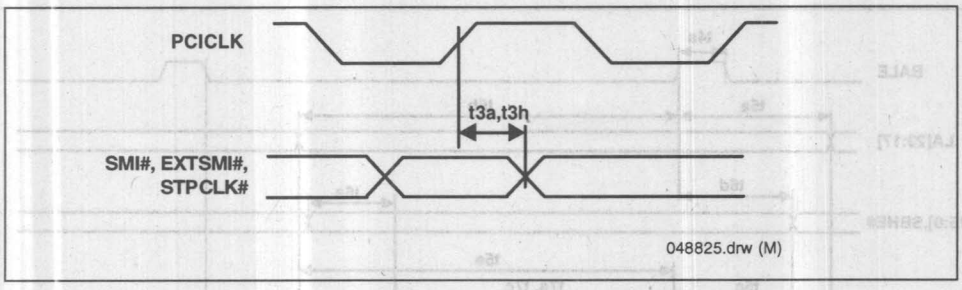


Figure 7. HCLKIN to Output Valid Delay

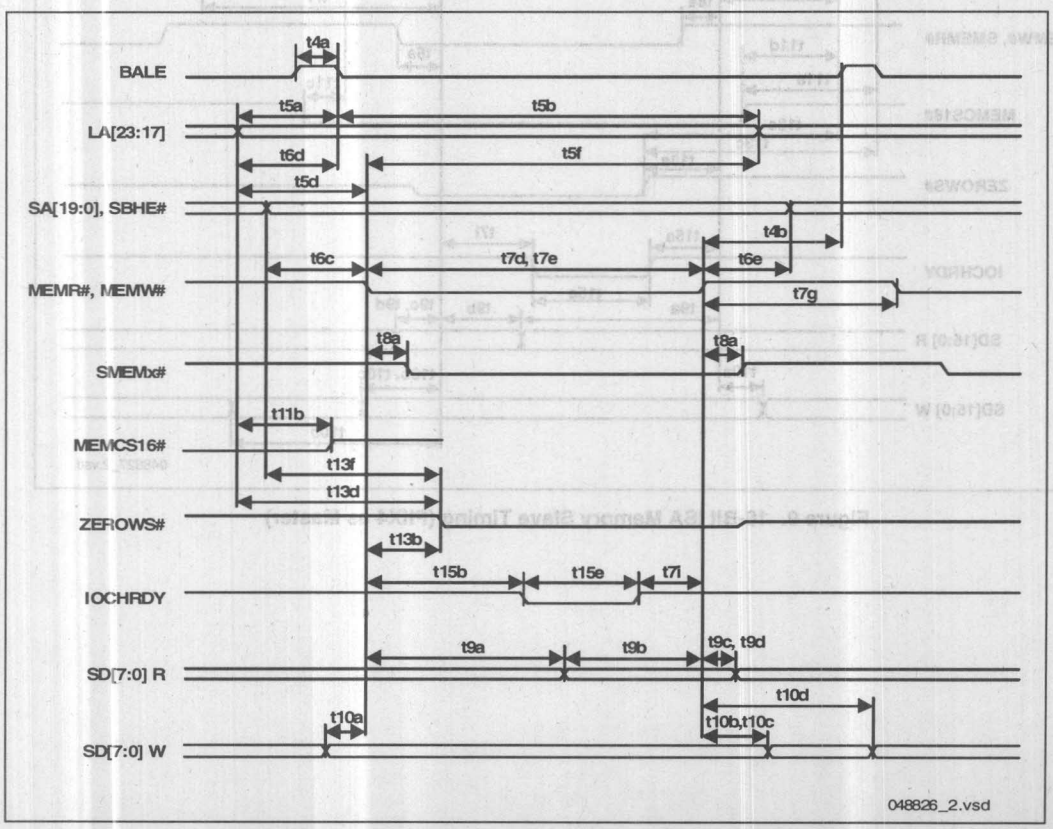


Figure 8. 8-Bit ISA Memory Slave Timing (PIIX4 as Master)

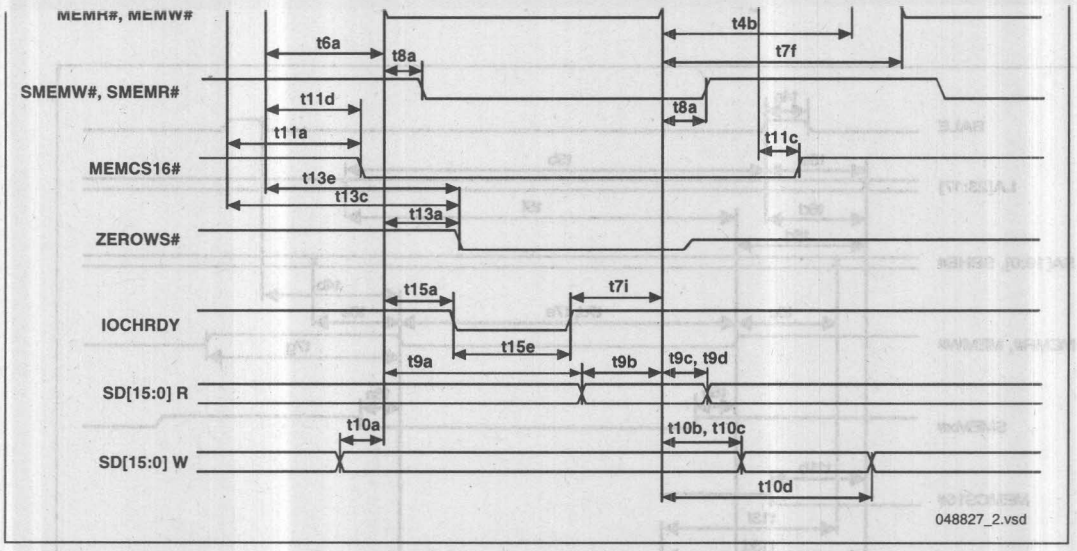


Figure 9. 16-Bit ISA Memory Slave Timing (PIIX4 as Master)

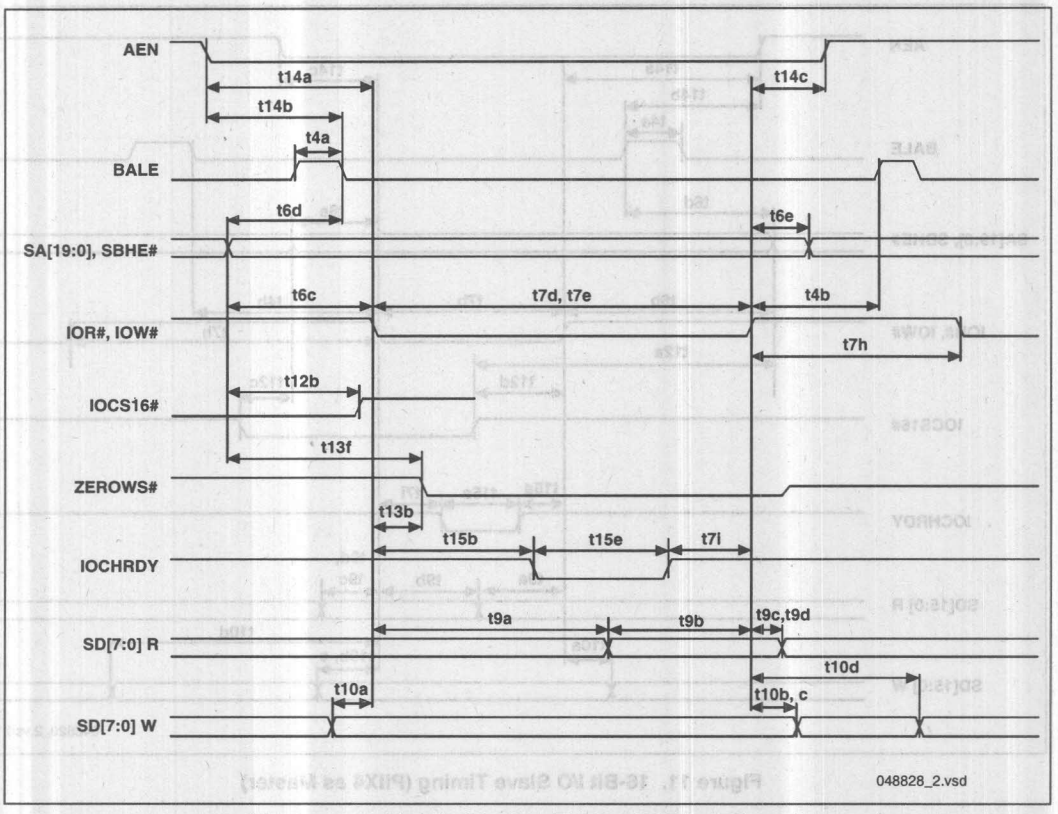


Figure 10. 8-Bit ISA I/O Slave Timing (PIIX4 as Master)

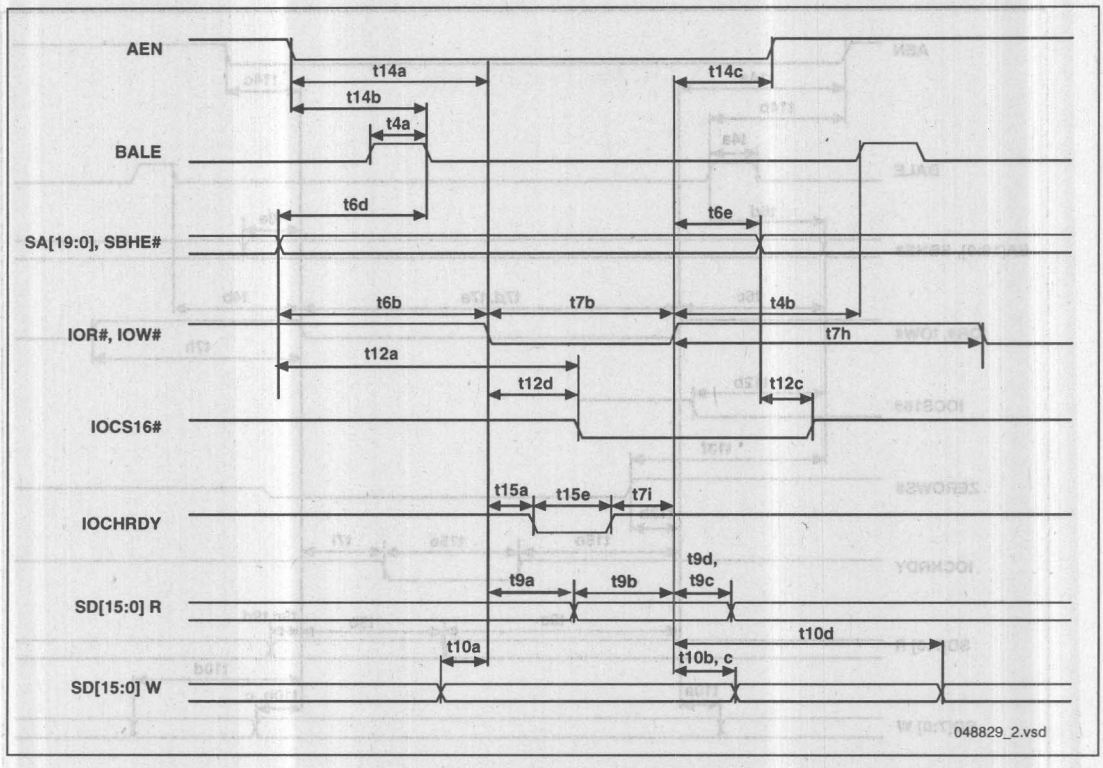


Figure 11. 16-Bit I/O Slave Timing (PIIX4 as Master)

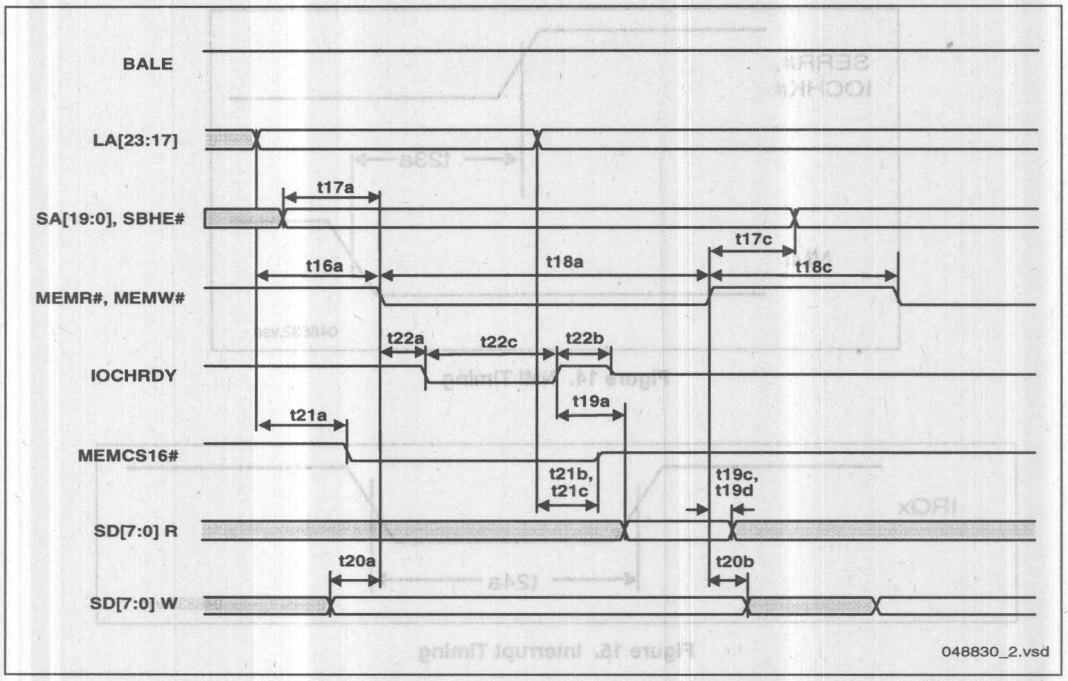


Figure 12. ISA Master Accessing PCI Memory Timing

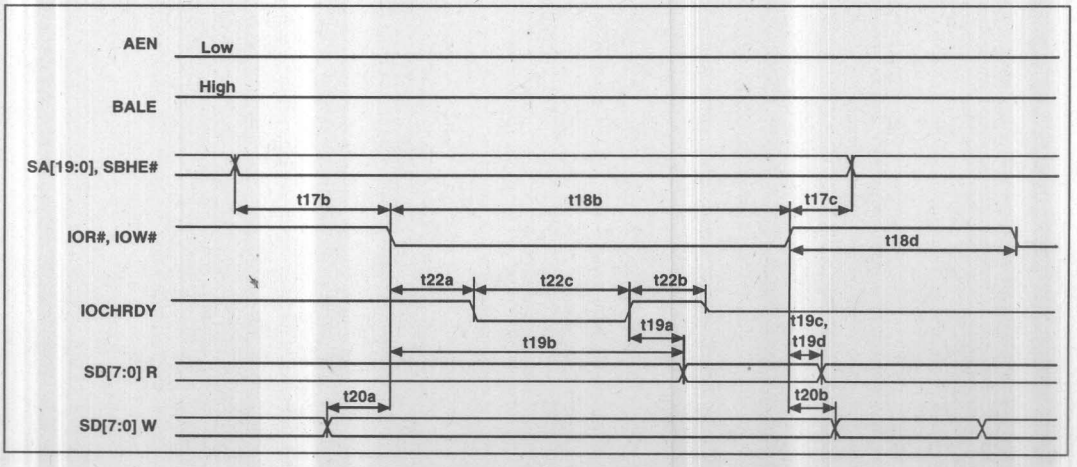


Figure 13. ISA Master Accessing PIIX4 Register Timing

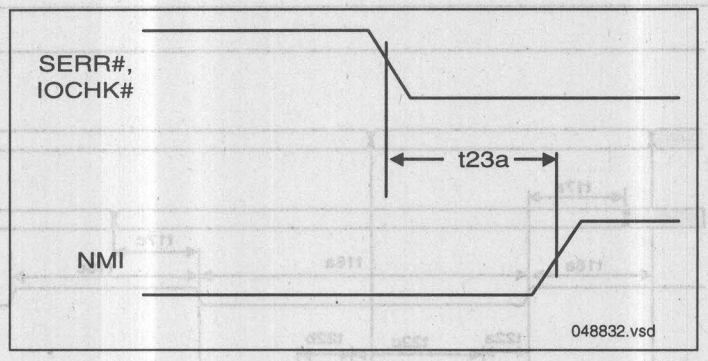


Figure 14. NMI Timing

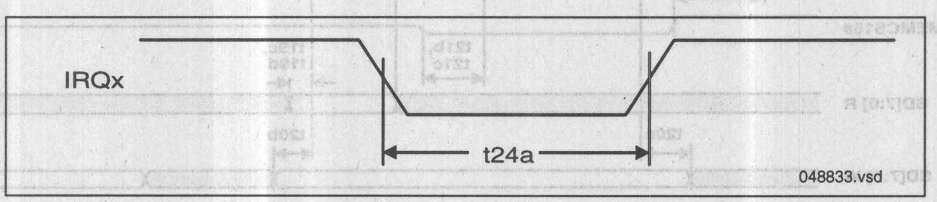


Figure 15. Interrupt Timing

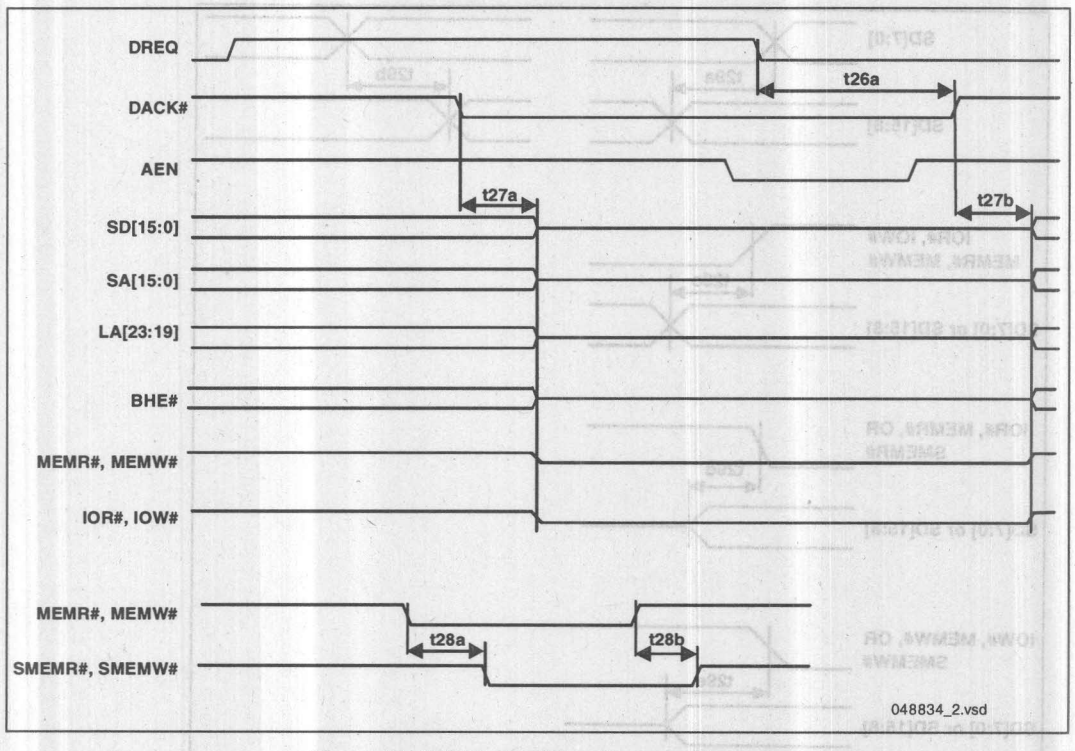


Figure 16. ISA Master Miscellaneous Timing

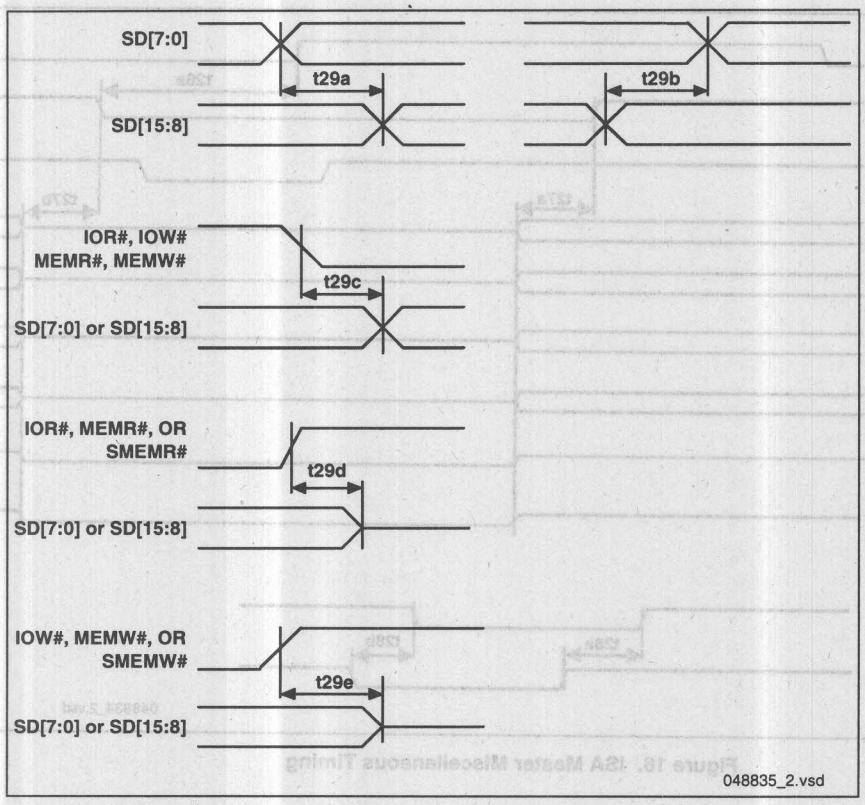


Figure 17. ISA Master Data Swap Timing

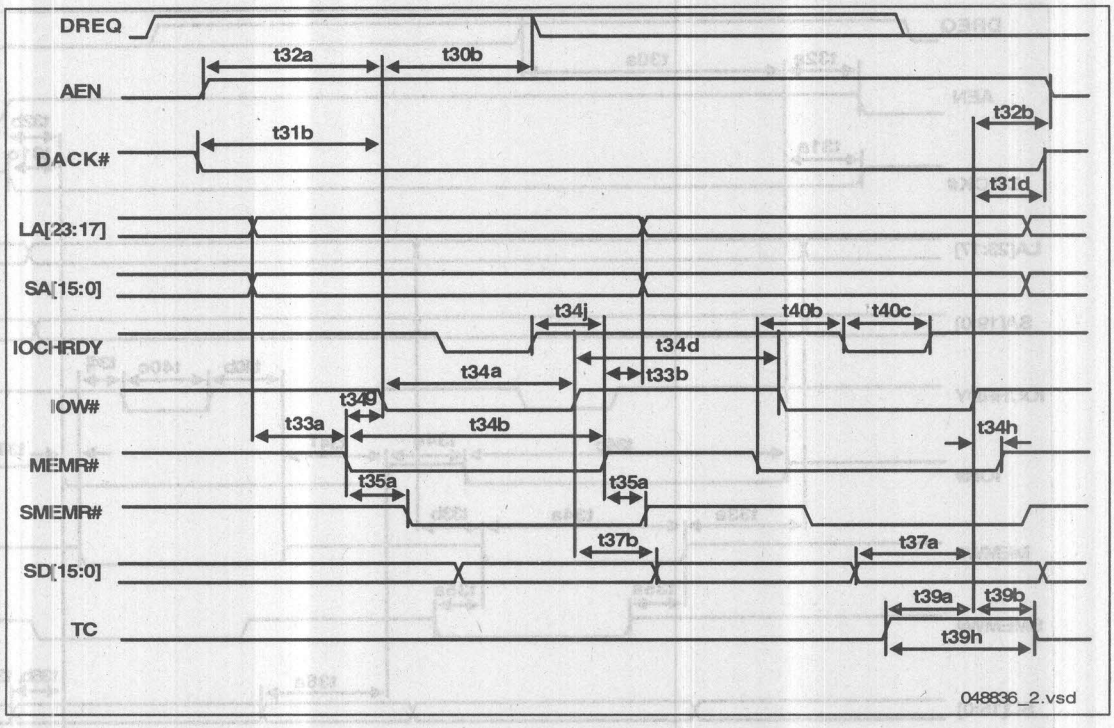


Figure 18. DMA Compatible Timing (Memory Read)

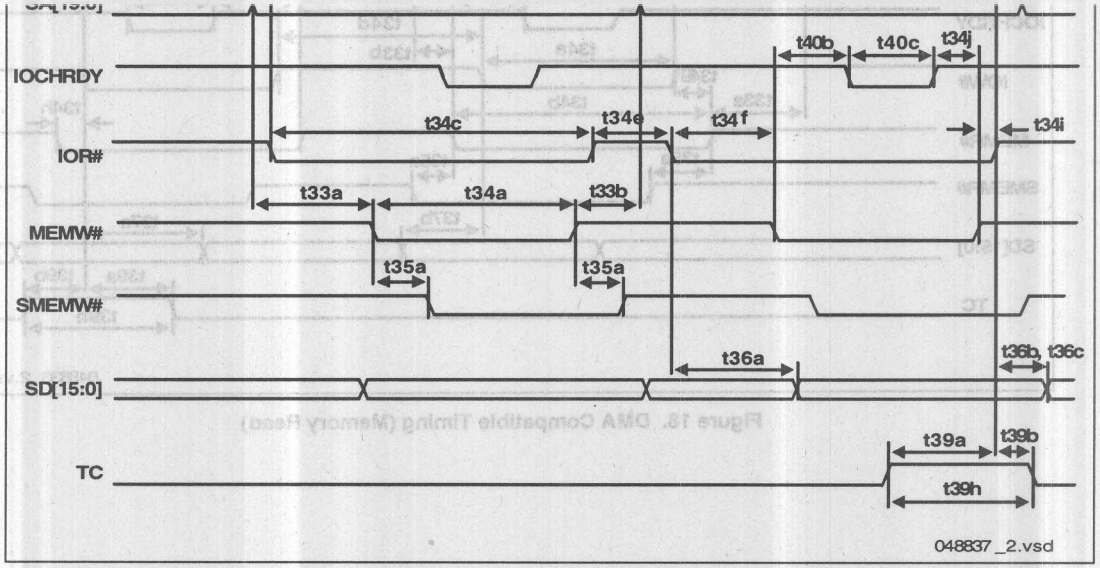


Figure 19. DMA Compatible Timing (Memory Write)

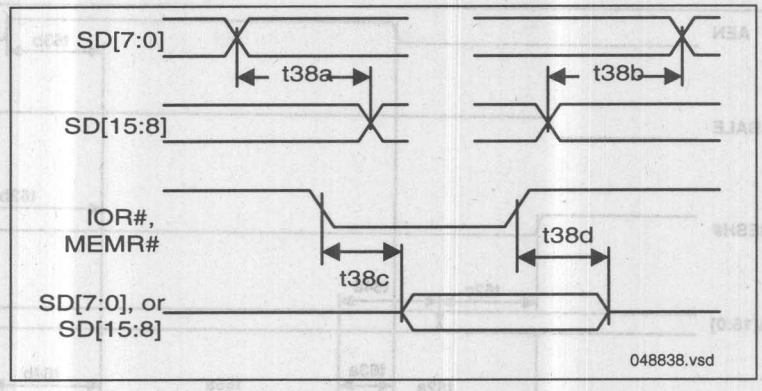


Figure 20. DMA Compatible Timing (Data Swap)

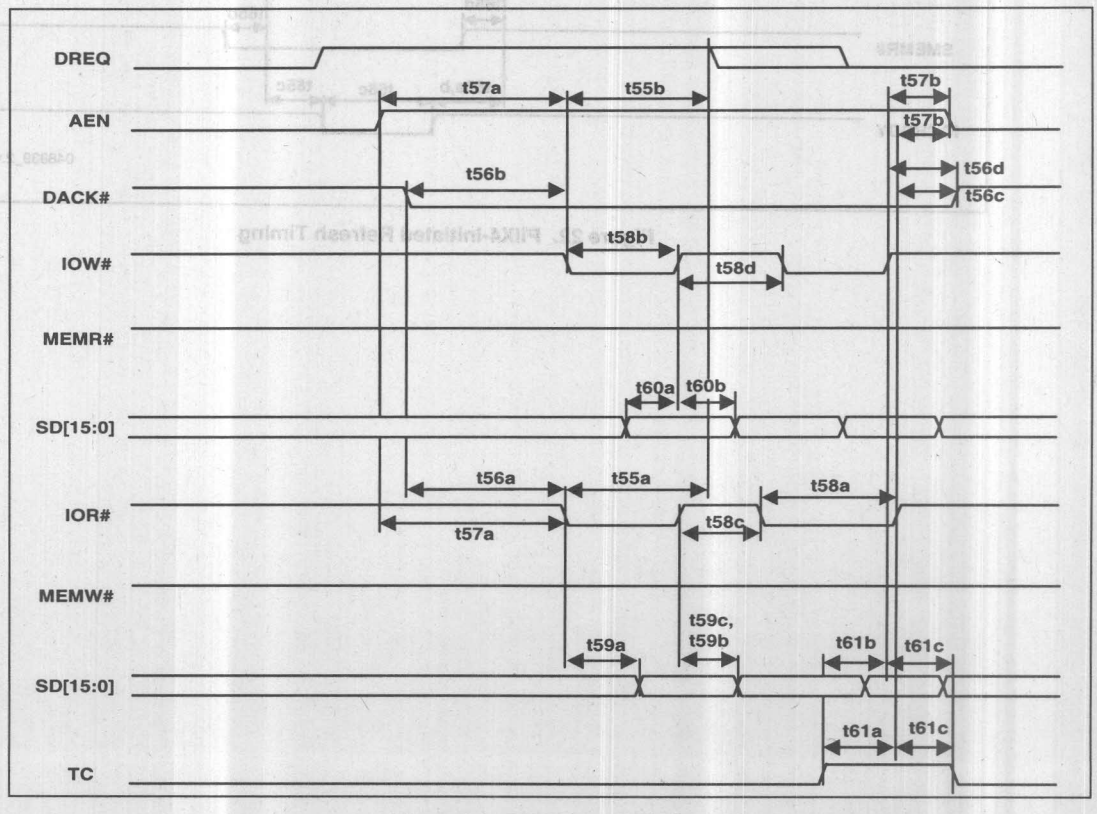


Figure 21. DMA Type F Timing

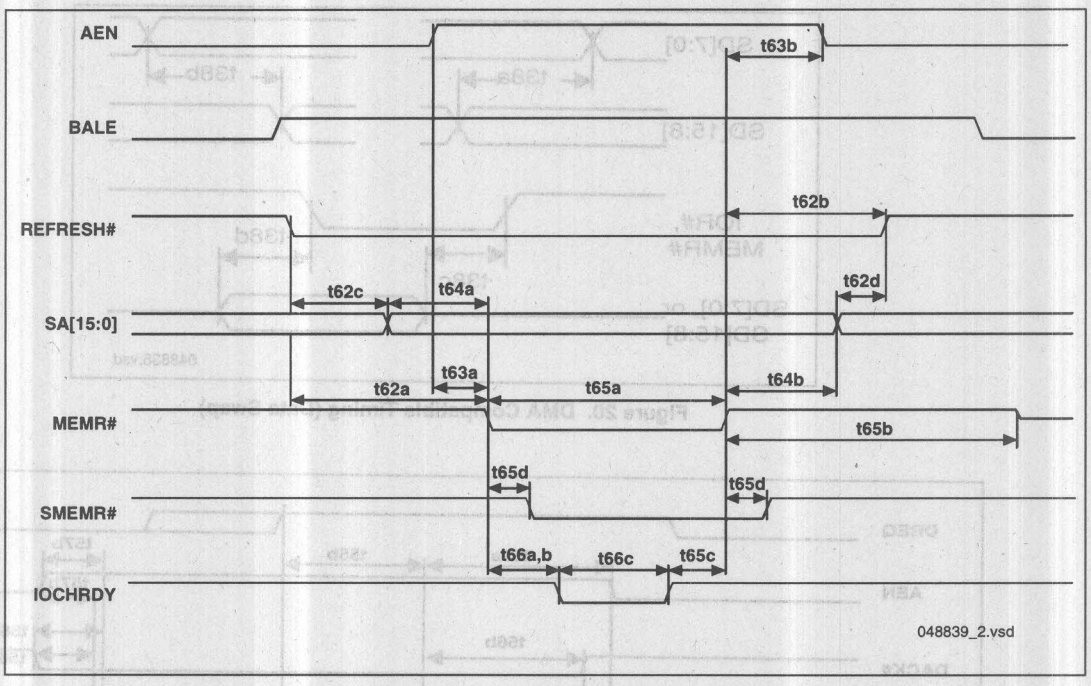


Figure 22. PIIX4-Initiated Refresh Timing

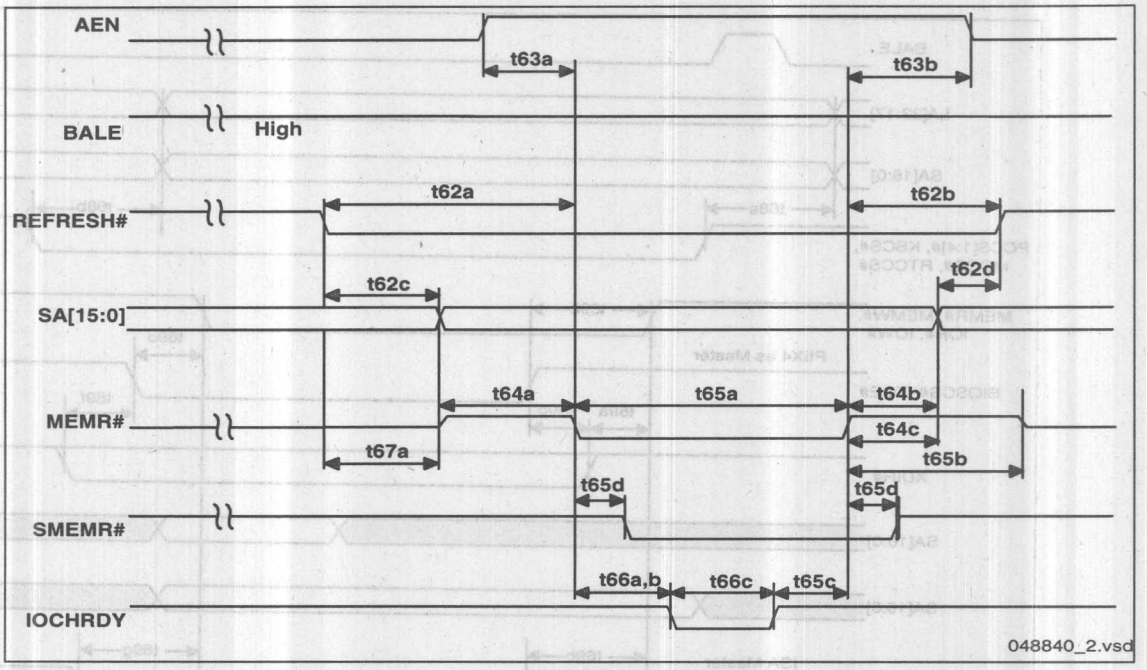


Figure 23. ISA Master-Initiated Refresh Timing

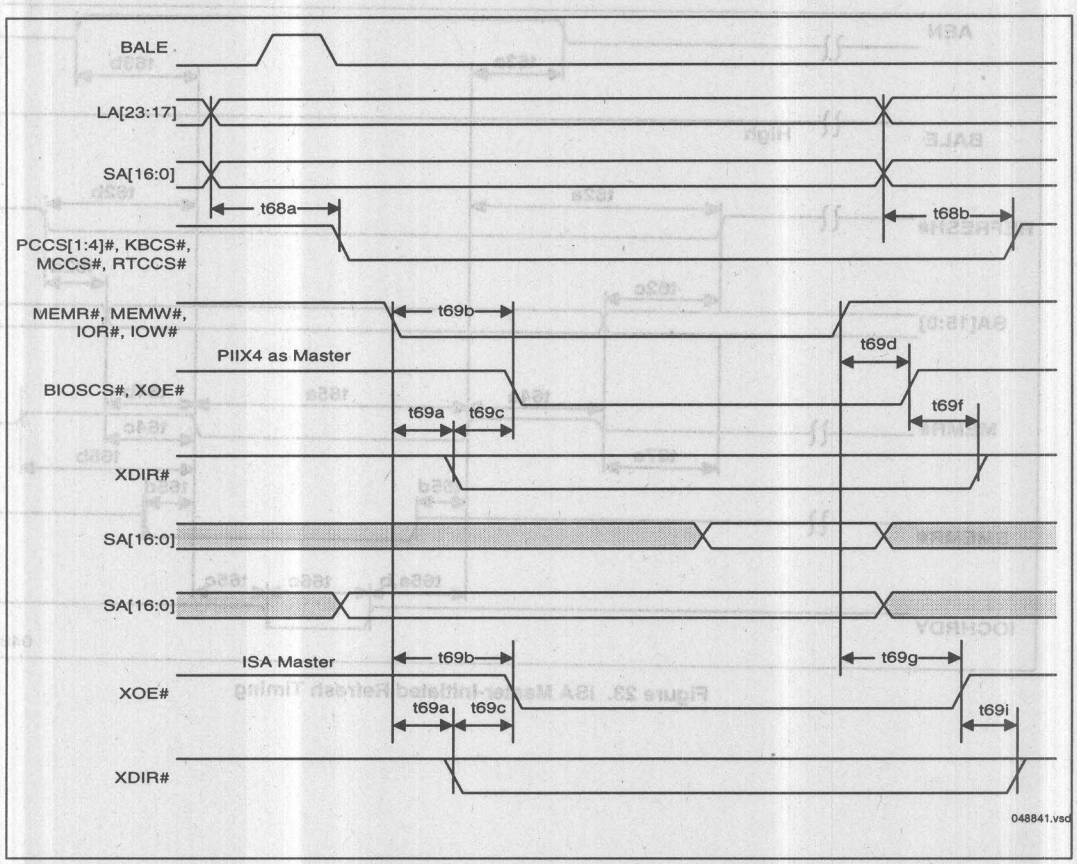


Figure 24. PIIX4 and ISA Master Access to X-Bus Timing

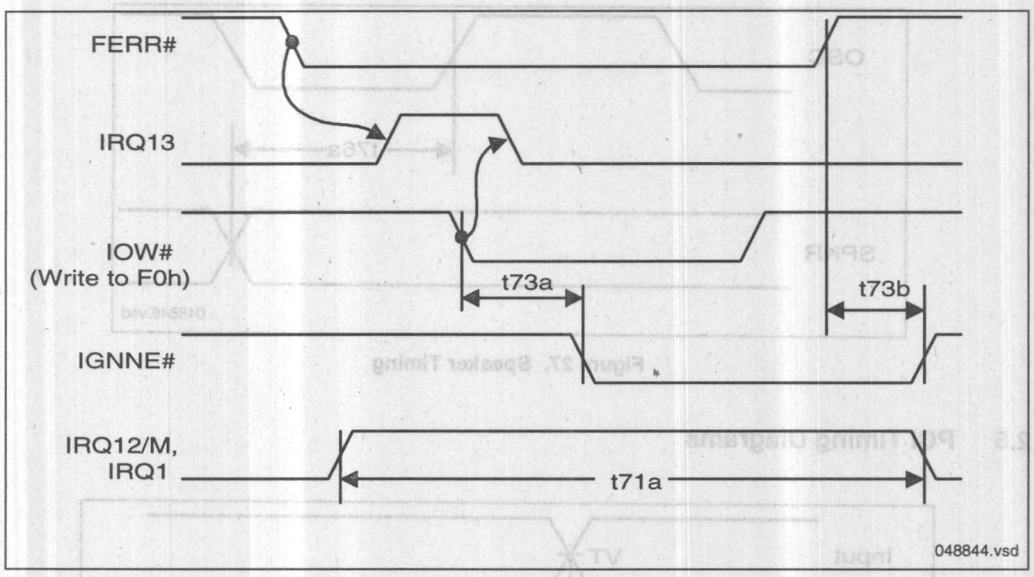


Figure 25. Coprocessor Error and Mouse Support Timing

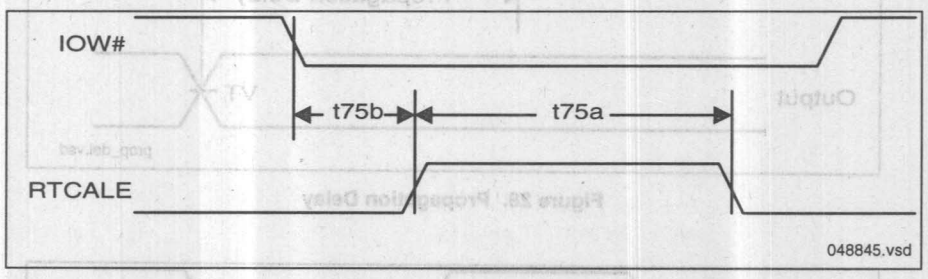


Figure 26. Real Time Clock Timing (RTCALE Generation)

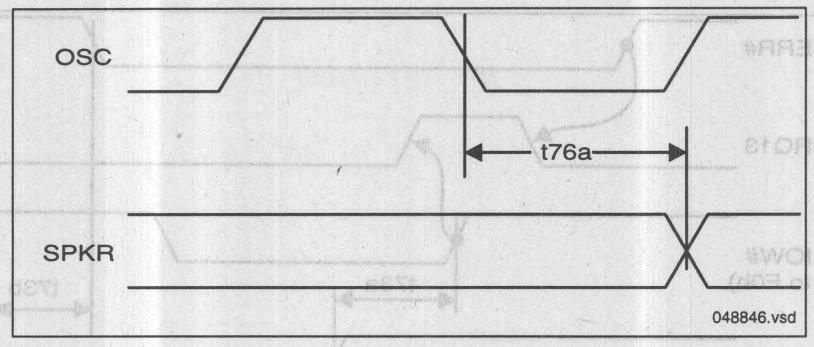


Figure 27. Speaker Timing

2.5 PCI Timing Diagrams

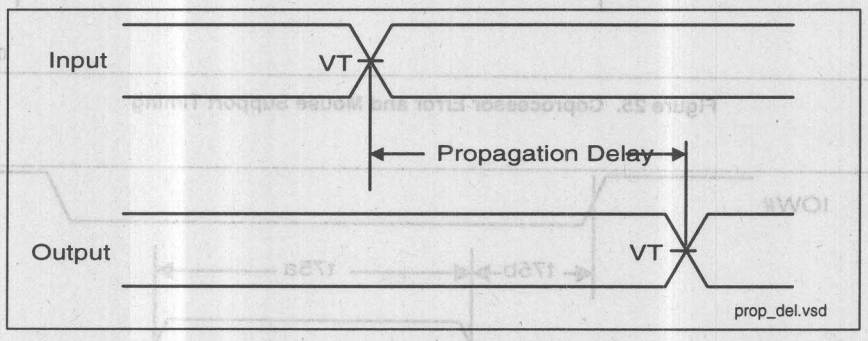


Figure 28. Propagation Delay

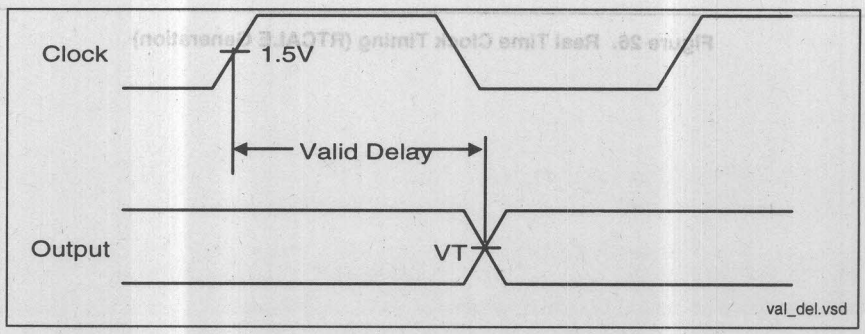


Figure 29. Valid Delay From Rising Clock Edge

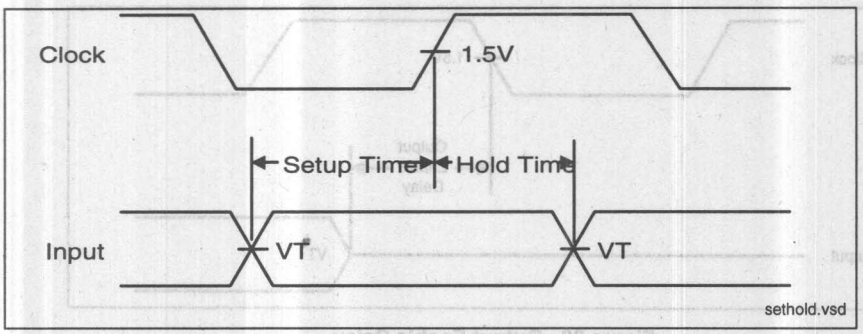


Figure 30. Setup and Hold Times

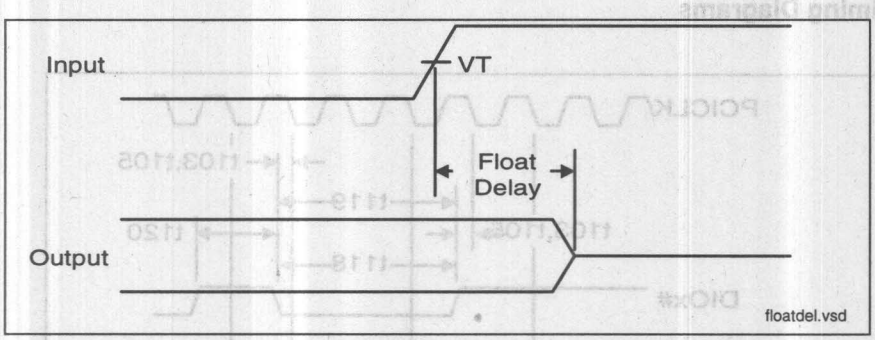


Figure 31. Float Delay

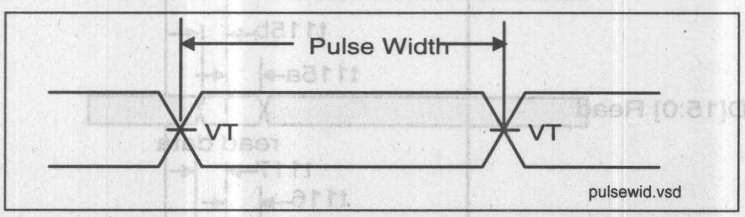


Figure 32. Pulse Width

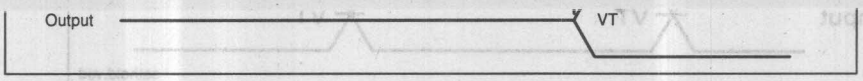


Figure 33. Output Enable Delay

2.6 IDE Timing Diagrams

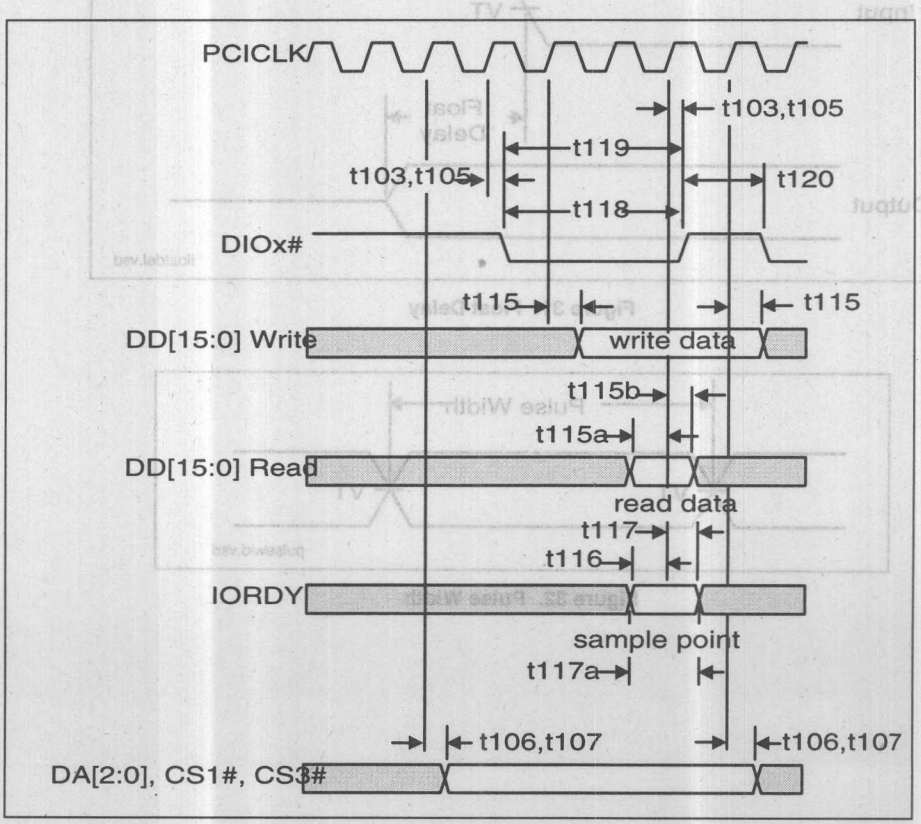


Figure 34. IDE PIO Mode

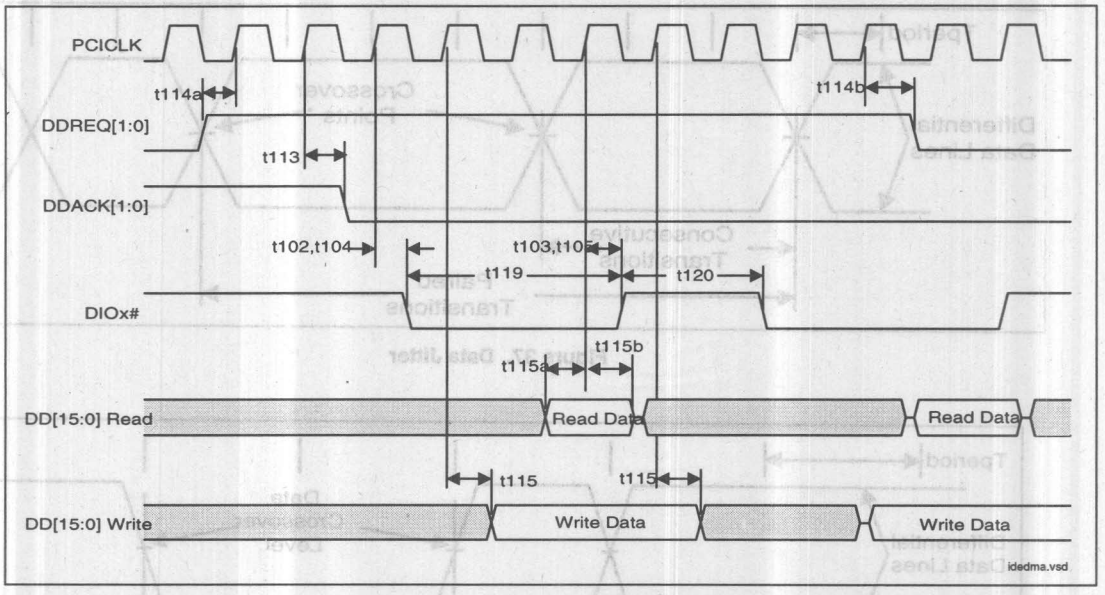


Figure 35. IDE Multiword DMA Mode

2.7 USB Timing Diagrams

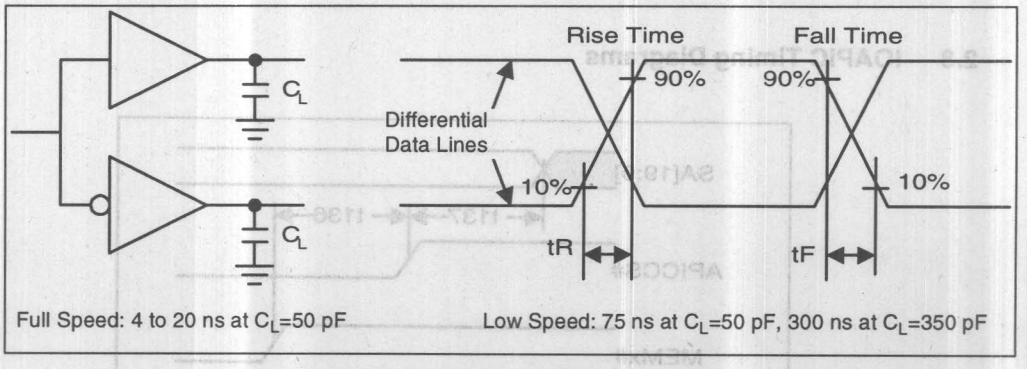


Figure 36. Data Signal Rise and Fall Time

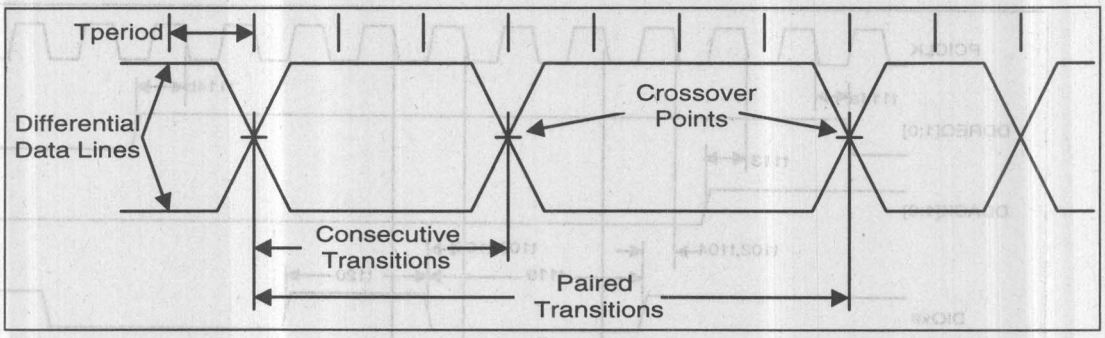


Figure 37. Data Jitter

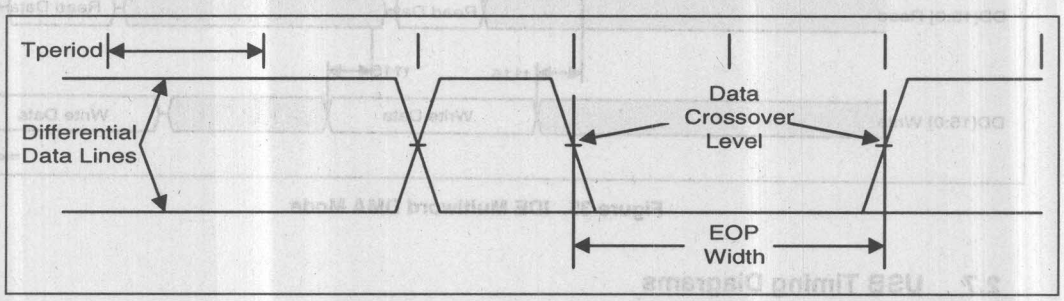


Figure 38. EOP Width Timing

2.8 IOAPIC Timing Diagrams

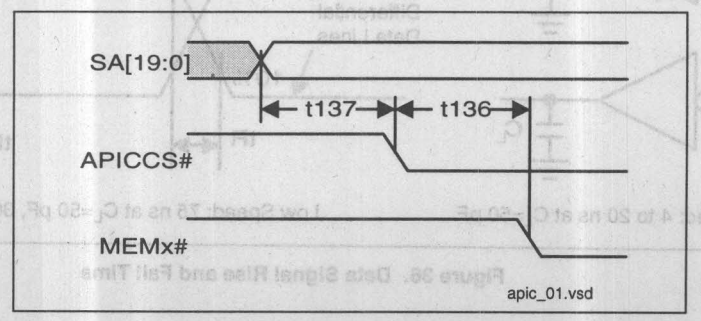


Figure 39. PIIX4 to IOAPIC Timing

2.9 SMBus Timing Diagrams

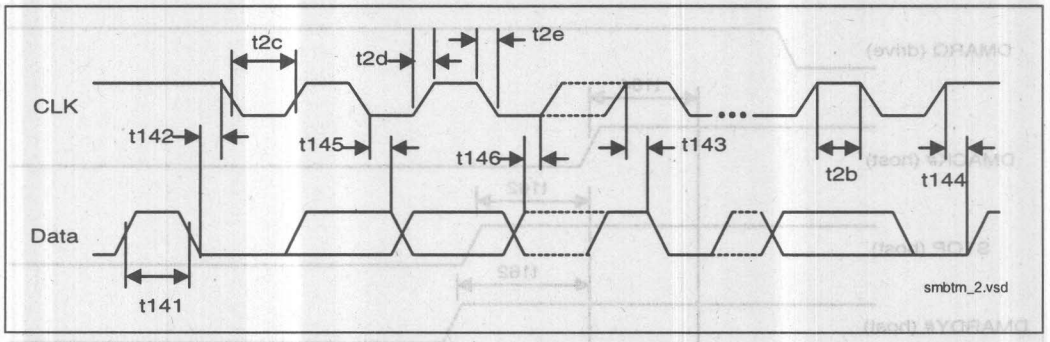


Figure 40. SMBus Timing

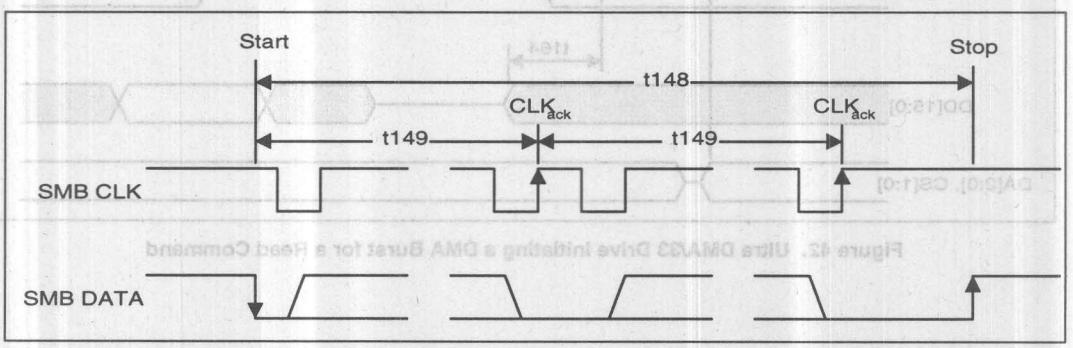


Figure 41. SMBus Timeout timing

2.10 Ultra DMA/33 Timing Diagrams

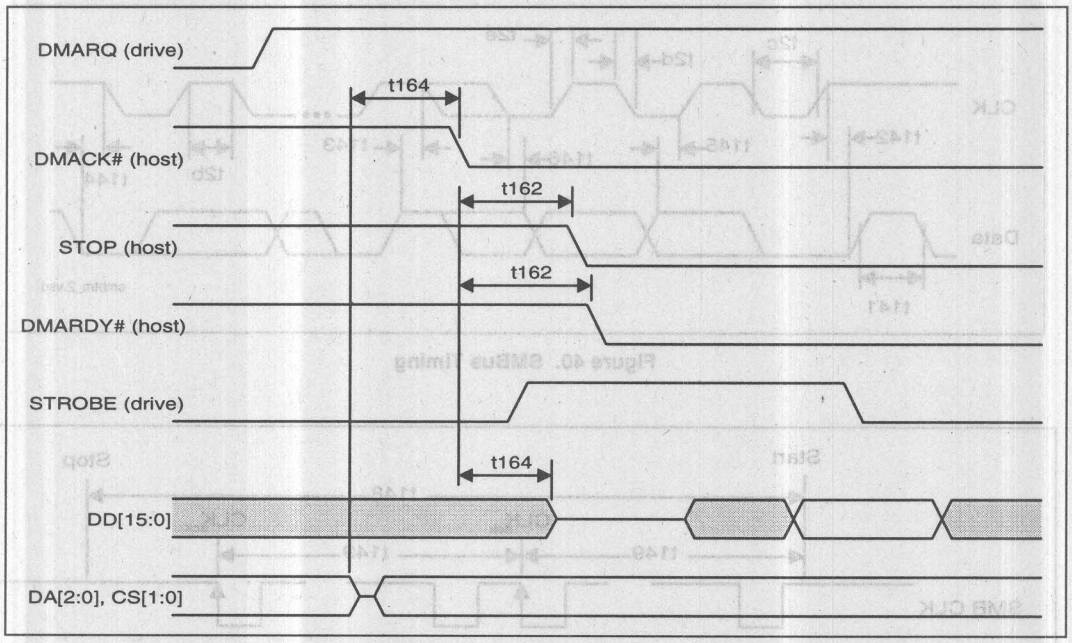


Figure 42. Ultra DMA/33 Drive Initiating a DMA Burst for a Read Command

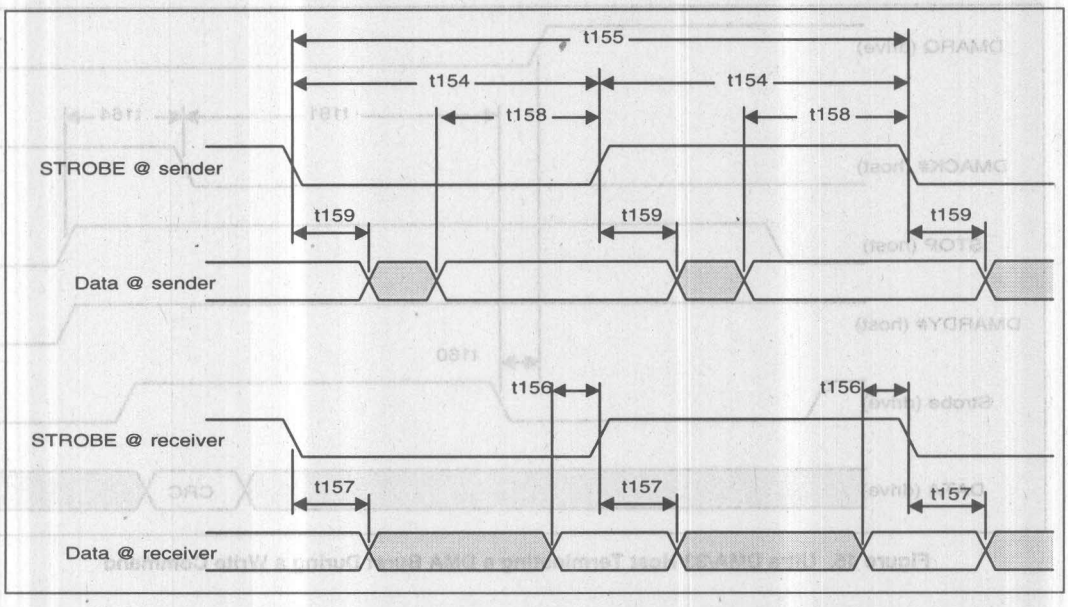


Figure 43. Ultra DMA/33 Sustained Synchronous DMA Burst

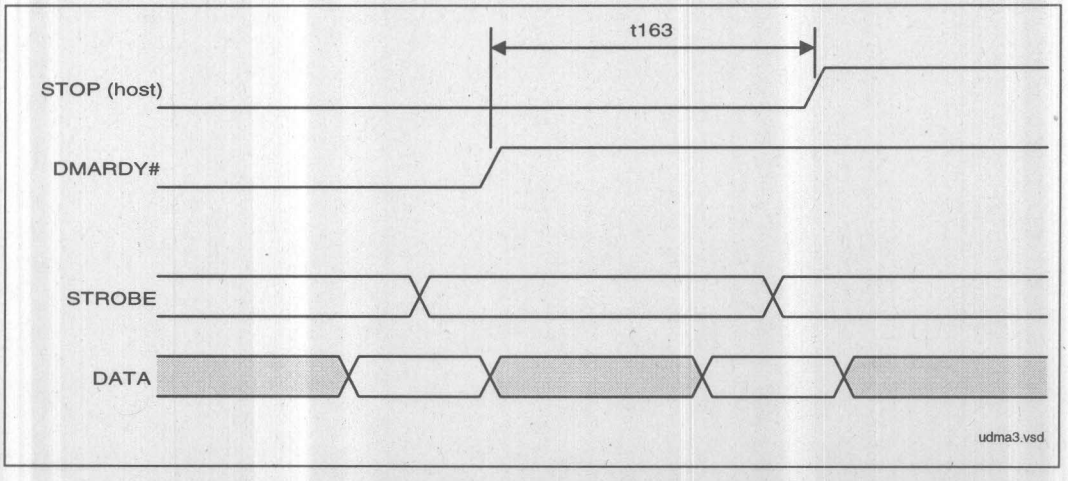


Figure 44. Ultra DMA/33 Sustained Synchronous DMA Burst

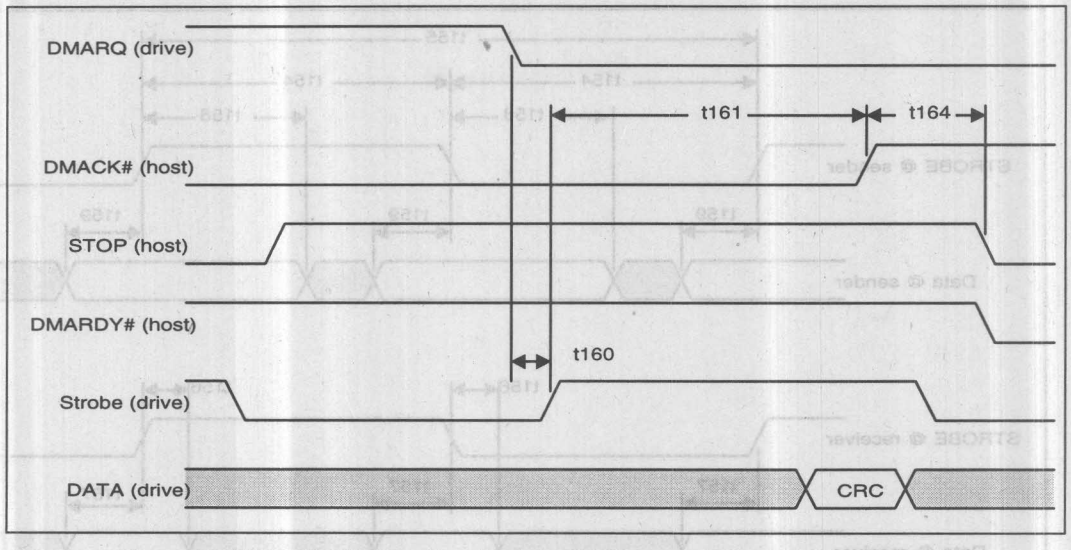


Figure 45. Ultra DMA/33 Host Terminating a DMA Burst During a Write Command

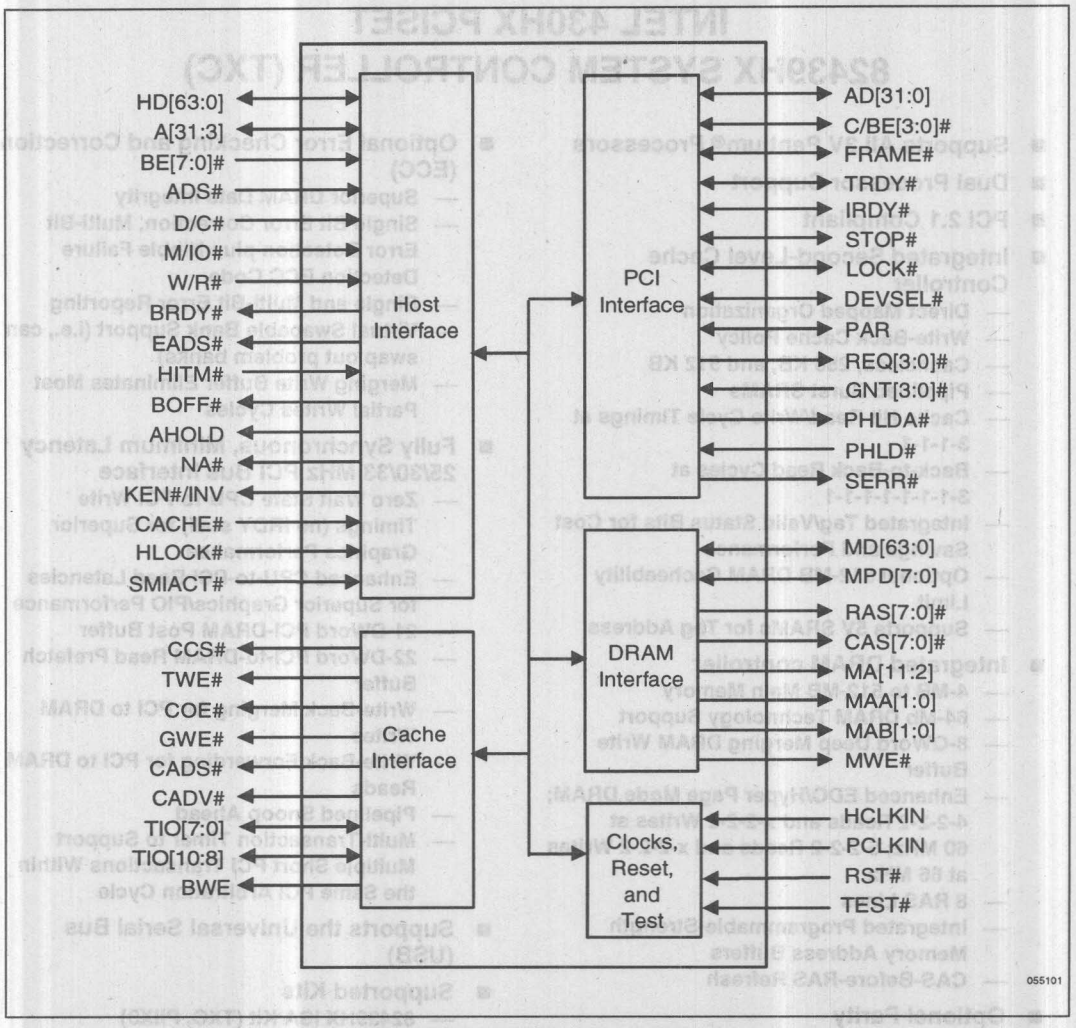
INTEL 430HX PCISET
82439HX SYSTEM CONTROLLER (TXC)

- Supports All 3V Pentium® Processors
- Dual Processor Support
- PCI 2.1 Compliant
- Integrated Second-Level Cache Controller
  - Direct Mapped Organization
  - Write-Back Cache Policy
  - Cacheless, 256 KB, and 512 KB
  - Pipelined Burst SRAMs
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1
  - Integrated Tag/Valid Status Bits for Cost Savings and Performance
  - Optional 512-MB DRAM Cacheability Limit
  - Supports 5V SRAMs for Tag Address
- Integrated DRAM controller
  - 4-MB to 512-MB Main Memory
  - 64-Mb DRAM Technology Support
  - 8-QWord Deep Merging DRAM Write Buffer
  - Enhanced EDO/Hyper Page Mode DRAM; 4-2-2-2 Reads and x-2-2-2 Writes at 60 MHz; 5-2-2-2 Reads and x-2-2-2 Writes at 66 MHz
  - 8 RAS Lines
  - Integrated Programmable-Strength Memory Address Buffers
  - CAS-Before-RAS Refresh
- Optional Parity
- Single 324-Pin BGA Package
- Optional Error Checking and Correction (ECC)
  - Superior DRAM Data Integrity
  - Single Bit Error Correction, Multi-Bit Error Detection plus Nibble Failure Detection ECC Code
  - Single and Multi-Bit Error Reporting
  - Virtual Swapable Bank Support (i.e., can swap out problem banks)
  - Merging Write Buffer Eliminates Most Partial Writes Cycles
- Fully Synchronous, Minimum Latency 25/30/33 MHz PCI Bus Interface
  - Zero Wait State CPU-to-PCI Write Timings (no IRDY stall) for Superior Graphics Performance
  - Enhanced CPU-to-PCI Read Latencies for Superior Graphics/PIO Performance
  - 21-DWord PCI-DRAM Post Buffer
  - 22-DWord PCI-to-DRAM Read Prefetch Buffer
  - Write-Back Merging for PCI to DRAM Writes
  - Write-Back Forwarding for PCI to DRAM Reads
  - Pipelined Snoop Ahead
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions Within the Same PCI Arbitration Cycle
- Supports the Universal Serial Bus (USB)
- Supported Kits
  - 82439HX ISA Kit (TXC, PIIX3)
  - 82439HX ISA/DP Kit (TXC, PIIX3, IOAPIC)

The Intel 430HX PCIset consists of the 82439HX System Controller (TXC) and the 82371SB PCI I/O IDE Xcelerator (PIIX3). The TXC is a single-chip host-to-PCI bridge and provides the second level cache control and DRAM control functions. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory is implemented with synchronous pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. The TXC provides a 64/72-bit data path to main memory and memory sizes up to 512 Mbytes. The DRAM controller provides eight rows and optional DRAM Error detection/correction or parity. The TXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, The TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC contains read prefetch and posted write buffers.

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April 1997 Order Number: 290551-002



82439HX TXC Simplified Block Diagram

1.0. ARCHITECTURE OVERVIEW

The TXC interfaces with the Pentium® processor host bus, a dedicated memory data bus, and the PCI bus (Figure 1). The TXC connects directly to the Pentium processor 3V host bus, directly to 5V or 3V DRAMs, and directly to the 5V PCI bus. The Intel 430HX PCIset consists of the 82439HX TXC and the PCI IDE/ISA Xcellerator (PIIX3) components. PIIX3 provides the PCI-to-ISA bridge functions along with other features such as a fast IDE interface, Plug-n-Play port, APIC interface, Universal Serial Bus (USB) and PCI 2.1 Compliance operation.

Data Flow

Processor cycles are sent directly to the second level cache with control for the second level cache provided by the TXC. All other processor cycles are sent to their destination (DRAM, PCI or internal TXC configuration space) via the TXC. PCI Master cycles are sent to main memory through the TXC. The TXC performs snoop or inquire cycles using the host bus.

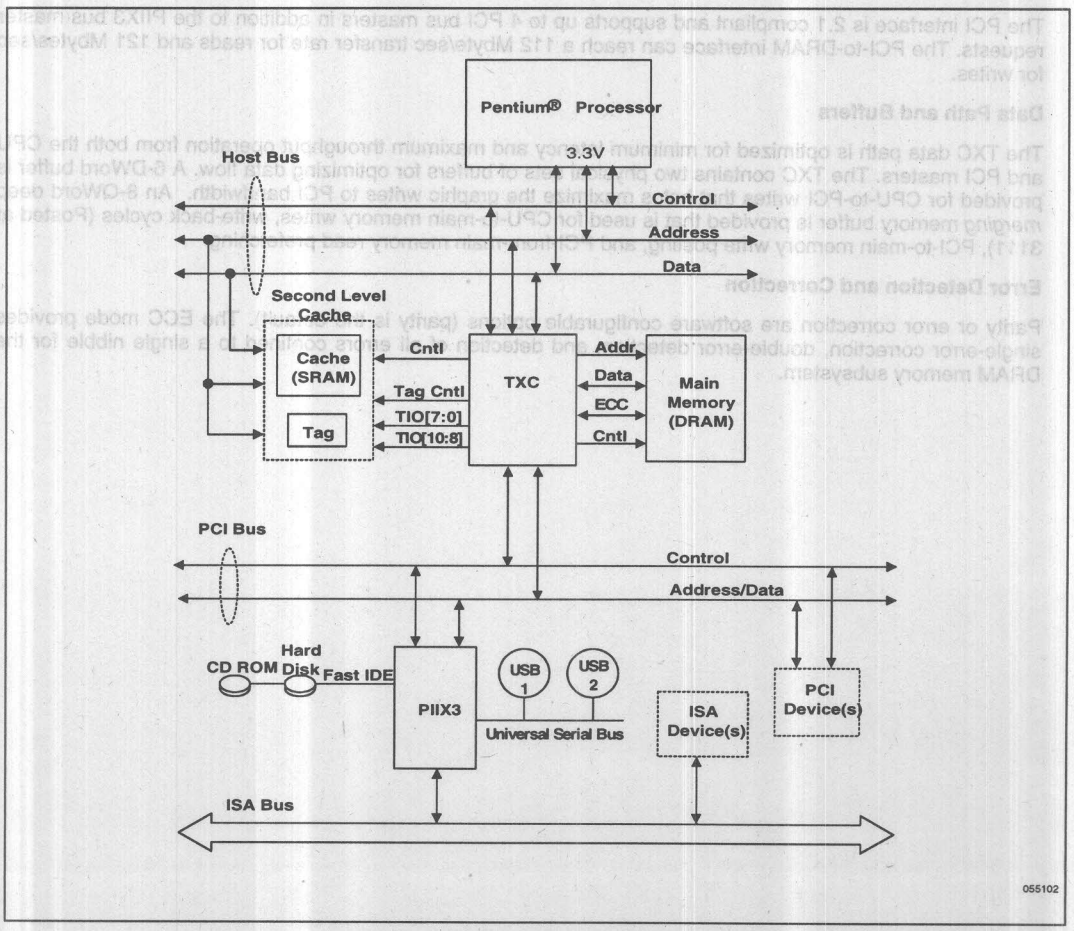


Figure 1. TXC System Block Diagram

DRAM Interface

The DRAM interface is a 64/72-bit data path that supports both standard page mode and Extended Data Out (EDO) memory. The DRAM interface supports 4 Mbytes to 512 Mbytes with 8 RAS lines and also supports symmetrical and asymmetrical addressing for 1M, 2M, and 4M deep SIMMs and symmetrical addressing for 16-Mbyte deep SIMMs.

Second Level Cache

The TXC supports a write-back cache policy providing all necessary snoop functions and inquire cycles. The second level cache is direct mapped and supports both a 256-Kbyte or 512-Kbyte SRAM configuration using pipelined burst SRAMs. The burst 256-Kbyte configuration performance is 3-1-1-1 for read/write cycles; pipelined back-to-back reads can maintain a 3-1-1-1-1-1-1-1 transfer rate. An optional mode extends the DRAM L2 cacheability range to 512 Mbytes.

PCI Interface

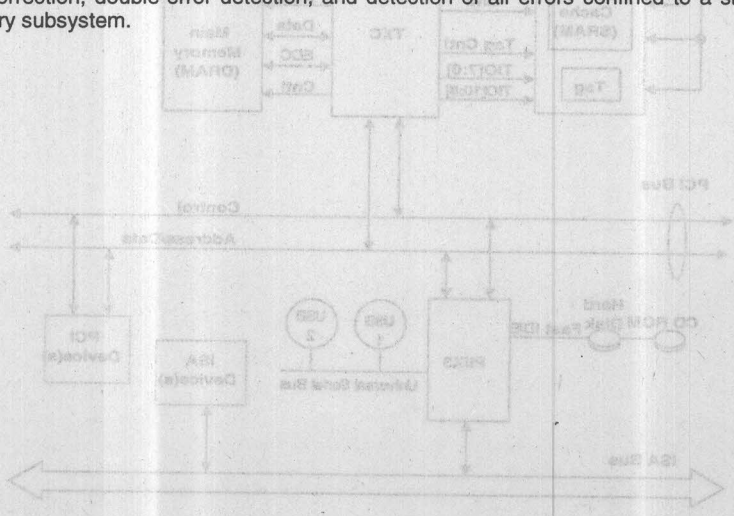
The PCI interface is 2.1 compliant and supports up to 4 PCI bus masters in addition to the PIIX3 bus master requests. The PCI-to-DRAM interface can reach a 112 Mbyte/sec transfer rate for reads and 121 Mbytes/sec for writes.

Data Path and Buffers

The TXC data path is optimized for minimum latency and maximum throughput operation from both the CPU and PCI masters. The TXC contains two physical sets of buffers for optimizing data flow. A 6-DWord buffer is provided for CPU-to-PCI writes that helps maximize the graphic writes to PCI bandwidth. An 8-QWord deep *merging* memory buffer is provided that is used for CPU-to-main memory writes, write-back cycles (Posted at 3111), PCI-to-main memory write posting, and PCI-from-main memory read prefetching.

Error Detection and Correction

Parity or error correction are software configurable options (parity is the default). The ECC mode provides single-error correction, double-error detection, and detection of all errors confined to a single nibble for the DRAM memory subsystem.



2.0. SIGNAL DESCRIPTION

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

All 3V output signals can drive 5V TTL inputs.

2.1. Host Interface

Name	Type	Description
A[31:3]	I/O 3V TTL	**Address Bus:** A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The TXC drives A[31:3] during inquire cycles on behalf of PCI initiators. Strapping options on A[31:28] are described in the Cache Control Register Description section. Strapping options on A27 are described in the DRAMC Register Description.
BE[7:0]#	I 3V TTL	**Byte Enables:** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3V TTL	**Address Status:** The CPU asserts ADS# in T1 of the CPU bus cycle.
BRDY#	O 3V TTL	**Bus Ready:** The TXC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
NA#	O 3V TTL	**Next Address:** The TXC asserts NA# to the CPU to enable pipelining.
AHOLD	O 3V TTL	**Address Hold:** The TXC asserts AHOLD when a PCI initiator is performing a cycle to DRAM.
EADS#	O 3V TTL	**External Address Strobe:** Asserted by the TXC to inquire the first level cache when servicing PCI master references of DRAM.
BOFF#	O 3V TTL	**Back Off:** Asserted by the TXC when required to terminate a CPU cycle that was in progress.
HITM#	I 3V TTL	**Hit Modified:** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.

Name	Type	Description
M/IO#, D/C#, W/R#	I 3V TTL	**Memory/IO; Data/Control; Write/Read:** Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3V TTL	**Host Lock:** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., no PCI activity to DRAM is allowed).
CACHE#	I 3V TTL	**Cacheable:** CACHE# is asserted by the CPU during a read cycle to indicate the CPU will perform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst write-back cycle.
KEN#/INV	O 3V TTL	**Cache Enable:** KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write (read) snoop cycle.
SMIACT#	I 3V TTL	**System Management Interrupt Active:** The CPU asserts SMIACT# when it is in system management mode as a result of an SMI.
HD[63:0]	I/O 3V TTL	**Host Data:** These signals are connected to the CPU data bus.

NOTES:
All of the signals in the host interface are described in the Pentium processor datasheet. The preceding table highlights TXC specific uses of these signals.

2.2. DRAM Interface

Name	Type	Description
MPD[7:0]	I/O 3V/5V TTL	**MEMORY PARITY DATA:** These signals connect to the DRAM parity or ECC bits. The MPD pins have similar timing and drive capability to the MD pins. ECC versus parity operation is determined by PCON[DDIM] field. These signals have internal weak pulldowns, the same as the existing MD signals. These signals are always driven during write cycles, regardless of the existence of parity memory.
RAS[7:0]#	O 3V	**Row Address Strobe:** These pins select the DRAM row.
CAS[7:0]#	O 3V	**Column Address Strobe:** These pins select the DRAM column.
MA[11:2]	O 3V	**Memory Address:** This is the row and column address for DRAM. These buffers include programmable size selection.
MAA[1:0]	O 3V	**Memory Address Copy A:** One copy of the MAs that change during a burst read or write of DRAM. These buffers include programmable size selection.
MAB[1:0]	O 3V	**Memory Address Copy B.** A second copy of the MAs that change during a burst read or write of DRAM. These buffers include programmable size selection.

Name	Type	Description
MWE#	O 3V	**Memory Write Enable.** MWE# should be used as the write enable for the memory data bus. This signal has a programmable size selection (see DRAMEC[MAD] field).
MD[63:0]	I/O 3V/5V TTL	**Memory Data:** These signals are connected to the DRAM data bus.

2.3. Secondary Cache Interface

Name	Type	Description
CADV#	O 3V	**Cache Advance:** Assertion causes the PBSRAM in the secondary cache to advance to the next QWord in the cache line.
CADS#	O 3V	**Cache Address Strobe:** Assertion causes the PBSRAM in the secondary cache to load the PBSRAM address register from the PBSRAM address pins.
CCS#	O 3V	**Cache Chip Select:** When this signal is asserted and CADS# is asserted, the second level cache will power up (if necessary). When this signal is negated and CADS# is asserted, the second level cache will power down. When CCS# is negated the second level cache ignores ADS#. If CCS# is asserted when ADS# is asserted the second level cache will power up (if necessary) and perform an access.
COE#	O 3V	**Cache Output Enable:** The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3V	**Global Write Enable:** GWE# assertion causes all the byte lanes to be written into the secondary cache data RAMs independent of BE[7:0]#.
BWE#	O 3V	**Byte Write Enable:** Asserted low with GWE#=high to enable using host's BE[7:0]# to control byte lanes to pipeline burst SRAM cache.
TIO[10:8]	I/O 3V5V TTL	**Extended Tag Address:** These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. TIO[10:8] contain the optional extension tag address to increase cacheability limit to 512 Mbytes. TIO[10:8] is enabled via the ECE bit of the CC register. When the extended tag address is not enabled, these bits are not used, but are tied internally low to prevent them from floating. TIO[9:8] have internal pull-down resistors. TIO[10] requires an external pull-down resistor for the extended cacheability and a pull-up resistor for the normal cacheability/DRAM cache. The extended cacheability and DRAM cache functions are mutually exclusive.
TIO[7:0]	I/O 3V/5V TTL	**Tag Address:** These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. TIO[7:0] have internal pull-down resistors.
TWE#	O 5V TTL	**Tag Write Enable:** When asserted, new state and tag addresses are written into the external tag.

2.4. PCI Interface

Name	Type	Description
AD[31:0]	I/O 5V	**Address/Data:** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 5V	**Command/Byte Enable:** The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks.
FRAME#	I/O 5V	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 5V	**Device Select:** This signal is driven by the TXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 5V	**Initiator Ready:** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 5V	**Target Ready:** Asserted when the target is ready for a data transfer.
STOP#	I/O 5V	**Stop:** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 5V	**Lock:** Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 5V	**PCI Request:** PCI master requests for PCI. Weak external pull-up resistors are required on these signals.
GNT[3:0]#	O 5V	**PCI Grant:** Permission is given to the master to use PCI. Weak external pull-up resistors are required on these signals.
PHLD#	I 5V	**PCI Hold:** This signal comes from the expansion bridge. It is the bridge request for PCI. The PHLD# protocol supports passive release. A weak external pull-up resistor is required on this signal.
PHLDA#	O 5V	**PCI Hold Acknowledge:** This signal is driven by the TXC to grant PCI to the expansion bridge. The PHLDA# protocol supports passive release. A weak external pull-up resistor is required on this signal.
PAR	I/O 5V	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	O 5V	**SYSTEM ERROR:** The TXC asserts SERR# to signal a system error. A system error can be optionally generated for either single bit error (correctable) events or any ECC bit error (correctable or uncorrectable), or for parity error.

NOTES:
All signals in the PCI interface conform to the PCI Rev 2.1 specification

2.5. Clock, Reset, and Test

Name	Type	Description
RST#	I 5V	**Reset:** When asserted this signal will asynchronously reset the TXC. The PCI signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.
TEST#	I 5V	**Test In:** NAND-tree mode is activated by driving this pin high when REQ [3:0]# pins are 0010. This signal requires an external pull-up resistor.
HCLKIN	I 5V	**Host Clock In:** This pin receives a buffered host clock. This clock is used by all of the TXC logic that is in the Host clock domain.
PCLKIN	I 5V	**PCI Clock In:** This pin receives a buffered divide-by-2 host clock. This clock is used by all of the TXC logic that is in the PCI clock domain.
VDD5V	I 5V	**VDD 5V reference:** This pin provides a 5V reference for all 5V I/O. It requires a 100 ohms series resistor and a 1.0 micro-farad cap to ground.

3.0. REGISTER DESCRIPTION

The TXC contains two sets of software accessible registers (I/O Control and Configuration registers), accessed via the Host CPU I/O address space. The I/O Control registers control access to PCI configuration space. Configuration Registers reside in PCI configuration space and specify PCI configuration, DRAM configuration, cache configuration, operating parameters, and optional system features.

The TXC internal registers (both I/O Control and Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFADD which can only be accessed as a Dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes.

RO **Read Only**. If a register is read only, writes to this register have no effect.

R/W **Read/Write**. A register with this attribute can be read and written.

R/WC **Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the TXC registers described in this section contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the TXC contains address locations in the PCI configuration space that are marked "Reserved" (Table 2). The TXC responds to accesses to these address locations by completing the Host cycle. Software should not write to reserved TXC configuration locations in the device-specific region (above address offset 3Fh).

During a hard reset (RST# asserted), the TXC sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the TXC registers accordingly.

3.1. I/O Control Registers

The TXC contains two registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) register and the Configuration Data (CONFDATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1. CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h (Accessed as a Dword)
Default Value: 00000000h
Access: Read/Write

CONFADD is a 32-bit register accessed only when referenced as a Dword. A Byte or Word reference will "pass through" the Configuration Address register to the PCI Bus. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CONE).** 1=Enable. 0=Disable.
30:24	**Reserved.**
23:16	**Bus Number (BUSNUM).** When BUSNUM is programmed to 00h, the target of the configuration cycle is either the TXC or the PCI Bus that is directly connected to the TXC, depending on the Device Number field. If the Bus Number is programmed to 00h and the TXC is not the target, a type 0 configuration cycle is generated on PCI. If the Bus Number is non-zero, a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**Device Number (DEVNUM).** This field selects one agent on the PCI Bus selected by the Bus Number. During a Type 1 Configuration cycle, this field is mapped to AD[15:11]. During a Type 0 configuration cycle, this field is decoded and one of AD[31:11] is driven to 1. The TXC is always Device Number 0.
10:8	**Function Number (FUNCNUM).** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The TXC responds to configuration cycles with a function number of 000b; all other function number values attempting access to the TXC (Device Number = 0, Bus Number = 0) generate a type 0 configuration cycle on the PCI Bus with no IDSEL asserted, which results in a master abort.
7:2	**Register Number (REGNUM).** This field selects one register within a particular bus, device, and function as specified by the other fields in the Configuration Address register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.1.2. CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write

CONFDATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFADD is 1, any I/O reference in the CONFDATA I/O space is mapped to configuration space using the contents of CONFADD.

3.2. PCI Configuration Space Mapped Registers

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium processor, configuration space is not supported. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The TXC only supports Mechanism #1 (both type 0 and 1 accesses). Table 1 shows the TXC configuration space.

The configuration access mechanism makes use of the CONFADD register and CONFDATA register. To reference a configuration register, a Dword I/O write cycle is used to place a value into CONFADD that specifies the PCI Bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. Then, CONFDATA becomes a window onto four bytes of configuration space specified by the contents of CONFADD. Read/write accesses to CONFDATA generates a PCI configuration cycle to the address specified by CONFADD.

3.2.1. PCI CONFIGURATION ACCESS

Type 0 Access: If the Bus Number field of CONFADD is 0, a type 0 configuration cycle is generated on PCI. CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The TXC is Device #0 and does not pass its configuration cycles to PCI. Thus, AD11 is never asserted. (For accesses to device #1, AD12 is asserted, etc., to Device #20 which asserts AD31.) Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which results in a master abort.

Type 1 Access: If the Bus Number field of CONFADD is non-zero, a type 1 configuration cycle is generated on PCI. CONFADD[23:2] are mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

Table 1. TXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	PCI Command	R/W
06–07h	PCISTS	PCI Status	RO, R/WC
08h	RID	Revision Identification	RO
09–0Bh	CLASSC	Class Code	RO
0Ch	—	Reserved	—
0Dh	MLT	Master Latency Timer	R/W
0Eh	HEADT	Header Type	—
0Fh	BIST	BIST	R/W
10–4Fh	—	Reserved	—
50h	PCON	PCI Control	R/W
51h	—	Reserved	—
52h	CC	Cache Control	R/W

Table 1. TXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
53–55h	—	Reserved	—
56h	DRAMEC	DRAM Extended Control	R/W
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	R/W
60–67h	DRB[7:0]	DRAM Row Boundary (8 registers)	R/W
68h	DRT	DRAM Row Type	R/W
69h	DRAT	DRAM Row Type	R/W
70–71h	—	Reserved	—
72h	SMRAM	System Management RAM Control	R/W
73–8Fh	—	Reserved	—
90h	ERRCMD	Error Command	R/W
91h	ERRSTS	Error Status	RO, RWC
92h	ERRSYN	Error Syndrome	RO
93–FFh	—	Reserved	—

3.2.2. VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel.

3.2.3. DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 1250h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the TXC.

3.2.4. PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h
Default: 06h
Access: Read/Write

This 16-bit register provides basic control over the TXC's ability to respond to PCI cycles. The PCICMD register in the TXC enables and disables the assertion of SERR# and PCI master accesses to main memory.

Bit	Descriptions
15:10	**Reserved.**
9	**Fast Back-to-Back (FB2B): (Not Implemented)** This bit is hardwired to 0.
8	**SERR# Enable (SERRE):** 1=Enable. 0=Disable. In systems that wish to report memory errors this bit should be set to 1 after memory has been scrubbed by BIOS
7	**Address/Data Stepping: (Not Implemented)** This bit is hardwired to 0.
6	**Parity Error Enable (PERRE): (Not Implemented)** This bit is hardwired to 0.
5	**Video Pallet Snooping (VPS): (Not Implemented)** This bit is hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE): (Not Implemented)** This bit is hardwired to 0. The TXC never uses the Memory Write and Invalidate PCI command.
3	**Special Cycle Enable (SCE): (Not Implemented)** This bit is hardwired to 0. The TXC does not respond to PCI special cycles.
2	**Bus Master Enable (BME): (Not Implemented)** This bit is hardwired to 1. The TXC does not support disabling of its bus master capability on the PCI Bus.
1	**Memory Access Enable (MAE):** 1=Enable PCI master access to main memory, if the PCI address selects enabled DRAM space; 0=Disable (TXC does not respond to main memory accesses).
0	**I/O Access Enable (IOAE): (Not Implemented)** This bit is hardwired to 0. The TXC does not respond to PCI I/O cycles.

3.2.5. PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h
Default Value: 0200h
Access: Read Only, Read/Write Clear

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort. PCISTS also indicates the DEVSEL# timing that has been set by the TXC hardware. Bits [15:12,8] are read/write clear and bits [10:9] are read only.

Bit	Descriptions
15	**Detected Parity Error (DPE): (Not Implemented)** This bit is hardwired to 0.
14	**Signaled System Error (SSE)—R/WC:** This bit is set to a 1 whenever the TXC signals an SERR#.
13	**Received Master Abort Status (RMAS)—R/WC:** When the TXC terminates a Host-to-PCI transaction (TXC is a PCI master) with an unexpected master abort, this bit is set to 1. Note that master abort is the normal and expected termination of PCI special cycles. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS)—R/WC:** When a TXC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. Software resets RTAS to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS):** This bit is hardwired to 0, as the TXC never terminates a PCI cycle with a target abort.
10:9	**DEVSEL# Timing (DEVT)—RO:** This 2-bit field indicates the timing of the DEVSEL# signal when the TXC responds as a target, and is hard-wired to the value 01b (medium) to indicate the slowest time that DEVSEL# is generated.
8	**Data Parity Detected (DPD):** This bit is hardwired to 0.
7	**Fast Back-to-Back (FB2B): (Not Implemented)** This bit is hardwired to 0.
6	**User Defined Format (UDF): (Not Implemented)** This bit is hardwired to 0. The TXC does not contain any configurations that depend on the environment, such as network frequencies.
5	**66 MHz PCI Capable (66C): (Not Implemented)** This bit is hardwired to 0. The TXC does not interface to 66 MHz PCI.
4:0	**Reserved.**

3.2.6. RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: Refer to product stepping information
Access: Read Only

This register contains the revision number of the TXC. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number:** This is an 8-bit value that indicates the revision identification number for the TXC.

Bit	Description
	A0 Stepping=00 A1 Stepping=01 A2 Stepping=02 A3 Stepping=03

3.2.7. CLASSC—CLASS CODE REGISTER

Address Offset: 09–0Bh
Default Value: 060000h
Access: Read Only

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the TXC. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Description
7:0	**Programming Interface (PI):** 00h=No register-level programming interface defined.
18:8	**Sub-Class Code (SCC):** 00h=Host Bridge.
23:16	**Base Class Code (BASEC):** 06=Bridge device.

3.2.8. MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write

MLT is an 8-bit register that controls the amount of time the TXC, as a bus master, can burst data on the PCI Bus. The Count Value is an 8-bit quantity. However, MLT[2:0] are hardwired to 0. MLT is used to guarantee the host CPU a minimum amount of the system resources.

Bit	Description
7:3	**Master Latency Timer Count Value.** The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allotted to the TXC, after which it must surrender the bus as soon as other PCI masters request the bus. The default value of MLT is 00h or 0 PCI clocks.
2:0	**Reserved.**

3.2.9. HEADT—HEADER TYPE REGISTER

Address Offset: 0Eh
Default Value: 00h
Access: Read Only

This register contains the Header Type of the TXC. This code is 00h indicating that the TXC's configuration space map follows the basic format. This register is read only.

Bit	Description
7:0	**Header Type (HTYPE):** 00h=Basic configuration space format.

3.2.10. BIST—BIST REGISTER

Address Offset: 0Fh
Default Value: 00h
Access: Read/Write

The Built In Self Test (BIST) function is not supported by the TXC. Writes to this register have no affect.

Bit	Descriptions
7	**BIST Supported:** This read only bit is always set to 0, disabling the BIST function. Writes to this bit position have no effect.
6	**Start BIST:** This function is not supported and writes have no effect.
5:4	**Reserved.**
3:0	**Completion Code:** This read only field always returns 0 when read and writes have no effect.

3.2.11. ACON—ARBITRATION CONTROL

Address Offset: 4Fh
Default Value: 00h
Access: Read/Write
Size: 8 bits

The ACON register enables and disables features related to the PCI arbitration and PCI 2.1 compliance.

Bit	Descriptions
7	**Extended CPU-toPIIX PHLDA# Signalling Enable (XPLDE):** When XPLDE = '1', the TXC adds the following additional signalling to signal PHLDA# (ie. In addition to the normal CPU/PIIX PHOLD/PHLDA# protocol); 1) Whenever the TXC begins a PCI read/write transation, it will assert PHLDA# for 1 PCLK within the address phase of the transaction. 2) If the CPU is attempting a LOCKed cycle AND LOCK has been established (ie. PLOCK# was seen deasserted in address phase), the PHLDA# remains asserted for one additional clock following the address phase.
6:3	**Reserved**

Bit	Descriptions
2	**Enable Retry on First Transfer Disable (ERFD):** When ERFD=0 and GT2E=1, the TXC will retry a PCI cycle when the latency to the first data transfer is about to exceed 32 PCI clocks. When ERFD=1 or GT2E=0, the TXC will complete the first data transfer regardless of latency. This bit should be set to 0 for normal operation unless ECC is enabled, in which case this bit should be set to 1.
1:0	**Reserved.**

3.2.12. PCON—PCI CONTROL

Address Offset: 50h
Default Value: 00h
Access: Read/Write

The PCON register enables and disables features related to the PCI unit operation not already covered in the PCI required configuration space.

Bit	Descriptions
7	**DRAM ECC/Parity Select (DEPS).** 1=ECC. 0=Parity (default). Note that this bit also adjusts the DRAM timings as documented in the DRAM section to account for the ECC operation.
6	**ECC TEST Enable (ETE).** 1=ECC Test Mode. 0=Normal mode (default). When set, The TXC handles subsequent cycles to DRAM.
5	**Shutdown to Port 92 (SP92).** When SP92=0, the TXC forwards a Shutdown special cycle from the host bus to PCI. When SP92=1, the TXC writes 01h to I/O address 92 on PCI in response to a Shutdown special cycle on the host bus.
4	**Dual Processor NA# Enable (DPNAE).** When DPNAE=0, the 82430FX PCIset NA# policies are used. When DPNAE=1, the NA# assertion policies are modified to prevent deadlocks in dual-processor PCI 2.1 systems. DPNAE should be correctly set by BIOS prior to the L1 cache being enabled.
3	**Peer Concurrency Enable (PCE).** When PCE=1, the CPU will be allowed to run DRAM/L2 cycles when non-PHLD PCI masters are running non-locked cycles targeting PCI peer devices. CPU-to-PCI cycles will be blocked (BRDY# stalled) during these peer cycles. When PCE=0, the CPU will be held off the bus during PCI peer cycles. This bit should be set to 1 for normal operation.
2	**SERR# Output Type (SOT).** 1=SERR# is a normal output actively driven high when negated. 0(default)=SERR# is an open drain output, compatible to the PCI SERR# signal. Note that SOT should not be programmed to a 1 if SERR# is connected to the PCI bus. SOT should only be programmed to a 1 in systems where SERR# is used as a sideband error signal (e.g. in ECC systems).
1	**Reserved.**
0	**Global TXC Enable (GTE).** This bit must be set to 1 to enable all new 82439HX features.

3.2.13. CC—CACHE CONTROL REGISTER

Address Offset: 52h
Default Value: SSSS0010 (S = Strapping option)
Access: Read/Write

This 8-bit register defines the secondary cache operations. The CC register enables and disables the second level cache, adjusts cache size, selects the cache write policy, selects the caching policy when CACHE# is negated on reads, informs the TXC how the SRAMs are connected, and defines the cache SRAM type. After a hard reset, CC[7:4] reflect the signal levels on the Host address lines A[31:28].

Bit	Description
7:6	**Secondary Cache Size (SCS):** This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the RESET signal. The default value can be overwritten with subsequent writes to the CC register. The options are: **Bits[7:6] Secondary Cache Size** 0 0 Cache not populated 0 1 256 Kbytes 1 0 512 Kbytes 1 1 Reserved **NOTE** 1. When SCS=00, the secondary cache is disabled. 2. To enable the L2 cache, SCS must be non-zero and the FLCE bit must be 1.
5:4	**SRAM Type (SRAMT):** This field reflects the inverted signal level on the A[29:28] pins at the rising edge of the RESET signal. The RESET values can be overwritten with subsequent writes to the CC register. The options are: **Bits[5:4] SRAM Type** 0 0 One bank of Pipelined Burst 0 1 Reserved 1 0 Reserved 1 1 Two banks of Pipelined Burst
3	**NA Disable (NAD):** When NAD=1, the TXC's NA# pin is never asserted. When NAD=0, NA# assertion is dependent on the cache type and size selected (via SRAMT, SCS). Note that NAD must be set to 1 if the NA pin of the TXC is not connected to the processor. This bit should be set to 0 for normal operation in systems that connect NA# to the processor.
2	**Extended Cacheability Enable (ECE).** 1=512-Mbyte limit (TIO[10:8] lines are enabled). 0=64-Mbyte limit (TIO[10:8] are disabled).
1	**Secondary Cache Force Miss or Invalidate (SCFMI):** When SCFMI=1, the L2 hit/miss detection is disabled, and all tag lookups result in a miss. If the L2 is enabled, the cycle is processed as a miss. If the L2 is populated but disabled (FLCE=0), then when SCFMI is set to a 1, any CPU read cycle will invalidate the selected tag entry. When SCFMI=0, normal L2 cache hit/miss detection and cycle processing occurs. Software can flush the cache (cause all modified lines to be written back to DRAM) by setting SCFMI to a 1 with L2 enabled (non-zero SCS, FLCE=1) immediately after reading twice the size of the L2. **NOTE** For a 512-Kbyte cache, software must read 1 Mbyte of non-overlapping, cacheable 512-Kbyte regions from the memory before setting the SCFMI bit.

Bit	Description
0	**First Level Cache Enable (FLCE):** FLCE enables/disables the first level cache. When FLCE=1, the TXC responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE=0, KEN# is always negated and new cache line fills to either the first level or second level cache are prevented. Note that, when FLCE=1 and SCFMI=1, writes to the cache are also forced as misses. Thus, it is possible to create incoherent data between main memory and the L2 cache. A summary of FLCE/SCFMI bit interactions is as follows: **FLCE SCFMI L2 Cache Result** 0 0 Disabled 0 1 Disabled; tag invalidate on reads 1 0 Normal L2 cache operation (dependent on SCS) 1 1 Enabled; miss forced on reads/writes

3.2.14. DRAMEC—DRAM EXTENDED CONTROL REGISTER

Address Offset: 56h
Default Value: 00h
Access: Read/Write

This 8-bit register contains additional controls for main memory DRAM operating modes and features.

Bit	Descriptions
7:5	**Reserved.**
4	**Speculative Leadoff Enable (SLE).** When SLE=1, the DRAM controller read request is presented before the final memory target (cache/DRAM/PCI) has been decoded by the TXC. This results in a 1 HCLK pull-in for all read leadoff latencies. Note that if the cycle does not actually target DRAM, the DRAM cycle is later terminated.
3	**Turn-around Insertion Enable (TIEN):** When TIEN=1, the TXC inserts one extra clock of turn-around on the MD lines after asserting MWE# before enabling the TXC MD buffers. When TIEN = 0, the TXC controls back-to-back DRAM cycles just like the 82430FX PCIset.
2:1	**Memory Address Drive Strength (MAD):** This field controls the strength of the output buffers driving the MA and MWE# pins. **Bit 2 Bit 1 MAA[1:0]/MAB[1:0] MA[11:2]/MWE#** 0 0 8 mA 8 mA 0 1 8 mA 12 mA 1 0 12 mA 8 mA 1 1 12 mA 12 mA
0	**64 Mbit Mode Enable (64ME):** When 64ME=1, the 64 Mbit density SIMMs are support by changing the MA address mux selection on row bit 11. Refer to the DRAM Interface section for more details.

3.2.15. DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h
Default Value: 01h
Access: Read/Write

This 8-bit register controls main memory DRAM operating modes and features.

Bit	Description
7:6	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. CPU cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole are ignored by the TXC (no DEVSEL#). Note that a selected hole is not remapped. **Bits[7:6] — Hole Enabled** 00 — None 01 — 512 Kbytes – 640 Kbytes 10 — 15 - 16 Mbytes 11 — Reserved
5:4	**Reserved.**
3	**EDO Detect Mode Enable (EDME):** This bit, if set to a 1, enables a special timing mode for BIOS to detect EDO DRAM type on a bank-by-bank basis. Once all DRAM row banks have been tested for EDO, the EDME bit should be set to 0. Otherwise, performance will be seriously impacted.
2:0	**DRAM Refresh Rate (DRR):** The DRAM refresh rate is adjusted according to the frequency selected by this field. Note that refresh is also disabled via this field, and that disabling refresh results in the eventual loss of DRAM data. **Bits[2:0] — Host Bus Frequency** 000 — Refresh Disabled 001 — 50 MHz 010 — 60 MHz 011 — 66 MHz 1XX — Reserved DRR0 is initialized to the inverted signal level on A27 at the rising edge of reset. A jumpered pull-up resistor option on A27 allows the BIOS to read DRR0 to determine 60 MHz bus operation. Otherwise, A27 should be externally pulled down for 66 MHz default. Subsequent writes to this field will override the reset strap value.

3.2.16. DRAMT—DRAM TIMING REGISTER

Address Offset: 58h
Default Value: 00h
Access: Read/Write

This 8-bit register controls main memory DRAM timings.

Systems that support ECC must set read and write burst rates to x333 or slower. Additionally, x222 timings are only supported for systems designed for up to 4 DRAM SIMMS and which do not use external MA buffers. Only 60ns, or faster EDO DRAMs will meet x222 EDO timings.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7</td><td>Turbo Read Leadoff (TRL): This bit, when set, enables bypass of the first input register in the DRAM data pipeline, resulting in a 1 HCLK pull-in of all read leadoff timings. TRL can only be set to 1 in a cacheless configuration.
NOTE
It is illegal to enable this feature if ERRCMD[1:0] is not 00.</td></tr>
<tr><td>6:5</td><td>DRAM Read Burst Timing (DRBT): The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower DRAMs. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register.
<table><tr><th>DRBT</th><th>EDO Burst Rate</th><th>Standard Page Mode Rate</th></tr><tr><td>00</td><td>x444</td><td>x444</td></tr><tr><td>01</td><td>x333</td><td>x444</td></tr><tr><td>10</td><td>x222</td><td>x333</td></tr><tr><td>11</td><td>Reserved</td><td>Reserved</td></tr></table></td></tr>
<tr><td>4:3</td><td>DRAM Write Burst Timing (DWBT): The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower DRAMs. Most system designs will be able to use one of the faster burst mode timings.
<table><tr><th>DWBT</th><th>Burst Rate</th></tr><tr><td>00</td><td>x444</td></tr><tr><td>01</td><td>x333</td></tr><tr><td>10</td><td>x222</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td></tr>
<tr><td>2</td><td>Fast RAS to CAS Delay (FRCD): The DRAM row miss leadoff timings are controlled by the FRCD bit. When FRCD=1, the RAS active to CAS active delay is 2 clocks. When FRCD=0, the timing is 3 host clocks. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower DRAMs. If DLT=x0, FRCD must be set to 0. If DLT=x1, either setting of FRCD is legal.</td></tr>
<tr><td>1:0</td><td>DRAM Leadoff Timing (DLT): The DRAM leadoff timings are controlled by the DLT bits. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower DRAMs. The page hit leadoff timings are summarized below: Page miss and bank miss timings are also affected (DLT controls the MA setup to the first CAS# assertion).
<table><tr><th>DLT</th><th>Read Leadoff</th><th>Write Leadoff</th><th>RAS# Precharge</th><th>Refresh RAS Assertion</th></tr><tr><td>00</td><td>7</td><td>6</td><td>3</td><td>4</td></tr><tr><td>01</td><td>6</td><td>5</td><td>3</td><td>4</td></tr><tr><td>10</td><td>7</td><td>6</td><td>4</td><td>5</td></tr><tr><td>11</td><td>6</td><td>5</td><td>4</td><td>5</td></tr></table>NOTES
1. The DLT field and the FRCD bit have cumulative affects (i.e., setting DLT0=0 and FRCD=0 results in two additional clocks between RAS# assertion and CAS# assertion).
2. The SLE and TRL fields have subtractive effects for reads only (i.e., setting SLE=1 and TRL=1 results in two less clocks from the read leadoff count).
3. If ECC is enabled, the combination of slow leadoffs (DLT=x0) and x222 write burst timings (DWBT=10) does not guarantee a 2-clock MWE# setup to CAS#. In all other cases, when DLT=x0, a 2-clock MWE# setup to CAS# is guaranteed.</td></tr>
</table>

3.2.17. PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: PAM0 (59h) — PAM6 (5Fh)
Default Value: 00h
Attribute: Read/Write

The TXC allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 640-Kbyte to 1-Mbyte address range. The PAM registers support these features. Three bits are used to specify L1 cacheability and memory attributes for each memory segment. These attributes are:

Read Enable (RE) When RE=1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE=0, the CPU read accesses are directed to PCI.

Write Enable (WE) When WE=1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE=0, the CPU write accesses are directed to PCI.

Cache Enable (CE) When CE=1, the corresponding memory segment is L1 cacheable. CE must not be set to 1 when RE is reset to 0 for any particular memory segment. When CE=1 and WE=0, the corresponding memory segment is cached in the first level cache only on CPU code read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Table 2. Attribute Definition

Read/Write Attribute	Definition
Read Only	Read cycles: CPU cycles are serviced by the DRAM in a normal manner. Write cycles: CPU initiated write cycles are ignored by the DRAM interface as well as the cache. Instead, the cycles are passed to PCI for termination. Areas marked as Read Only are L1 cacheable for Code accesses only. These regions are not cached in the second level cache.
Write Only	Read cycles: All read cycles are ignored by the DRAM interface as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. Write cycles: CPU write cycles are serviced by the DRAM and L2 cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by the DRAM and L2 cache interface.
Disabled	All read and write cycles to this area are ignored by the DRAM and cache interface. These cycles are forwarded to PCI for termination.

Each PAM register controls two regions, typically 16 Kbytes in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding.

PCI master access to DRAM space is also controlled by the PAM registers. If the PAM programming indicates a region is writeable, PCI master writes are accepted (DEVSEL# generated). If the PAM programming indicates a region is readable, PCI master reads are accepted. If a PCI write to a non-writeable DRAM region, or a PCI read to a non-readable DRAM region is seen, the TXC does not accept the cycle (DEVSEL# not asserted). PCI master accesses to enable memory hole regions are not accepted.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process the BIOS can be shadowed in main memory to increase the system performance. When a BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The CPU then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 3. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
	7,3	6,2	5,1	4,0			
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	CE	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

NOTES:
The CE bit should not be changed while the L2 cache is enabled.

DOS Application Area (00000–9FFFh)
Read, write, and cacheability attributes are always enabled and are not programmable for the 0–640-Kbyte DOS application region.

Video Buffer Area (A0000–BFFFFh)
This 128-Kbyte area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable.

Expansion Area (C0000–DFFFFh)
This 128-Kbyte area is divided into eight 16-Kbyte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled Memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000–EFFFFh)
This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000–FFFFFh)
This area is a single 64-Kbyte segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

Extended Memory Area (100000–FFFFFFFFh)
The extended memory area can be split into several parts;

- Flash BIOS area from 4 Gbytes to 4 Gbytes – 512 Kbytes (aliased on ISA at 16 Mbyte – 15.5 Mbyte)
- DRAM Memory from 1 Mbyte to a maximum of 512 Mbytes
- PCI Memory space from the top of DRAM to 4 Gbytes – 512 Kbyte

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 Gbyte to 4 Gbyte minus 512 Kbyte. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4-Gbyte range, the request is directed to PCI.

The DRAM memory space can occupy extended memory from a minimum of 1 Mbyte up to 512 Mbytes. This memory is cacheable.

PCI memory space from the top of main memory to 4 Gbytes is always non-cacheable.

3.2.18. DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: DRB0 (60h) — DRB7 (67h)
Default Value: 02h
Access: Read/Write

The TXC supports 8 rows of DRAM. Each row is 64 bits wide. The DRAM Row Boundary registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 4-Mbyte granularity.

DRB0 = Total amount of memory in row 0 (in 4 Mbytes)
DRB1 = Total amount of memory in row 0 + row 1 (in 4 Mbytes)
DRB2 = Total amount of memory in row 0 + row 1 + row 2 (in 4 Mbytes)
DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 4 Mbytes)
DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in 4 Mbytes)
etc ...

The DRAM array can be configured with 512 K , 1 M, 4 M, or 16 M deep by 32 or 36-bit wide SIMMs. Each register defines an address range that causes a particular RAS# line to be asserted (e.g., if the first DRAM row is 8 Mbytes in size, accesses within the 0 to 8-Mbyte range cause RAS0# to be asserted). The DRB registers are programmed with an 8-bit upper address limit value. This upper address limit is compared to A[29:22] of the Host address bus, for each row, to determine if DRAM is being targeted.

Bit	Description
7:0	**Row Boundary Address:** This 8-bit value is compared against address lines A[29:22] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB = row size).

Row Boundary Address

These 8-bit values represent the upper address limits of the 8 rows (i.e., this row minus previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). DRB7 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB7. If DRB7 is greater than 512 Mbytes, then 512 Mbytes of DRAM are available.

As an example of a general purpose configuration where 4 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured as shown in Figure 2. In this configuration, the TXC drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are

populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.

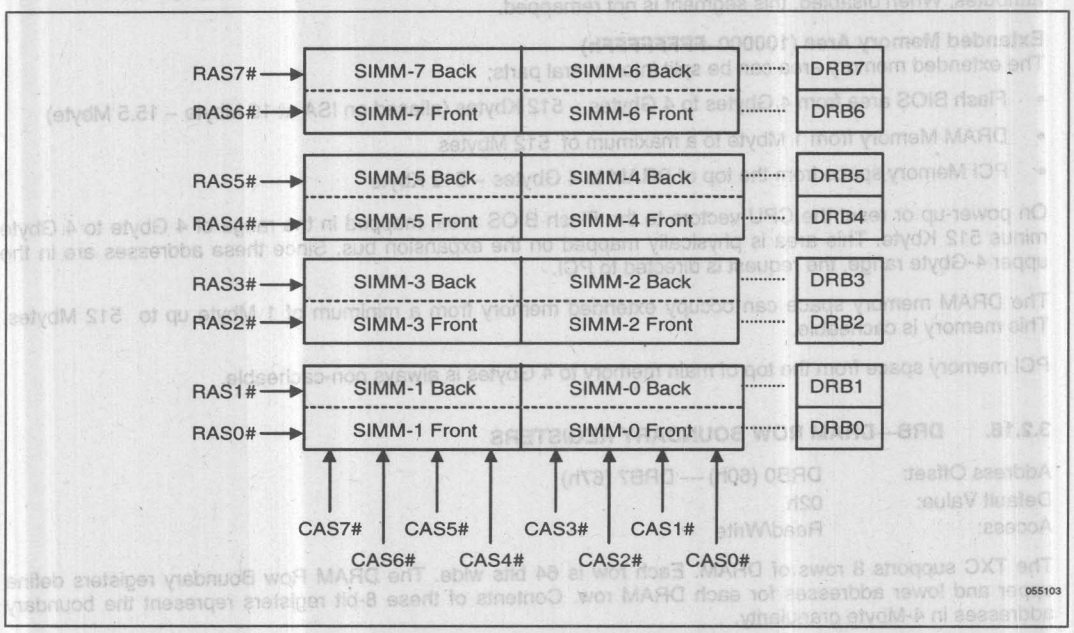


Figure 2. SIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of four 8-byte or eight 4-byte SIMM sockets.

Example #1
The memory array is populated with four single-sided 1MB x 32 SIMMs, a total of 16 Mbytes of DRAM. Two SIMMs are required for each populated row making each populated row 8 Mbytes in size.

DRB0 = 02h	populated (2 SIMMs, 8 Mbytes this row)
DRB1 = 02h	empty row
DRB2 = 04h	populated (2 SIMMs, 8 Mbytes this row)
DRB3 = 04h	empty row
DRB4 = 04h	empty row
DRB5 = 04h	empty row
DRB6 = 04h	empty row
DRB7 = 04h	empty row

3.2.19. DRT—DRAM ROW TYPE REGISTER

Address Offset: 68h
Default Value: 00h
Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO or page mode) used in each row, and should be programmed by BIOS for optimum performance if EDO DRAMs are used. The hardware uses these bits to determine the correct cycle timing to use before a DRAM cycle is run.

Bit	Description
7:0	**DRAM Row Type (DRT):** Each bit in this register corresponds to the DRAM row identified by the corresponding DRB register. When the DRT bit for a DRB register is programmed to a 0, then page mode DRAM timings are used for that bank. If the DRT bit for a DRB register is programmed to a 1, then EDO DRAM timings are used for that bank. DRT[0] corresponds to row 0, DRT[1] to row 1, etc.

3.2.20. SMRAM—SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 72h
Default Value: 02h
Access: Read/Write

The System Management RAM Control register controls how accesses to this space are treated. The Open, Close, and Lock SMRAM Space bits function only when the SMRAM enable bit is set to a 1. Also, the OPEN bit should be reset before the LOCK bit is set.

Bit	Description
7	**Reserved.**
6	**SMM Space Open (DOPEN):** When DOPEN=1 and DLCK=0 SMM space DRAM is made visible even when SMIACT# is negated. This is intended to help BIOS initialize SMM space. Software should ensure that DOPEN=1 is mutually exclusive with DCLS=1. When DLCK is set to a 1, DOPEN is reset to 0 and becomes read only.

Bit	Description
5	**SMM Space Closed (DCLS):** When DCLS=1, SMM space DRAM is not accessible to data references, even if SMIACT# is asserted. Code references may still access SMM space DRAM. This allows SMM software to reference "through" SMM space to update the display even when SMM space is mapped over the VGA range. Software should ensure that DOPEN=1 is mutually exclusive with DCLS=1.
4	**SMM Space Locked (DLCK):** When DLCK is set to 1, DOPEN is reset to 0 and both DLCK and DOPEN become read only. DLCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of DLCK and DOPEN provide convenience with security. The BIOS can use the DOPEN function to initialize SMM space and then use DLCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the DOPEN function.
3	**SMRAM Enable (SMRAME):** If set to a 1, the SMRAM function is enabled, providing 128 Kbytes of DRAM accessible at the A0000h address while in SMM (ADS# with SMIACT#). Refer to the section on SMM for more details.
2:0	**SMM Space Base Segment (DBASESEG):** This field programs the location of SMM space. "SMM DRAM" is not remapped. It is simply "made visible" if the conditions are right to access SMM space, otherwise the access is forwarded to PCI. DBASESEG = 010 is the only allowable setting, which selects the SMM space as A0000–BFFFFh. All other values are reserved. PCI initiators are not allowed access to SMM space.

Table 5 summarizes the operation of SMRAM space cycles targeting SMI space addresses (A-segment):

Table 4. SMRAM Space Cycles

SMRAME	DLCK	DCLS	DOPEN	SMIACT#	Code Fetch	Data Reference
0	X	X	X	X	PCI	PCI
1	0	0	0	0	DRAM	DRAM
1	0	X	0	1	PCI	PCI
1	0	0	1	X	DRAM	DRAM
1	0	1	0	0	DRAM	PCI
1	0	1	1	X	INVALID	INVALID
1	1	0	X	0	DRAM	DRAM
1	1	X	X	1	PCI	PCI
1	1	1	X	0	DRAM	PCI

3.2.21. ERRCMD—ERROR COMMAND REGISTER

Address Offset: 90h
Default Value: 00h
Access: Read/Write

This 8-bit register controls the operation of the Error Detection and Correction feature.

Bit	Description
7	**SERR# Duration (SED).** This bit determines the duration that SERR# is asserted when the TXC signals an error. The TXC signals an error if PCICMD[SERRE]=1 and ERRCMD[SMUE]=1 when an uncorrectable ECC or parity error is detected, or PCICMD[SERRE]=1 and ERRCMD[SSCE]=1 when a correctable ECC error is detected, or PCICMD[SERRE]=1 and ERRCMD[SMUE]=1 when a correctable ECC error is detected. When SED=0 and the conditions above are met, SERR# is asserted for 1 PCI clock. This setting, also referred to as pulse mode, is used to report memory errors via NMI. When SED=1, once SERR# becomes asserted, it will remain asserted until the error flags (MEF, SET) with a respective enable set (SMUE, SSCE) are cleared (i.e., MEF*SMUE + SEF*SSCE=0). This setting, also referred to as level mode, is used to report memory errors via an SMI event or APIC interrupt. Note that the SED setting does not affect software-generated error signaling that is always a pulse mode (see MEF description). This bit should be programmed to the same value as PCON[SOT, bit 2}.
6:3	**Reserved.**
2	**Bad PAR on Multiple-Bit Uncorrectable Error (BPARE).** When BPARE=1, the TXC forces incorrect PCI parity on PCI read data starting from the time that an uncorrectable DRAM read error occurs (either a multi-bit ECC or parity error) during a PCI read cycle until the end of that current cycle. Subsequent PCI read cycles will have correct parity presented. Note that it is the uncorrectable read *event* that begins the bad parity forcing, *not* the state of the MEF flag. Also, bad parity is immediately delivered to PCI, even if the error event occurs during a read prefetch for data that the PCI master may ultimately not request in that cycle. *For systems not supporting either ECC or parity, this bit must be set to 0.*
1	**SERR# on Multiple-Bit Uncorrectable Error (SMUE).** When SMUE=1, the TXC asserts SERR# when it detects a multi-bit ECC or parity error. When SMUE=0, the TXC does not assert SERR# on multi-bit or parity errors. The SERR# Enable bit (SERRE) in the PCICMD register must also be set to signal the SERR#. *For systems not supporting either ECC or parity, this bit must be set to 0.*
0	**SERR# on Single-Bit Correctable Error (SSCE).** When SSCE=1, the TXC asserts SERR# when it detects a single-bit ECC error. When SSCE=0, the TXC will not assert SERR# on single-bit errors. The SERR# Enable bit (SERRE) in the PCICMD register must also be set to signal the SERR#.

Table 5 shows the SED and SOT configurations:

Table 5. SED/SOT Configurations

SED	SOT	System Configuration
0	0	SERR# output connected to PCI, DRAM errors signaled via NMI.
0	1	Reserved
1	0	Reserved
1	1	SERR# output connected to external logic, DRAM errors signaled via SMI.

3.2.22. ERRSTS—ERROR STATUS REGISTER

Address Offset: 91h
Default Value: 00h
Access: Read Only / Read Write Clear

This 8-bit register contains status of the operation of the Error Detection and Correction feature.

Bit	Description
7:5	**Multi-Bit First Row Error (MBFRE)** This field is the encoded value of the DRAM row associated with the multi-bit error. When an error is detected, this field is updated and the MEF bit is set. This field will be locked (no further updates) until the MEF flag has been reset. When MEF=0, the value in this field is undefined.
4	**Multi-Bit (uncorrectable) Error Flag (MEF).** The TXC sets this bit to 1 when an uncorrectable multi-bit errors is detected with ECC enabled. If SERR# signaling is enabled by the ERRCMD[SMUE] bit, and PCICMD[SERRE] is set, then the error is reported via the SERR# pin. SERR# must be disabled, by setting PCICMD[SERRE]='0' before any write to the ERRSTS register except the ones which are done for the explicit purpose of generating a SERR#. Before any write to the ERRSTS register, the MEF and SEF bits must be checked, since any write to this register will clear these bits. For example, when software is writing to the ERRSTS register for clearing SEF or MEF bits, SERR# should be disabled. In systems which use SMI# for reporting ECC errors, when SERR# is asserted due to an uncorrectable error, the SMI routine should do the following sequence: 1. Read the ECC error flags (MEF, SEF) to determine that an uncorrectable error has occurred. 2. Disable SERR# by setting PCICMD [SERRE]='0'. 3. Clear MEF bit by writing '1' to it. 4. Enable SERR# again. 5. Write '1' to MEF bit to create an NMI event.
3:1	**Single-Bit First Row Error (SBFRE)** This field is the encoded value of the DRAM row associated with the first single bit error. When an error is detected, this field is updated and the SEF bit is set. This field will be locked (no further updates) until the SEF flag has been reset. When SEF=0, the value in this field is undefined.

Access: Read Only

This register contains the latest non-zero error syndrome, associated with the error row identified by either the MBFRE or SBFRE fields.

Bit	Description
7:0	**Error Syndrome.** When ECC is enabled, bits 7:0 contain the latest non-zero error syndrome. The error syndrome remains latched until software unlocks the respective field by clearing either the MEF or SEF bit. Multi-bit errors take priority over single-bit errors, so that if both MEF and SEF are signaled, the syndrome will be the one associated with the multi-bit error (MBFRE). In parity mode, this contents of this register are undefined. Writes to ERRSYN have no effect.

4.0. FUNCTIONAL DESCRIPTION

This section provides a functional description of the TXC including the Host bus interface, PCI bus interface, DRAM interface, L2 cache interface, PCI bus arbitration, and clock generation.

4.1. Host Interface

The Host Interface of the TXC is designed to support the Pentium processor. The host interface of the TXC supports 50 MHz, 60 MHz, and 66 MHz bus speeds. The TXC also supports the Pentium processors's dual processing mode. The TXC supports the Pentium processor with a full 64-bit data bus, 32-bit address bus, and associated internal write-back cache logic. Host bus addresses are decoded by the TXC for accesses to main memory, PCI memory, and PCI I/O. The TXC also supports the pipelined addressing capability of the Pentium processor.

4.2. PCI Interface

The TXC is fully compliant to the PCI 2.1 Specification. The TXC integrates a high performance interface to the PCI local bus taking full advantage of the high bandwidth and low latency of the PCI. Five PCI masters are supported by the integrated arbiter including four general purpose PCI masters and an optimized arbitration for the PCI-to-ISA bridge. The PCI-to-ISA bridge arbitration dynamically allocates bandwidth to PIIX3 to optimize system latencies for superior Universal Serial Bus (USB) performance.

TXC enhances the basic snoop protocol by allowing pipelining of snoops between two PCI cycles. Thus, more efficient back-to-back frames are possible, especially for short burst cycles.

The PCI interface does not assert PLOCK# on a write cycle, unless PLOCK# was already properly established by a prior read (i.e., read completed without a retry). If a locked cycle is initiated to a read-only PAM region, the cycle is handled on the host bus as a locked cycle, and the write propagates to PCI as a normal, unlocked, write cycle.

4.3. Secondary Cache Interface

The TXC integrates a high performance write-back second level cache controller using internal/external tags and provides a full first level and second level cache coherency mechanism. The second level cache is direct mapped, non-sectored, and supports a write-back cache policy. Cache lines are allocated on read misses (no write allocate).

The second level cache can be configured to support either a 256-Kbyte or 512-Kbyte cache using synchronous pipelined burst SRAMs. (Note that the TXC does not support asynchronous or burst SRAMs for the cache memory.) For a 256-Kbyte configuration, an 8kx8 standard SRAM is used to store the tags (64-Mbyte memory space cacheability limit). For the 512-Kbyte configuration, a 16kx8 standard SRAM is used to store the tags and the valid bits tags (64-Mbyte memory space cacheability limit). The TXC also supports an optional extended memory space cacheability limit of 512 Mbytes.

A second level cache line is 32 Bytes wide. In the 256-Kbyte configurations, the second level cache contains 8k lines, while the 512-Kbyte configurations contain 16k lines. Valid and modified status bits are kept on a per-line basis. Cacheability of the entire memory space in first level cache is supported. The memory space cacheability for the secondary cache is either 64 Mbytes or 512 Mbytes of main memory, depending on the programming of the ECE bit in the CC register. Table 6 shows the tag sizes needed to support different sizes of cacheability. Only main memory controlled by the TXC DRAM interface is cached. PCI memory is not cached.

Table 6. Cacheability

Cache Size	Tag Size	Cacheability
256 Kbyte	8K by 8 bits	64 Mbyte
256 Kbyte	8K by 9 bits	128 Mbyte
256 Kbyte	8K by 10 bits	256 Mbyte
256 Kbyte	8K by 11 bits	512 Mbyte
512 Kbyte	16K by 8 bits (including valid bit)	64 Mbyte
512 Kbyte	16K by 9 bits (including valid bit)	128 Mbyte
512 Kbyte	16K by 10 bits (including valid bit)	256 Mbyte
512 Kbyte	16K by 11 bits (including valid bit)	512 Mbyte

Table 7 shows the different standard SRAM access time requirements for different host clock frequencies.

Table 7. SRAM Access Time Requirements

Host Clock Frequency (MHz)	Pipelined Burst Clock-to-Output Access Time (ns)	Tag RAM Cycle Time (ns)
50	13.5	20
60	10	15
66	8.5	15

4.3.1. CLOCK LATENCIES

Table 8 lists the latencies for various processor transfers to/from the second level cache.

Table 8. Second Level Cache Latencies with Pipelined Burst SRAM

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write (write back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1, 1-1-1-1 (note 1)
Pipelined Back-to-Back Burst Reads (dual bank)	3-1-1-1, 2-1-1-1 (note 1)

NOTES:

1. The back-to-back cycles do not account for CPU idle clocks between cycles.

4.3.2. SNOOP CYCLES

The snoop (i.e., inquire) cycle is used to probe the first level and second level caches when a PCI master attempts to access main memory. This is done in order to maintain coherency between the first and second level caches and main memory. Each cache line accessed during PCI master DRAM transfers is snooped by the TXC.

To maintain optimum PCI bandwidth to DRAM, the TXC utilizes a "snoop ahead" algorithm. Once the snoop for the first cache line of a transfer has completed, the TXC will automatically snoop the next sequential cache line. This snoop ahead policy eliminates most data stall delays while waiting for snoop results.

Reads

When a write-back occurs due to a PCI read cycle snoop, the resulting write-back data is returned to the merge buffer. Data from the merge buffer is then returned directly to PCI, eliminating the delay to perform the write-back to DRAM and a subsequent DRAM read before returning valid data to PCI.

Writes

When a write-back occurs due to a PCI write cycle snoop, the resulting write-back data is merged with the incoming PCI write data. The PCI data will not stall while waiting for a write-back to complete unless there is no space in the merge buffer for the write-back data.

4.3.3. CACHE ORGANIZATION

Figure 3 and Figure 4 show the connections between the TXC and the external tag RAM and data SRAM.

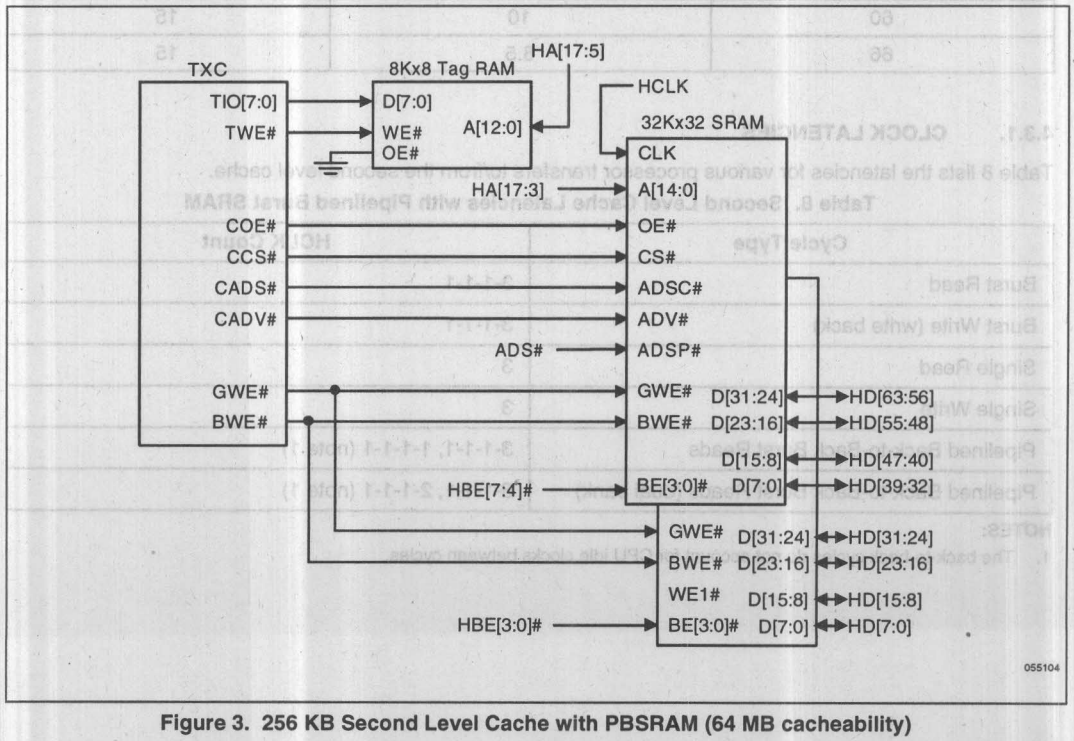


Figure 3. 256 KB Second Level Cache with PBSRAM (64 MB cacheability)

4.3.4. DRAM CACHE

TXC supports DRAM cache. The TIO[10] pin has to be pulled up for DRAM cache. Extended cache and DRAM cache are mutually exclusive.

For single processor systems using a DRAM cache, register 51, bit 5 in the 82439HX should be set to a 1. For dual processor systems using a DRAM cache and using the cC0 (or later) stepping of the Pentium® processor, this bit should also be set to a 1. For dual processor systems using earlier steppings of the Pentium® processor, the DRAM cache is not supported.

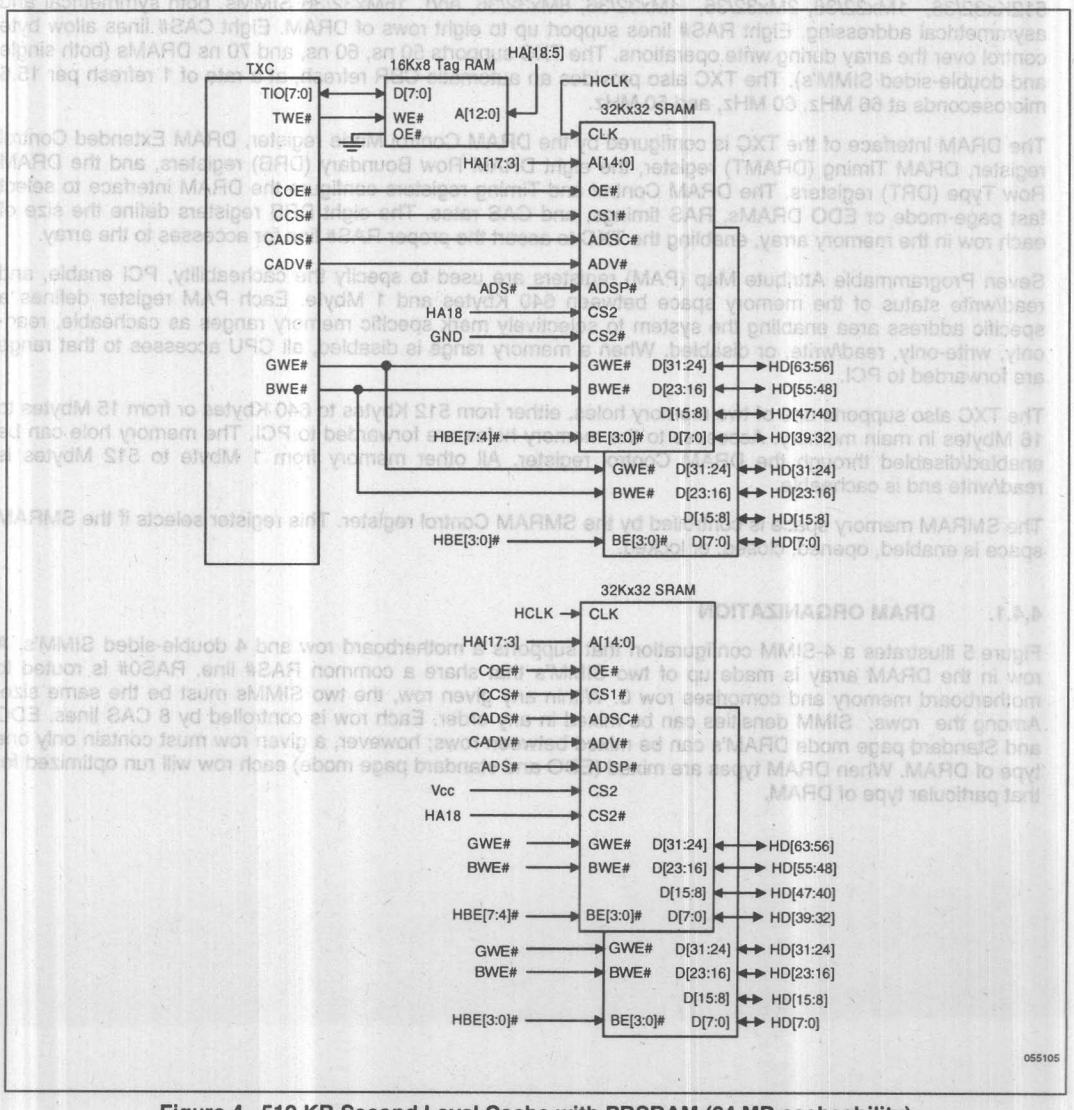


Figure 4. 512 KB Second Level Cache with PBSRAM (64 MB cacheability)

4.4. DRAM Interface

The TXC integrates a DRAM controller that supports a 64-bit memory array and main memory sizes from 4 Mbytes to 512 Mbytes. The TXC generates all control signals (such as RAS#, CAS#, WE# (using MWE#)) and multiplexed addresses for the DRAM array. The address and data flows through the TXC for all DRAM accesses.

The TXC supports industry standard 32- and 36-bit wide memory modules with fast page-mode DRAMs and supports EDO (Extended Data Out) DRAMs. Twelve multiplexed address lines (MA[11:0]) support 512Kx32/36, 1Mx32/36, 2Mx32/36, 4Mx32/36, 8Mx32/36, and 16Mx32/36 SIMMs, both symmetrical and asymmetrical addressing. Eight RAS# lines support up to eight rows of DRAM. Eight CAS# lines allow byte control over the array during write operations. The TXC supports 50 ns, 60 ns, and 70 ns DRAMs (both single and double-sided SIMM's). The TXC also provides an automatic CBR refresh, at a rate of 1 refresh per 15.6 microseconds at 66 MHz, 60 MHz, and 50 MHz.

The DRAM interface of the TXC is configured by the DRAM Control Mode register, DRAM Extended Control register, DRAM Timing (DRAMT) register, the eight DRAM Row Boundary (DRB) registers, and the DRAM Row Type (DRT) registers. The DRAM Control and Timing registers configure the DRAM interface to select fast page-mode or EDO DRAMs, RAS timings, and CAS rates. The eight DRB registers define the size of each row in the memory array, enabling the TXC to assert the proper RAS# line for accesses to the array.

Seven Programmable Attribute Map (PAM) registers are used to specify the cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbyte. Each PAM register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read-only, write-only, read/write, or disabled. When a memory range is disabled, all CPU accesses to that range are forwarded to PCI.

The TXC also supports one of two memory holes, either from 512 Kbytes to 640 Kbytes or from 15 Mbytes to 16 Mbytes in main memory. Accesses to the memory holes are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control register. All other memory from 1 Mbyte to 512 Mbytes is read/write and is cacheable.

The SMRAM memory space is controlled by the SMRAM Control register. This register selects if the SMRAM space is enabled, opened, closed, or locked.

4.4.1. DRAM ORGANIZATION

Figure 5 illustrates a 4-SIMM configuration that supports a motherboard row and 4 double-sided SIMM's. A row in the DRAM array is made up of two SIMM's that share a common RAS# line. RAS0# is routed to motherboard memory and comprises row 0. Within any given row, the two SIMMs must be the same size. Among the rows, SIMM densities can be mixed in any order. Each row is controlled by 8 CAS lines. EDO and Standard page mode DRAM's can be mixed between rows; however, a given row must contain only one type of DRAM. When DRAM types are mixed (EDO and standard page mode) each row will run optimized for that particular type of DRAM.

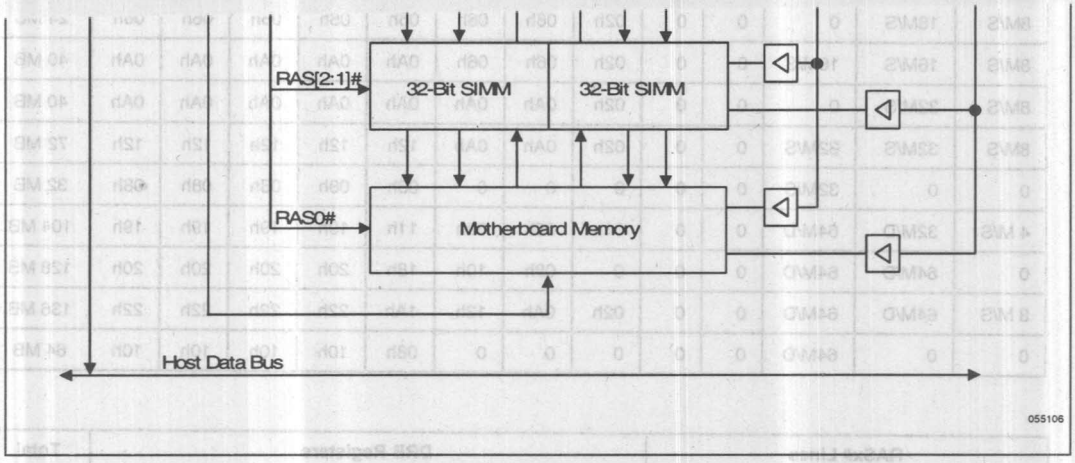


Figure 5. SIMM Socket

The fastest possible leadoff and burst times are easier to achieve by using a subset of the RAS# lines. Depending on the system layout, the DRAMEC[MAD] configuration field can be used to provide optimum address drive for a small number of rows.

Rules for Populating the Memory Array

The following rules apply to the SIMM configuration.

- SIMM sockets must be populated in pairs. The memory array is 64- or 72-bits wide.
- SIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).
- SIMM socket pairs need to be populated with the same densities. For example, SIMM sockets for RAS[2:1]# should be populated with identical densities. However, SIMM sockets for RAS[4:3]# can be populated with different densities than the SIMM socket pair for RAS[2:1]#.
- EDO and standard page mode can both be used. However, only one type should be used per SIMM socket pair. For example, in the table shown below SIMM sockets for RAS[2:1]# can be populated with EDOs while SIMM sockets for RAS[4:3]# can be populated with standard page mode. If different memory is used for different rows, each row will be optimized for that type of memory.
- The DRAM Timing register which provides the DRAM speed grade control for the entire memory array must be programmed to use the timings of the slowest DRAMs installed.

Table 9. Sample Of Possible Mix And Match Options For SIMMs

RASx# Lines					DRB Registers								Total
0	1,2	3,4	5,6	7	0	1	2	3	4	5	6	7	Mem
8M/S	0	0	0	0	02h	02h	02h	02h	02h	02h	02h	02h	8 MB
0	4M/S	0	0	0	0	01h	01h	01h	01h	01h	01h	01h	4 MB
0	0	8M/S	0	0	0	0	0	02h	02h	02h	02h	02h	8 MB
8M/S	8M/S	0	0	0	02h	04h	04h	04h	04h	04h	04h	04h	16 MB
4M/S	8M/S	8M/S	0	0	01h	03h	03h	05h	05h	05h	05h	05h	20 MB
8M/S	16M/S	0	0	0	02h	06h	06h	06h	06h	06h	06h	06h	24 MB
8M/S	16M/S	16M/S	0	0	02h	06h	06h	0Ah	0Ah	0Ah	0Ah	0Ah	40 MB
8M/S	32M/S	0	0	0	02h	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	40 MB
8M/S	32M/S	32M/S	0	0	02h	0Ah	0Ah	12h	12h	12h	12h	12h	72 MB
0	0	32M/S	0	0	0	0	0	08h	08h	08h	08h	08h	32 MB
4 M/S	32M/D	64M/D	0	0	01h	05h	09h	11h	19h	19h	19h	19h	104 MB
0	64M/D	64M/D	0	0	0	08h	10h	18h	20h	20h	20h	20h	128 MB
8 M/S	64M/D	64M/D	0	0	02h	0Ah	12h	1Ah	22h	22h	22h	22h	136 MB
0	0	64M/D	0	0	0	0	0	08h	10h	10h	10h	10h	64 MB

RASx# Lines				DRB Registers								Total
0,1	2,3	4,5	6,7	0	1	2	3	4	5	6	7	Mem
64M/D	64M/D	64M/D	64M/D	08h	10h	18h	20h	28h	30h	38h	40h	256 MB
64M/S	64M/S	64M/S	64M/S	10h	10h	20h	20h	30h	30h	40h	40h	256 MB
128M/D	128M/D	128M/D	128M/D	10h	20h	30h	40h	50h	60h	70h	80h	512 MB
128M/S	128M/S	128M/S	128M/S	20h	20h	40h	40h	60h	60h	80h	80h	512 MB

NOTES:

"S" denotes single-sided SIMM's, "D" denotes double-sided SIMM's.

Table 10 provides a summary of the characteristics of memory configurations supported by the TXC. Minimum values listed are obtained with single-sided SIMMs and maximum values are obtained with double-sided SIMMs. Note that for a 64-bit wide memory array, a minimum of two 32-/36-bit wide DRAM SIMM configuration is required. The minimum values used are also the smallest upgradeable memory size.

Table 10. Minimum (Upgradeable) and Maximum Memory Size for each configuration

DRAM Tech.	DRAM Density	DRAM Width	DRAM SIMM		DRAM Addressing	Address Size		DRAM Size	
			SS x32 or 36	DS x32 or 36		Row	Column	Min (UP)	Max
4M									
	512K	8	512K	1M	Asymmetric	10	9	4 MB	32 MB
	1M	4	1M	2M	Symmetric	10	10	8 MB	64 MB
16M									
	1M	16	1M	2M	Symmetric	10	10	8 MB	64 MB
	2M	8	2M	4M	Asymmetric	11	10	16 MB	128 MB
	4M	4	4M	8M	Symmetric	11	11	32 MB	256 MB
	4M	4	4M	8M	Asymmetric	12	10	32 MB	256 MB
64M									
	4M	16	4M	8M	Symmetric	11	11	32 MB	256 MB
	8M	8	8M	16M	Asymmetric	12	11	64 MB	512 MB
	16M	4	16M	32M	Symmetric	12	12	128 MB	512 MB

The memory organization (Figure 6) represents the maximum 512 Mbytes of address space. Accesses to memory space above top of DRAM, video buffer, or the memory gaps (if enabled) are forwarded to PCI, and these regions are not cacheable. Below 1 Mbyte, there are several memory segments that have selectable cacheability. None of the DRAM space occupied by the video buffer or the memory space gaps is remapped and is therefore "lost".

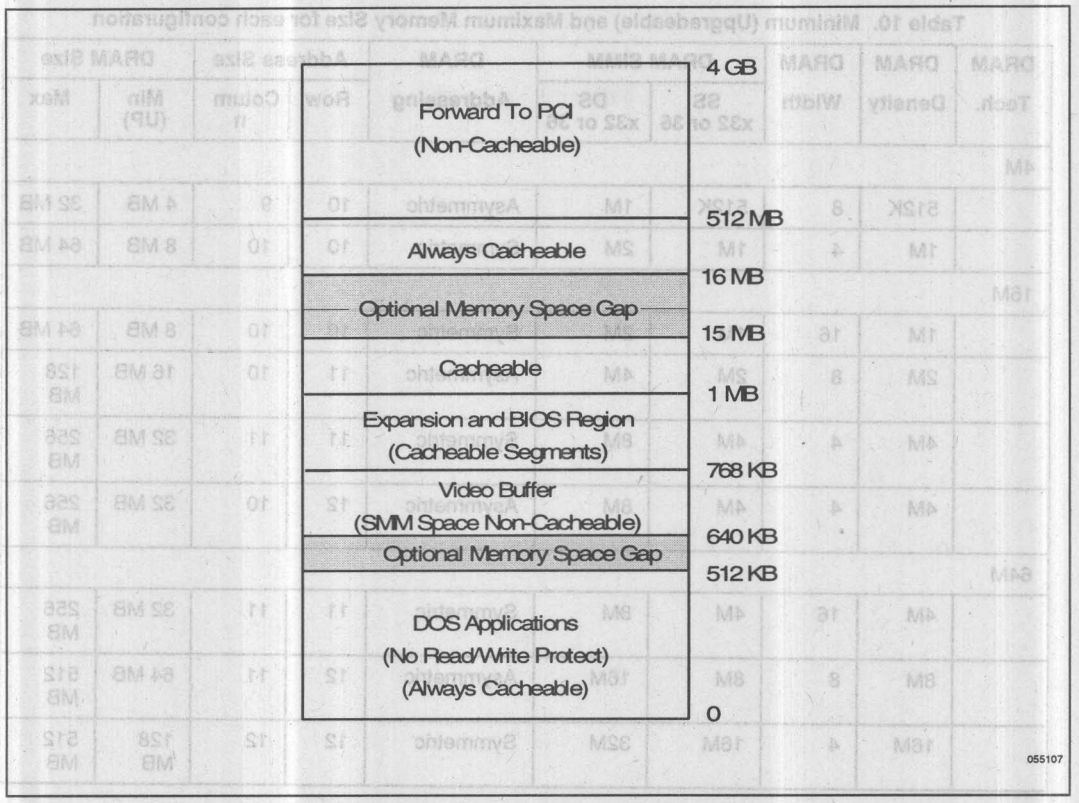


Figure 6. Memory Space Organization

4.4.2. DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by the MA[11:0] signals. The MA[11:0] bits are derived from the host or PCI address bus as defined by Table 11. Note that the lower 10 row address bits and all the column address bits are fixed. The upper 2 row address bit selection varies for each row, and is dependent on the row mux option programmed for that row.

Table 11. DRAM Address Translation

Row Mux Option	MA [11:0]	11	10	9	8	7	6	5	4	3	2	1	0
64M	Row	A25	Default										
Default	Row	A24	A23	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
	Col	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

The DRAM addressing and the size supported by these options is shown in Table 12.

Note: 12 x 8 Asymmetric DRAM is not supported.

Table 12. Memory Mapping Options

Memory Organization	Addressing	Address size
4 MB		
512K x8	Asymmetric	10 x 9
1M x 4	Symmetric	10 x 10
16 MB		
1M x 16	Symmetric	10 x 10
2M x 8	Asymmetric	11 x 10
4M x 4	Symmetric	11 x 11
4M x 4	Asymmetric	12 x 10
64 MB		
4M x 16	Symmetric	11 x 11
8M x 8	Asymmetric	12 x 11
16M x 4	Symmetric	12 x 12

4.4.3. DRAM TYPES

FPM Mode

The TXC, as a default, supports the standard fast page mode (FPM) DRAM.

EDO Mode

Extended Data Out DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge. Compared to standard page mode DRAM which tri-states the memory data when CAS# negates to precharge. With EDO the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

Auto-Detection

A special timing mode (DRAMC[EDME]) may be used for BIOS to detect EDO DRAM's on a bank-by-bank basis. The BIOS first assumes all memory is EDO (sets EDO) and writes a pattern sequence to the main memory. The BIOS then sets the EDO/FPM detect bit to enable the TXC's hardware detect mode. The BIOS then reads the memory location that was previously written. Any read subsequent to the setting of the EDO/FPM detect mode bit will go through the following sequence:

- The TXC waits for the refresh timeout and then asserts CAS# for 3 host clocks.
- The TXC waits for another refresh timeout.
- For a timeout, the DRAM controller latches the data present on the MDxx bus currently and then drives the data onto the host data bus.

The BIOS reads the latched data to determine the type of DRAM present. If the DRAM was FPM type, the negation of the CASx# should have tri-stated the DRAM buffers and, due to the internal pulldowns on the MDxx lines, the data read by the BIOS would be all zeros. If the DRAM was EDO type, the negation of the CASx# would have kept the DRAM buffers active and the BIOS would have read the written pattern, since the data is still driven. Any subsequent DRAM read request will start this sequence again, so all writes must be done before any reads. All writes to the DRAM are treated normally, even if the auto-detection mode is enabled.

Once the type of DRAM has been detected, this information must then be programmed into the DRAM Row Type register. The TXC uses the DRAM Row Type information in conjunction with the DRAM timings set in the DRAM Timing register to configure DRAM accesses optimally.

4.4.4. DRAM PERFORMANCE

The DRAM performance is controlled by the DRAM timing, processor pipelining, and by the type of DRAM used (EDO or standard page mode).

Tables 12 and 13 depict DRAM mode optimum timings for a 64-bit wide double-sided row of EDO SIMMs (i.e., two RAS# lines), without parity and ECC enabled. Expected performance differs depending on DRAM type (EDO vs. FPM), parity or ECC enabled/disabled, DRAM access time, and bus frequency.

Read Cycles

DRAM read performance is measured in two parts. The first part (leadoff) consists of data read from DRAM and is affected by the DRAM technology's page-dependent access time, level of pipelining, and the TXC's ability in identifying cache hits or misses. The second part (burst) is determined by the DRAM technology's ability to put out data bursts.

Write Cycles

DRAM write performance is measured in two parts. The first part is when data is posted into the TXC, and thus, has a leadoff dependent on the availability of the DRAM write posting buffers space. The second part is the latency to write the data from the TXC to memory.

Table 13. CPU to DRAM Read Performance Summary (Notes 2 and 5, Table 13)

DRAM Speed	DRAM Type	Performance (in host clocks)	
		50/60 MHz	66 MHz
Read (Burst Rate)			
50 ns	EDO	x-222	x-222
	FPM	x-333	x-333
60 ns	EDO	x-222	x-222
	FPM	x-333	x-333
70 ns	EDO	x-333	x-333
	FPM (lightly loaded)	x-333	x-444
Read Page Hit/Page Miss/Row Miss Leadoff Rate			
Page Hit			
60 ns	EDO/FPM	4	5
Row Miss (Note 1)			
60 ns	EDO/FPM	7	8
Page Miss			
60 ns	EDO/FPM	10	11
Back-to-Back Burst Reads Page Hit			
60 ns	EDO	4-2223222	5-2223222
60 ns	FPM	4-3333333	5-3333333

Table 14. CPU to DRAM Write Performance Summary (Note 5)

DRAM Speed	DRAM Type	Performance (in host clocks)	
		50/60 MHz	66 MHz
Posted Single Write (Note 3,4)			
60 ns	EDO/FPM		3-3-3
Posted Burst Write (Note 3,4)			
60 ns	EDO/FPM		3-111
Single Retire Hit			
60 ns	FPM	2	3
	EDO	2	2
Single Retire Row Miss (Note 6)			
60 ns	FPM	4	5
	EDO	4	4
Single Retire Page Miss (Note 6)			
60 ns	FPM	7	8
	EDO	7	7
Retire Burst			
60 ns	FPM	- 222	-333
	EDO	-222	-222

NOTES:

1. The above row miss cycles assume that the new page is closed from the prior cycle. Due to the MA[11:2] to RAS# setup requirements, if the page is open, 2 clocks are added to the leadoff.
2. 50/60 MHz allows both Speculative Leadoff and Turbo Read Leadoff to be enabled, whereas 66 MHz only allows Speculative Leadoff to be enabled.
3. This cycle timing assumes the write buffer is empty.
4. Timings are the same for cached or cacheless systems.
5. Timings with ECC enabled (EDE=1) are adjusted by +1 HCLK for all leadoff latencies. Read Turbo Leadoff enabled is illegal if ECC is enabled or L2 is enabled. Reads don't pass writes except for dirty replacements.
6. Assumes fast RAS to CAS timings.

4.4.5. DRAM REFRESH

The TXC supports only CAS-before-RAS# (CBR) refresh. The refresh rate is controlled via the DRAM Refresh Rate field in the DRAM Control register. Refresh is only performed on rows that are populated (i.e., "smart refresh"). The controller determines which rows are populated by looking at the DRB registers.

BIOS should turn off refresh during the DRAM sizing. A delay of at least 60 microseconds should also be added once refresh is turned off and before the first write occurs.

4.4.6. SYSTEM MANAGEMENT RAM

SMRAM is placed at A0000-BFFFFh via the SMRAM Space register.

4.4.7. DATA INTEGRITY SUPPORT

ECC or parity can be checked on the DRAM interface. The default status is parity selected. The DRAM must be populated with 72-bit wide memory to implement ECC or parity.

4.4.7.1. Parity

When parity is enabled, the DRAM parity protection is 8-bit based even parity. If the DRAM array is populated with 64-bit memory (vs 72-bit) the parity logic still logs parity errors in the ERRSTS register. For such DRAM configurations, bit 1 of the ERRCMD register must be 0 (default) to prevent these errors from being signaled via the SERR# mechanism.

BIOS must be aware of the implication of the optional parity support. All physically present DRAM must be first written before SERR#-based NMI generation in the PIIX3 is enabled.

Detection of 64- versus 72-bit Wide SIMMs. The TXC only supports parity or ECC properly if all DRAMs are 72-bit wide. A system with a mixture of 64- and 72-bit wide memory should disable parity and ECC. BIOS can detect the 64-bit wide DRAMs (so that it can disable SERR# on parity error) by writing data that forces the parity bits to be all 1's for address A, and then writing data that forces the parity bits to be all 0's in another location, address B. Now, if address A is read, no parity error will result only if there's a 72-bit wide DRAM present, whereas parity errors would get flagged in the ERRSTS register for a 64-bit wide DRAM. To guard against the chance that somehow the parity pins are being pulled high inadvertently, the test should be redone, this time writing data that forces the parity bits to be all 0's for address A, and all 1's for address B.

4.4.7.2. Error Detection and correction

ECC is an optional data integrity feature provided by the TXC. The feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DED-S4ED) for the DRAM memory subsystem. Additional features are provided that enable software-based system management capabilities.

In systems that support ECC, the read burst timings in the DRAMT register must be programmed to x-3-3-3 (or x-4-4-4). For ECC systems, the 32 clock retry feature should be disabled. The feature can be disabled by setting bit 2 at register offset 4FH to 1.

ECC Generation. When enabled, the TXC generates an 8-bit protection code for 64-bit data during DRAM write operations. If the original write is less than 64-bits, a read-modify-write operation is performed.

ECC Checking and Correction. When enabled, the TXC detects all single and dual-bit errors, and corrects all single-bit errors during DRAM reads. The corrected data is transferred to the requester (CPU or PCI). Note that the corrected data is *not* written back to DRAM.

Error Reporting. When ECC is enabled and ERRCMD is used to set SERR# functionality, ECC errors are signaled to the system via the SERR# pin. The TXC can be programmed to signal SERR# on uncorrectable errors, correctable errors, or both. The type of error condition is latched until cleared by software (regardless of SERR# signaling).

When a single or multi-bit error is detected, the offending DRAM row ID is latched in the ERRSTS register in the TXC. The latched value is held until software explicitly clears the error status flag.

Software Requirements

Initialization. If the ECC feature or parity is enabled, BIOS must take care to properly initialize the memory before enabling the checking. Software should first ensure PCICMD[SERRE] =0, then enable ECC or parity via ERRCMD. Next, the entire DRAM array should be written to ensure valid syndrome/parity bits. Finally, the desired ECC/parity error reporting should be enabled via the ERRCMD and PCICMD registers.

Parity Error Handling. Parity error handling should be via the system's normal NMI routines.

ECC Support Levels. The TXC allows for various levels of ECC support, depending on the specific platform requirements. The software architecture requirements vary based on the level of support implemented. The levels and basic software implications are summarized in the Table 15.

Table 15. ECC Software Levels

Level	Features	Software Requirements
1	Error Checking/Correction	Configuration BIOS
2	Error Checking/Correction Error Scrubbing	Configuration BIOS SMI Scrubbing Routine
3	Error Checking/Correction Error Scrubbing System Management (e.g. error logging, error isolation, memory remapping, etc.)	Configuration BIOS SMI Scrubbing Routine OS-dependent System management handler/applet

Level 1

Level 1 defines a minimal support level for ECC handling that would use the system's standard NMI routine. The configuration BIOS enables SERR# generation only for uncorrectable errors, and disables SERR# generation for correctable errors. The NMI routine will interpret the uncorrectable error event as a parity error, and typically reboot the system. The SERR#-duration should be initialized to generate a pulsed SERR# event (ERRCMD[SED] = 0).

Level 2

Level 2 adds support for error scrubbing of correctable errors using operating system (OS) independent mechanisms. SMI is the preferred mechanism to implement OS-independence. In this case, the SMI handler would be invoked for both correctable and uncorrectable errors. The SERR# output will not be connected to the PCI bus, but will instead connect to external logic that differentiates between SMI and NMI requests. The SERR#-output type should be configured as a normal output (PCON[SOT]=1), and the duration should be initialized to the level mode (ERRCMD[SED] = 1).

For correctable errors, the handler first clears the error flags and then starts a scrub process. The time spent in an SMI routine should be minimized, since interrupts are disabled and OS services (e.g. real time clocks) could be adversely affected. To minimize time spent during the SMI handler, the scrub process should be distributed into small time slices. The handler can setup future SMI events to re-occur based on a hardware timer (e.g. the "Fast Off" green timer in Intel PCIset standard expansion bridges [PIIX3]) until the memory scrub has completed.

The following example estimates the worst-case scrub duration for a single correctable error.

Example Assumptions:

- 128 Mbytes/Row (64 Mbit technology) =4M lines at 32 bytes/line
- Scrub operation memory bound by linefill + write-back (with medium DRAM timings) = 30 clks/line
- SMI scrub time slice budget = 1 msec/SMI
- Fast-off SMI interrupt interval = 100 msec/interrupt

With the above assumptions The scrub time is:

- the time to scrub one row is 4M lines/row X 30 clks/line X 15 ns/clk = 1.8 msec/row.
- Thus, spreading the scrub time requires: (1.8 sec/row)/(1 msec /SMI) = 1800 SMI events.
- The total duration for the scrub SMI events will be 1800 SMI events * 100 msec/interrupt = 180 sec.

For uncorrectable errors, the SMI handler should pass the error to the system's normal NMI handler, making it appear as a standard parity error to the software. To pass the NMI event, the SMI routine should first clear out the ECC error flags (MEF, SEF). The handler should then generate a pulsed SERR# event by writing a 1 to the MEF flag. This generates a 1 PCLK SERR# assertion, which will be converted into an NMI interrupt by the expansion bridge.

Level 3

Level 3 adds more sophisticated system management functions beyond simple error scrubbing. Typical functions could include error event logging, error isolation, memory remapping, system diagnostics and user interface application. Software to implement Level 3 functions are OS-dependent, and beyond the scope of this document. However, the features used to implement Level 2 functions can also be leveraged in Level 3 systems.

4.5. PCI Bus Arbitration

The TXC's PCI Bus arbiter allows PCI peer-to-peer traffic concurrent with CPU main memory/second level cache cycles. The arbiter supports five PCI masters (Figure 7). REQ[3:0]#/GNT[3:0]# are used by PCI masters other than the PCI-to-ISA expansion bridge (PIIX3). PHLD#/PHLDA# are the arbitration request/grant signals for the PIIX3 and provide guaranteed access time capability for ISA masters. PHLD#/PHLDA# also optimize system performance based on PIIX3 known policies. The arbitration mechanism is enhanced with a Multi-Transaction Timer mechanism. This feature improves the PCI bandwidth allocation to short bursts, an important consideration for example, with typical video capture devices.

Multi-Transaction Timer (MTT)

The priority chain algorithm has been enhanced by the Multi-Transaction Timer (MTT), register 70h. The effect of the MTT is to guarantee a minimum time slice on PCI to an agent that keeps its request asserted. (Note that this mechanism differs from the MLT operation, that enforces a maximum time slice for an agent.) The MTT algorithm ensures a fairer bandwidth allocation for PCI devices that generate short burst traffic, or for multi-function devices with several bus master agents behind one physical PCI interface.

Passive Release and Bus Lock

To comply with PCI 2.1 latency requirements, the TXC supports passive release. The TXC only supports bus lock mode. The bus lock mode precludes 3rd party locks.

Enabling Delayed Transactions

To enable Delayed Transactions, Delayed Transactions (PIIX3 Function 0, 82h[0]), North Bridge Retry Enable (PIIX3 Function 0, 6Ah[7]), and TXC 4Fh[7]), bits should all be set to '1'. When enabling, PIIX3 bits should be set first and then the TXC 4Fh[7]. When disabling, the reverse order must be followed.

4.5.1. CPU POLICIES

The CPU never explicitly requests the bus. Instead, the arbiter grants the bus to the CPU when:

- the CPU is the highest priority
- PCI agents do not require main memory (peer-to-peer transfers or bus idle) and the PCI Bus is not currently locked by a PCI master

When the CPU is granted as highest priority, the MLT timer is used to guarantee a minimum amount of system resources to the CPU before another requesting PCI agent is granted. An AHOLD mechanism controls granting the bus to the CPU.

4.6. Clock Generation and Distribution

The skew between any two HCLK loads must be less than or equal to 1 ns. The skew between HCLK at the pin of the TXC and the pin of the CPU must be less than or equal to 0.3 ns. The skew between any two PCLK loads must be less than or equal to 2 ns, the requirement of the PCI Rev 2.0 specification. For HCLK to PCLK ratios of 2-to-1, the rising edge of PCLKIN must be within 1 to 6.0 ns of the rising edge of HCLKIN, with HCLK leading PCLK.

4.6.1. RESET SEQUENCING

The TXC is asynchronously reset by the PCI reset RST#. The TXC will change MWE# to its default value (inactive) synchronous to HCLK after RST# is negated.

Arbiter (Central Resource) Functions on Reset

The TXC arbiter includes support for PCI central resource functions. These functions include driving the AD[31:0], C/BE[3:0]#, and PAR signals whenever no one is granted the PCI bus and the bus is idle. The TXC drives 0's on these signals during these times, plus during RESET.

5.0. PINOUT AND PACKAGE INFORMATION

5.1. TXC Pinout Information

Figure 8 shows the pin assignments for the TXC.

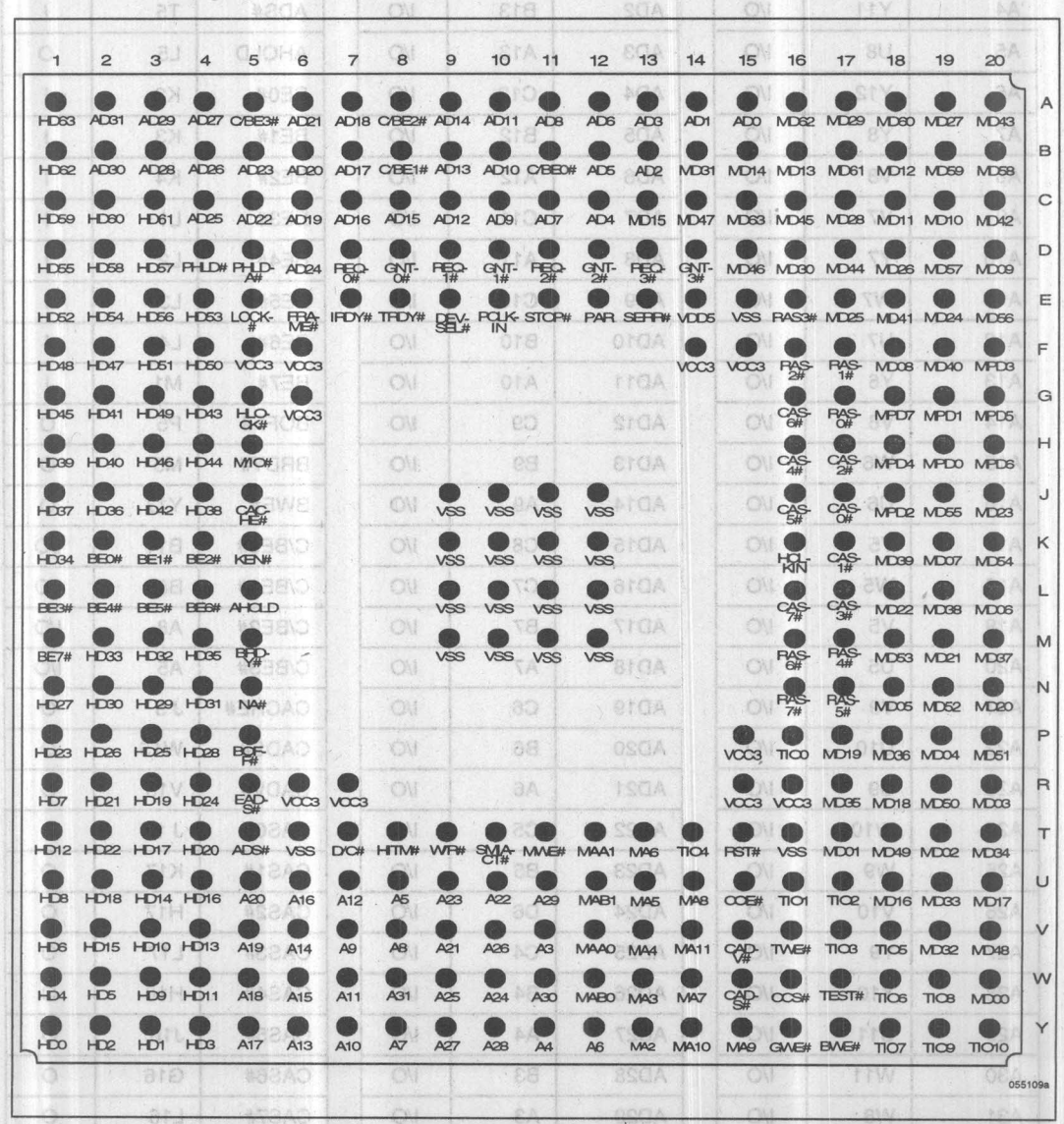


Figure 8. TXC Pinout

Table 16. TXC Alphabetical Pin Assignment

Name	Ball #	Type
A3	V11	I/O
A4	Y11	I/O
A5	U8	I/O
A6	Y12	I/O
A7	Y8	I/O
A8	V8	I/O
A9	V7	I/O
A10	Y7	I/O
A11	W7	I/O
A12	U7	I/O
A13	Y6	I/O
A14	V6	I/O
A15	W6	I/O
A16	U6	I/O
A17	Y5	I/O
A18	W5	I/O
A19	V5	I/O
A20	U5	I/O
A21	V9	I/O
A22	U10	I/O
A23	U9	I/O
A24	W10	I/O
A25	W9	I/O
A26	V10	I/O
A27	Y9	I/O
A28	Y10	I/O
A29	U11	I/O
A30	W11	I/O
A31	W8	I/O
AD0	A15	I/O

Name	Ball #	Type
AD1	A14	I/O
AD2	B13	I/O
AD3	A13	I/O
AD4	C12	I/O
AD5	B12	I/O
AD6	A12	I/O
AD7	C11	I/O
AD8	A11	I/O
AD9	C10	I/O
AD10	B10	I/O
AD11	A10	I/O
AD12	C9	I/O
AD13	B9	I/O
AD14	A9	I/O
AD15	C8	I/O
AD16	C7	I/O
AD17	B7	I/O
AD18	A7	I/O
AD19	C6	I/O
AD20	B6	I/O
AD21	A6	I/O
AD22	C5	I/O
AD23	B5	I/O
AD24	D6	I/O
AD25	C4	I/O
AD26	B4	I/O
AD27	A4	I/O
AD28	B3	I/O
AD29	A3	I/O
AD30	B2	I/O

Name	Ball #	Type
AD31	A2	I/O
ADS#	T5	I
AHOLD	L5	O
BE0#	K2	I
BE1#	K3	I
BE2#	K4	I
BE3#	L1	I
BE4#	L2	I
BE5#	L3	I
BE6#	L4	I
BE7#	M1	I
BOFF#	P5	O
BRDY#	M5	O
BWE#	Y17	O
C/BE0#	B11	I/O
C/BE1#	B8	I/O
C/BE2#	A8	I/O
C/BE3#	A5	I/O
CACHE#	J 5	O
CADS#	W15	O
CADV#	V15	O
CAS0#	J 17	O
CAS1#	K17	O
CAS2#	H17	O
CAS3#	L17	O
CAS4#	H16	O
CAS5#	J16	O
CAS6#	G16	O
CAS7#	L16	O
CCS#	W16	O

Name	Ball #	Type
COE#	U15	O
D/C#	T7	I
DEVSEL#	E9	I/O
EADS#	R5	O
FRAME#	E6	I/O
GNT0#	D8	I
GNT1#	D10	I
GNT2#	D12	I
GNT3#	D14	I
GWE#	Y16	O
HCLKIN	K	I
HD0	Y1	I/O
HD1	Y3	I/O
HD2	Y2	I/O
HD3	Y4	I/O
HD4	W1	I/O
HD5	W2	I/O
HD6	V1	I/O
HD7	R1	I/O
HD8	U1	I/O
HD9	W3	I/O
HD10	V3	I/O
HD11	W4	I/O
HD12	T1	I/O
HD13	V4	I/O
HD14	U3	I/O
HD15	V2	I/O
HD16	U4	I/O
HD17	T3	I/O
HD18	U2	I/O
HD19	R3	I/O

Name	Ball #	Type
HD20	T4	I/O
HD21	R2	I/O
HD22	T2	I/O
HD23	P1	I/O
HD24	R4	I/O
HD25	P3	I/O
HD26	P2	I/O
HD27	N1	I/O
HD28	P4	I/O
HD29	N3	I/O
HD30	N2	I/O
HD31	N4	I/O
HD32	M3	I/O
HD33	M2	I/O
HD34	K1	I/O
HD35	M4	I/O
HD36	J 2	I/O
HD37	J1	I/O
HD38	J 4	I/O
HD39	H1	I/O
HD40	H2	I/O
HD41	G2	I/O
HD42	J 3	I/O
HD43	G4	I/O
HD44	H4	I/O
HD45	G1	I/O
HD46	H3	I/O
HD47	F2	I/O
HD48	F1	I/O
HD49	G3	I/O
HD50	F4	I/O

Name	Ball #	Type
HD51	F3	I/O
HD52	E1	I/O
HD53	E4	I/O
HD54	E2	I/O
HD55	D1	I/O
HD56	E3	I/O
HD57	D3	I/O
HD58	D2	I/O
HD59	C1	I/O
HD60	C2	I/O
HD61	C3	I/O
HD62	B1	I/O
HD63	A1	I/O
HITM#	T8	I
HLOCK#	G5	I
IRDY#	E7	I/O
KEN#/INV	K5	O
LOCK#	E5	I/O
M/IO#	H5	I
MA2	Y13	O
MA3	W13	O
MA4	V13	O
MA5	U13	O
MA6	T13	O
MA7	W14	O
MA8	U14	O
MA9	Y15	O
MA10	Y14	O
MA11	V14	O
MAA0	V12	O
MAA1	T12	O

Name	Ball #	Type
MAB0	W12	O
MAB1	U12	O
MD00	W20	I/O
MD01	T17	I/O
MD02	T19	I/O
MD03	R20	I/O
MD04	P19	I/O
MD05	N18	I/O
MD06	L20	I/O
MD07	K19	I/O
MD08	F18	I/O
MD09	D20	I/O
MD10	C19	I/O
MD11	C18	I/O
MD12	B18	I/O
MD13	B16	I/O
MD14	B15	I/O
MD15	C13	I/O
MD16	U18	I/O
MD17	U20	I/O
MD18	R18	I/O
MD19	P17	I/O
MD20	N20	I/O
MD21	M19	I/O
MD22	L18	I/O
MD23	J 20	I/O
MD24	E19	I/O
MD25	E17	I/O
MD26	D18	I/O
MD27	A19	I/O
MD28	C17	I/O

Name	Ball #	Type
MD29	A17	I/O
MD30	D16	I/O
MD31	B14	I/O
MD32	V19	I/O
MD33	U19	I/O
MD34	T20	I/O
MD35	R17	I/O
MD36	P18	I/O
MD37	M20	I/O
MD38	L19	I/O
MD39	K18	I/O
MD40	F19	I/O
MD41	E18	I/O
MD42	C20	I/O
MD43	A20	I/O
MD44	D17	I/O
MD45	C16	I/O
MD46	D15	I/O
MD47	C14	I/O
MD48	V20	I/O
MD49	T18	I/O
MD50	R19	I/O
MD51	P20	I/O
MD52	N19	I/O
MD53	M18	I/O
MD54	K20	I/O
MD55	J19	I/O
MD56	E20	I/O
MD57	D19	I/O
MD58	B20	I/O
MD59	B19	I/O

Name	Ball #	Type
MD60	A18	I/O
MD61	B17	I/O
MD62	A16	I/O
MD63	C15	I/O
MPD0	H19	I/O
MPD1	G19	I/O
MPD2	J18	I/O
MPD3	F20	I/O
MPD4	H18	I/O
MPD5	G20	I/O
MPD6	H20	I/O
MPD7	G18	I/O
MWE#	T11	O
NA#	N5	O
PAR	E12	I/O
PCLKIN	E10	I
PHLD#	D4	I
PHLDA#	D5	O
RAS0#	G17	O
RAS1#	F17	O
RAS2#	F16	O
RAS3#	E16	O
RAS4#	M17	O
RAS5#	N17	O
RAS6#	M16	O
RAS7#	N16	O
REQ0#	D7	O
REQ1#	D9	O
REQ2#	D11	O
REQ3#	D13	O
RST#	T15	I

Name	Ball #	Type
SERR#	E13	O
SMIACT#	T10	I
STOP#	E11	I/O
TEST#	W17	I
TIO0	P16	I/O
TIO1	U16	I/O
TIO2	U17	I/O
TIO3	V17	I/O
TIO4	T14	I/O
TIO5	V18	I/O
TIO6	W18	I/O
TIO7	Y18	I/O
TIO8	W19	I/O
TIO9	Y	I/O
TIO10	Y20	I/O
TRDY#	E8	I/O

Name	Ball #	Type
TWE#	V16	O
VCC3	R16	—
VCC3	F5	—
VCC3	F6	—
VCC3	G6	—
VCC3	R6	—
VCC3	R7	—
VCC3	F14	—
VCC3	F15	—
VCC3	P15	—
VCC3	R15	—
VDD5	E14	—
VSS	T6	—
VSS	J 9	—
VSS	K9	—
VSS	L9	—

Name	Ball #	Type
VSS	M9	—
VSS	J 10	—
VSS	K10	—
VSS	L10	—
VSS	M10	—
VSS	J 11	—
VSS	K11	—
VSS	L11	—
VSS	M11	—
VSS	J 12	—
VSS	K12	—
VSS	L12	—
VSS	M12	—
VSS	E15	—
VSS	T16	—
W/R#	T9	I

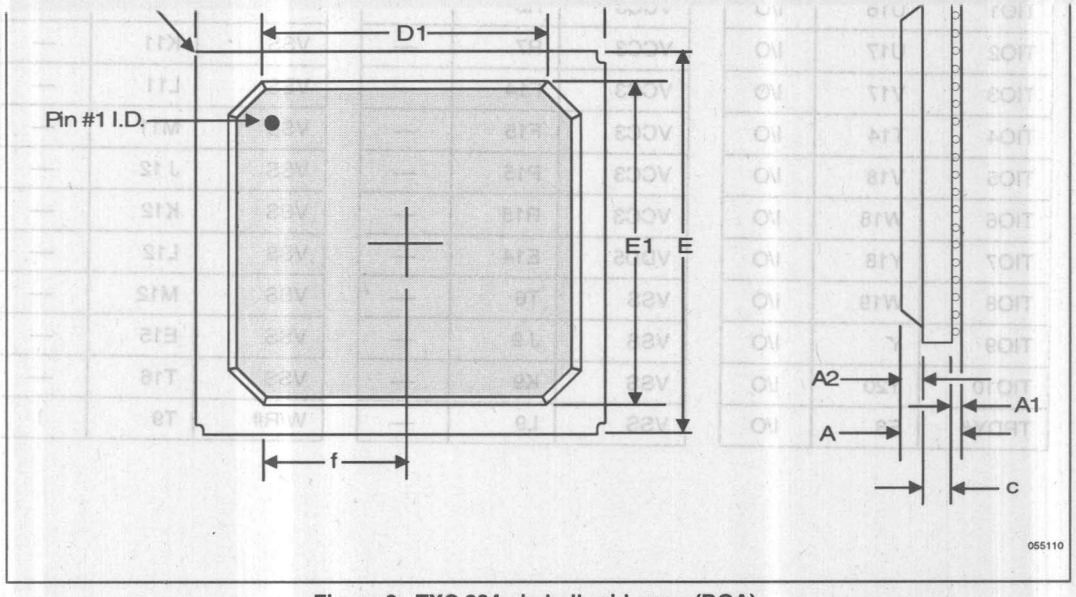


Figure 9. TXC 324 pin ball grid array (BGA).

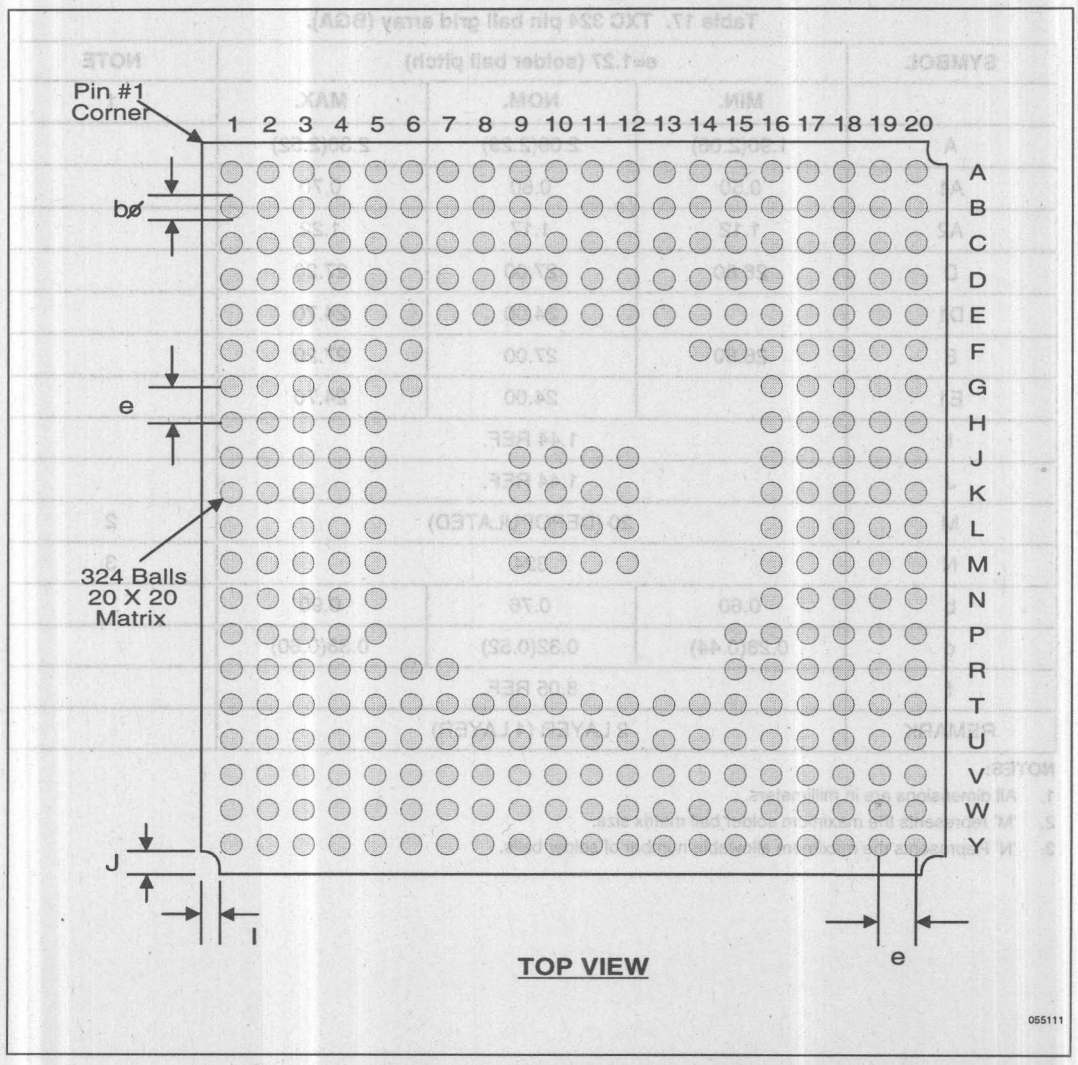


Figure 10. TXC 324 pin ball grid array (BGA) Ball Pattern

Table 17. TXC 324 pin ball grid array (BGA).

SYMBOL	e=1.27 (solder ball pitch)			NOTE
	MIN.	NOM.	MAX.	1
A	1.90(2.06)	2.09(2.29)	2.30(2.52)	
A1	0.50	0.60	0.70	
A2	1.12	1.17	1.22	
D	26.80	27.00	27.20	
D1		24.00	24.70	
E	26.80	27.00	27.20	
E1		24.00	24.70	
I	1.44 REF.			
J	1.44 REF.			
M	20 (DEPOPULATED)			2
N	324			3
b	0.60	0.76	0.90	
c	0.28(0.44)	0.32(0.52)	0.38(0.60)	
f	8.05 REF.			
REMARK	2 LAYER (4 LAYER)			

NOTES:

1. All dimensions are in millimeters.
2. 'M' represents the maximum solder ball matrix size.
3. 'N' Represents the maximum allowable number of solder balls.

6.0. TESTABILITY

6.1. NAND Tree Mode

A NAND tree mode is provided for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to set the connectivity of each of the TXC's signal pins. The NAND tree mode is activated by driving the test-pin TEST# when REQ[3:0]# pins are 0010. If TEST is negated at any time, the test-mode is de-activated and the TXC goes back to normal operation. There is no guarantee that upon re-entering normal operation the chip will function properly if the test-mode was entered while the TXC was not in a completely idle state.

In NAND tree mode, all outputs are Tri-stated except GNT[3:0]# and PHLDA#. These pins are the NAND-chain and test mode outputs. The chain is separated into 4 77-pin chains.

6.1.1. OVERVIEW

The TXC has 2 full-chip test-modes to improve board manufacture. If the TEST# is asserted (driven low), the value on REQ#[3:0] indicates the test-mode to enable. The test-mode enabled at the rising edge of TEST# will remain enabled while TEST# is high (Figure 11). A new test-mode can be enabled by again driving TEST# low and selecting a new combination on PHLD# and REQ#[3:0]. Any active test-mode is disabled by asserting RST# with TEST# is de-asserted or selecting the DISABLE mode with TEST# low (see table below). Asserting RST# while TEST# is asserted has no effect on the test-mode. In addition, all outputs are floated while RST# and TEST# are both asserted.

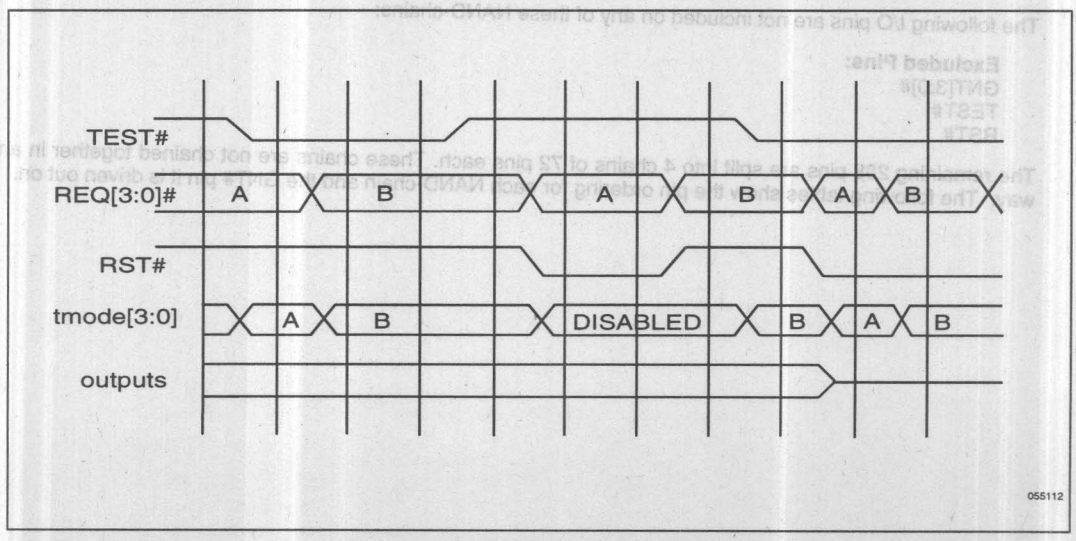


Figure 11. Full-Chip Test Mode Timing

The following sub-sections describe both test-modes in more detail.

6.1.2. NAND CHAIN MODE

All outputs are tri-stated, except GNT[3:0]#. All pins on the TXC are either pure inputs are bi-directional. Because the bi-directional pins are tri-stated during nand-chain test there is no need to back-drive outputs. However, all internal pull-ups or pull-downs are still active. The GNT[3:0]# pins drive the output of the NAND Chains. The only pins not included on the NAND-Chain are RST#, TEST# and GNT[3:0]#. The RST# pin is NOT required for enabling NAND-Chain mode. This is important to board-level test as assertion of reset on a system board can force other components into an undesirable state. All pins must be driven using a maximum of 3.3V.

The following I/O pins are not included on any of these NAND-chains:

Excluded Pins:
GNT[3:0]#
TEST#
RST#

The remaining 288 pins are split into 4 chains of 72 pins each. These chains are not chained together in any way. The following tables show the pin ordering for each NAND-chain and the GNT# pin it is driven out on.

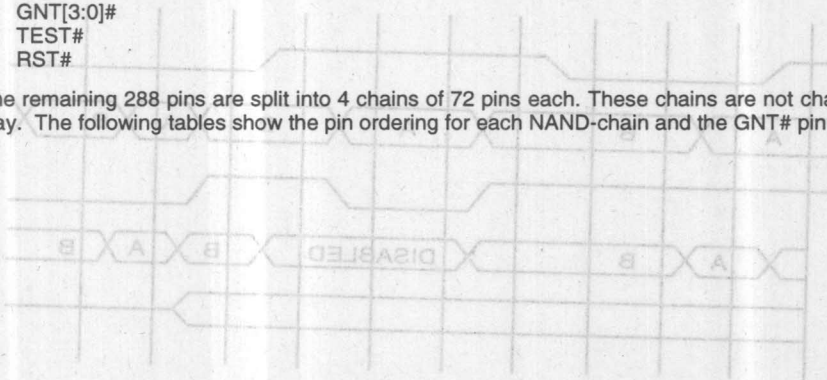


Table 19. Chain 0 (GNT0#)

Pin Name	Chain Element
A25	CH0_00
A7	CH0_01
A10	CH0_02
A21	CH0_03
A23	CH0_04
SMIACTB	CH0_05
A31	CH0_06
A18	CH0_07
HD3	CH0_08
A12	CH0_09
A14	CH0_10
HD11	CH0_11
A19	CH0_12
A16	CH0_13
HITMB	CH0_14
HD13	CH0_15
D_CB	CH0_16
HD0	CH0_17
HD10	CH0_18
HD16	CH0_19
HD6	CH0_20
HD14	CH0_21
BOFFB	CH0_22
HD18	CH0_23
HD24	CH0_24

Pin Name	Chain Element
HD8	CH0_25
HD19	CH0_26
HD7	CH0_27
HD31	CH0_28
HD26	CH0_29
HD27	CH0_30
HD33	CH0_31
AHOLD	CH0_32
BE5B	CH0_33
BE6B	CH0_34
HD34	CH0_35
BE2B	CH0_36
BE0B	CH0_37
HD37	CH0_38
BE1B	CH0_39
HD36	CH0_40
HD41	CH0_41
HD52	CH0_42
CACHEB	CH0_43
HD47	CH0_44
HD44	CH0_45
HD49	CH0_46
HD54	CH0_47
HD55	CH0_48
HD57	CH0_49

Pin Name	Chain Element
HLOCKB	CH0_50
HD53	CH0_51
HD60	CH0_52
HD62	CH0_53
HD61	CH0_54
AD30	CH0_55
AD25	CH0_56
AD22	CH0_57
AD24	CH0_58
AD27	CH0_59
AD19	CH0_60
C_BE3B	CH0_61
REQ0B	CH0_62
AD20	CH0_63
AD21	CH0_64
TRDYB	CH0_65
AD16	CH0_66
C_BE2B	CH0_67
C_BE1B	CH0_68
AD14	CH0_69
AD12	CH0_70
AD13	CH0_71

Table 20. Chain 1 (GNT1#)

Pin Name	Chain Element
A24	CH1_00
A27	CH1_01
A26	CH1_02
A13	CH1_03
A8	CH1_04
W_RB	CH1_05
A11	CH1_06
A17	CH1_07
A15	CH1_08
A5	CH1_09
A9	CH1_10
HD1	CH1_11
HD9	CH1_12
A20	CH1_13
HD2	CH1_14
HD5	CH1_15
HD4	CH1_16
ADSB	CH1_17
HD15	CH1_18
EADSB	CH1_19
HD20	CH1_20
HD17	CH1_21
HD22	CH1_22
HD12	CH1_23
HD28	CH1_24
HD21	CH1_25
NAB	CH1_26
HD25	CH1_27
BRDYB	CH1_28
HD23	CH1_29
HD35	CH1_30
HD29	CH1_31
HD30	CH1_32
BE7B	CH1_33
HD32	CH1_34
BE3B	CH1_35
BE4B	CH1_36
HD39	CH1_37
HD45	CH1_38
HD42	CH1_39
HD38	CH1_40
HD40	CH1_41
HD48	CH1_42
KENB	CH1_43
HD46	CH1_44
HD43	CH1_45
HD51	CH1_46
HD58	CH1_47
HD56	CH1_48
HD50	CH1_49
M_IOB	CH1_50
HD59	CH1_51
HD63	CH1_52
PHLDB	CH1_53
AD31	CH1_54
PLOCKB	CH1_55
AD28	CH1_56
FRAMEB	CH1_57
AD29	CH1_58
PHLDAB	CH1_59
IRDYB	CH1_60
AD26	CH1_61
AD23	CH1_62
AD17	CH1_63
DEVSELB	CH1_64
AD18	CH1_65
REQ1B	CH1_66
AD15	CH1_67
PCLKIN	CH1_68
AD11	CH1_69
AD10	CH1_70
AD9	CH1_71

Table 21. Chain 2 (GNT2#)

Pin Name	Chain Element
A28	CH2_00
A29	CH2_01
A3	CH2_02
A30	CH2_03
A4	CH2_04
MWEB	CH2_05
MA10	CH2_06
MAA1	CH2_07
MA7	CH2_08
MA5	CH2_09
MA11	CH2_10
MA6	CH2_11
MA9	CH2_12
BWEB	CH2_13
COEB	CH2_14
CCSB	CH2_15
MD0	CH2_16
MD1	CH2_17
MD16	CH2_18
MD32	CH2_19
MD48	CH2_20
MD49	CH2_21
MD18	CH2_22
MD19	CH2_23
MD17	CH2_24
MD2	CH2_25
MD50	CH2_26
MD34	CH2_27
RAS6B	CH2_28
MD5	CH2_29
CAS7B	CH2_30
RAS4B	CH2_31
MD53	CH2_32
MD22	CH2_33
MD6	CH2_34
MD39	CH2_35
MD7	CH2_36
MD54	CH2_37
HCLKIN	CH2_38
MD55	CH2_39
MPD2	CH2_40
CAS5B	CH2_41
MPD1	CH2_42
CAS2B	CH2_43
MPD7	CH2_44
CAS4B	CH2_45
MPD3	CH2_46
MD40	CH2_47
RAS0B	CH2_48
MD26	CH2_49
MD25	CH2_50
MD42	CH2_51
RAS2B	CH2_52
MD59	CH2_53
MD11	CH2_54
MD43	CH2_55
MD27	CH2_56
MD30	CH2_57
MD28	CH2_58
MD12	CH2_59
MD60	CH2_60
AD2	CH2_61
STOPB	CH2_62
AD4	CH2_63
AD0	CH2_64
AD3	CH2_65
AD5	CH2_66
AD7	CH2_67
AD6	CH2_68
C_BE0B	CH2_69
REQ2B	CH2_70
AD8	CH2_71

Table 22. Chain 3 (GNT3#)

Pin Name	Chain Element
A22	CH3_00
MAB0	CH3_01
MAA0	CH3_02
A6	CH3_03
MA3	CH3_04
MA2	CH3_05
MA4	CH3_06
MAB1	CH3_07
CADSB	CH3_08
MA8	CH3_09
GWEB	CH3_10
CADVB	CH3_11
TWEB	CH3_12
TIO4	CH3_13
TIO3	CH3_14
TIO1	CH3_15
TIO7	CH3_16
TIO6	CH3_17
TIO9	CH3_18
TIO2	CH3_19
TIO8	CH3_20
TIO5	CH3_21
TIO10	CH3_22
TIO0	CH3_23
RAS7B	CH3_24
MD35	CH3_25
MD33	CH3_26
MD36	CH3_27
RAS5B	CH3_28
MD4	CH3_29
MD3	CH3_30
MD52	CH3_31
MD51	CH3_32
MD20	CH3_33
MD21	CH3_34
MD37	CH3_35
MD38	CH3_36
CAS3B	CH3_37
CAS1B	CH3_38
MD23	CH3_39
MPD0	CH3_40
MPD6	CH3_41
MPD4	CH3_42
CAS0B	CH3_43
MPD5	CH3_44
MD56	CH3_45
MD8	CH3_46
MD9	CH3_47
RAS1B	CH3_48
MD24	CH3_49
MD41	CH3_50
MD57	CH3_51
CAS6B	CH3_52
MD10	CH3_53
RAS3B	CH3_54
MD58	CH3_55
MD44	CH3_56
SERRB	CH3_57
MD46	CH3_58
MD45	CH3_59
MD61	CH3_60
MD31	CH3_61
MD29	CH3_62
MD13	CH3_63
MD15	CH3_64
REQ3B	CH3_65
MD63	CH3_66
MD62	CH3_67
MD47	CH3_68
PAR	CH3_69
MD14	CH3_70
AD1	CH3_71

6.2. ID Code Test Mode

To enable this mode TEST# and RST# must be asserted and REQ[3:0]# must be set to 1110. RST# is then negated after 2 HCLKs and TEST# must then be negated after 2 more HCLKs and REQ[3:0]# changed to the value 1111. The value of PHLD# and RST# pin must also be 1. Once REQ[3:0]#, PHLD# and RST# are all driven high, the Device ID (DID) will be driven on AD[15:0], and the Revision ID (RID) will be driven on AD[23:16]. The value on AD[31:24] is indeterminate. The following timing diagram shows how the test-mode is enabled:

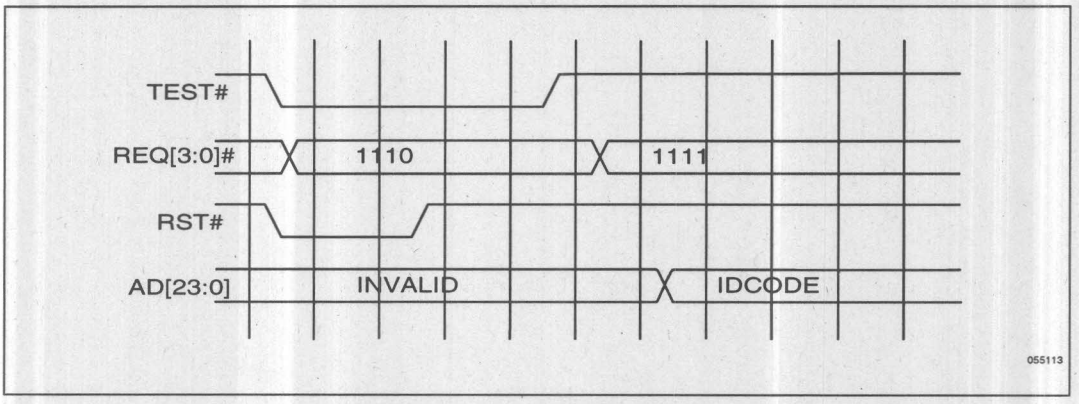


Figure 12. Test Mode Enable

TEST#
REQ[3:0]#
RST#
ADL[23:0]
1111
1110
INVALID
IDC ODE

intel®

DATASHEET
ADDENDUM

Intel 430HX PCIset
82439HX System Controller (TXC)
Timing Specification

272945-001

September, 1996

DATASHEET
ADDENDUM

Intel 430HX PCIset
82439HX System Controller (TXC)
Timing Specification

272945-001

September, 1996

Intel 430HX PCIset
82439HX SYSTEM CONTROLLER (TXC) FEATURES

- Supports the Pentium® Processor at 66 MHz, 60 MHz, and 50 MHz at 3 V
- Supports the Universal Serial Bus (USB)
- Dual Processor Support
- PCI 2.1 Compliant
- Integrated Second Level Cache Controller
  - Direct Mapped Organization
  - Write-Back Cache Policy
  - Cacheless, 256 Kbytes, and 512 Kbytes
  - Pipelined Burst SRAMs
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1
  - Integrated Tag/Valid Status Bits for Cost Savings and Performance
  - Optional 512 MB DRAM Cacheability Limit
  - Supports 5 V SRAMs for Tag Address
- Integrated DRAM Controller
  - 4 Mbytes to 512 Mbytes Memory
  - 64-Mbit DRAM Technology Support
  - Asymmetric DRAM Support
  - 8 Qword Deep Merging DRAM Write Buffer
  - Enhanced EDO/Hyper Page Mode DRAM Supports 4-2-2-2 Reads and x-2-2-2 Writes at 60 MHz, 5-2-2-2 Reads and x-2-2-2 Writes at 66 MHz
  - 8 RAS Lines Available
  - Integrated Programmable-Strength MA Buffers
  - CAS-Before-RAS Refresh
- Optional Parity
- Optional Error Checking and Correction (ECC)
  - Superior DRAM Data Integrity
  - Single-Bit Error Correction, Multi-Bit Error Detection plus Nibble Failure Detection ECC Code
  - Single- and Multi-bit Error Reporting
  - Virtual Swapable Bank Support (i.e., can swap out problem banks)
  - Merging Write Buffer Eliminates Most Partial Write Cycles
- Fully Synchronous, Minimum Latency 25/30/33 MHz PCI Bus Interface
  - Zero Wait State CPU-to-PCI Write Timings for Superior Graphics Performance
  - Enhanced CPU-to-PCI Read Latencies for Superior Graphics/PIO Performance
  - 21 DWORD PCI-DRAM Post Buffer
  - 22 DWord PCI-to-DRAM Read Prefetch Buffer
  - Writeback Merging for PCI-to-DRAM Writes
  - Writeback Forwarding for PCI-to-DRAM Reads
  - Pipelined Snoop Ahead
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions Within the Same PCI Arbitration Cycle
- Single 324-Pin BGA Package

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 430HX PCIset. Please refer to the standard package datasheet (order number 290551) for product information and specifications not found in this document.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

- Dual Processor Support
- PCI 2.1 Compliant
- Integrated Second Level Cache Controller
  - Direct Mapped Organization
  - Write-Back Cache Policy
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  - Pipelined Burst SRAMs
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  - Optional 512 MB DRAM Cacheability Limit
  - Supports 5 V SRAMs for Tag Address
- Integrated DRAM Controller
  - 4 Mbytes to 512 Mbytes Memory
  - 64-Mbit DRAM Technology Support
  - Asymmetric DRAM Support
  - 8 Qword Deep Merging DRAM Write Buffer
  - Enhanced EDO/Hyper Page Mode DRAM Supports 4-2-2-2 Reads and x-2-2-2 Writes at 90 MHz, 5-2-2-2 Reads and x-2-2-2 Writes at 66 MHz
  - 8 RAS Lines Available
  - Integrated Programmable-Strength MA Buffers
  - CAS-Before-RAS Refresh
- Fully Synchronous, Minimum Latency 25/30/33 MHz PCI Bus Interface
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NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Case Temperature under Bias ..... 0°C to +85°C
Storage Temperature ..... -55°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3 V to VDD + 0.3 V
Maximum Power Dissipation ..... 1.26 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.*

1.2 Thermal Characteristics

The 82439HX is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the 82439HX BGA (Ball Grid Array) package are given in Table 1.

Table 1. 82439HX System Controller (TXC) Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/Watt)	29.0	24.5
θ_{jc} (°C/Watt)	9.0	

1.3 D.C. Characteristics

Table 2. 82439HX System Controller (TXC) D.C. Characteristics
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Notes 1,8; VDD3 = 3.135 V
V_{IH1}	Input High Voltage	2.0	VDD3 + 0.3	V	Notes 1,9; VDD3 = 3.6V
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2; VDD = 4.75V
V_{IH2}	Input High Voltage	2.0	VDD + 0.3	V	Note 2; VDD = 5.25V
V_{IL3}	Input Low Voltage	-0.4	0.8	V	Note 3; VDD3 = 3.135
V_{IH3}	Input High Voltage	2.8	VDD3 + 0.3	V	Note 3; VDD3 = 3.6
V_{OL1}	Output Low Voltage		0.4	V	Note 4
V_{OH1}	Output High Voltage	2.4		V	Note 4
I_{OL1}	Output Low Current		4	mA	Note 5
I_{OH1}	Output High Current	-2		mA	Note 5
I_{OL2}	Output Low Current		8	mA	Note 6
I_{OH2}	Output High Current	-2		mA	Note 6
I_{OL3}	Output Low Current		12	mA	Note 7
I_{OH3}	Output High Current	-2		mA	Note 7
I_{IH1}	Input Leakage Current		10	µA	0 V<V_{in}<VDD/VDD3
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		10	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		10	pF	FC = 1 MHz
I_{CC}	V_{CC} Supply Current		10 350	mA mA	5 V Supply 3 V Supply

NOTES:

1. V_{IL1} and V_{IH1} apply to the following 3.3 V input signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#, SMIACT#, PHLD#, REQ[3:0]#, RST#, HCLKIN, PCLKIN as well the following signals when used as 3.3 V inputs during NAND tree testing: BRDY#, NA#, AHOLD, EADS#, BOFF#, KEN#/INV, CADV#, CADS#, CCS#, COE#, GWE#, BWE#, TWE#, MWE#, MA[11:2], MAA[1:0], MAB[1:0]
2. V_{IL2} and V_{IH2} apply to the following 5.0 V tolerant input signals: TIO[10:0], AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, SERR#, MD[63:0], MPD[7:0], HD[63:0]
3. V_{IL3} and V_{IH3} apply to the following input signals: TESTIN#, RST#
4. V_{OL1} and V_{OH1} apply to the following signals: TIO[10:0], TWE#, CADV#, CADS#, CCS#, COE#, GWE#, BWE#, A[31:3], HD[63:0], KEN#/INV, AHOLD, BRDY#, NA#, BOFF#, EADS#, MAA[1:0], MAB[1:0], MA[11:2], MWE#, MD[63:0], MPD[7:0], CAS[7:0]#, RAS[7:0]#, GNT[3:0]#, PHLDA#, AD[31:0], C/BE[3:0]#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, SERR#, PLOCK#
5. I_{OL1} and I_{OH1} apply to: BRDY#, NA#, AHOLD, EADS#, BOFF#, KEN#/INV, CADV#, CADS#, CCS#, COE#, GWE#, BWE#, TWE#, A[31:3], T10[10:0], MD[63:0], MPD[7:0]
6. I_{OL2} and I_{OH2} apply to: MWE#, MA[11:2], MAA[1:0], MAB[1:0], RAS[7:0]#, CAS[7:0]#, PHLDA#, GNT[3:0]#, HD[63:0]
7. I_{OL3} and I_{OH3} apply to: MWE#, MA[11:2], MAA[1:0], MAB[1:0] if programmed for 12 mA strength
8. For transient voltages, V_{IL1} min is V_{SS} - 1.4 V. This applies to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#.
9. For transient voltages, V_{IH1} max is VDD3 + 1.7 V. This applies to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#.

1.4 82439HX System Controller (TXC) AC Characteristics

All timings are in nanoseconds (ns), unless otherwise specified.

Table 3. Host Clock Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t1	HCLKIN Period	15.0	20.0	1	
	HCLKIN Period Stability		±100		pS
t3	HCLKIN High Time	6.0		1	
t4	HCLKIN Low Time	6.0		1	
t5	HCLKIN Rise Time		1.2	1	
t6	HCLKIN Fall Time		1.2	1	
	HCLKIN Rising Edge to PCLKIN Rising Edge Skew	1	6		HCLKIN must lead PCLKIN

Table 4. CPU Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C) (Sheet 1 of 2)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t7	ADS# Setup Time to HCLKIN Rising	5.0		4	
t7a	ADS# Hold Time from HCLKIN Rising	1.5		4	
t8	W/R# Setup Time to HCLKIN Rising	5.5		4	
t9	BE[7:0]# Setup Time to HCLKIN Rising	5.0		4	
t10	HITM# Setup Time to HCLKIN Rising	6.0		4	
t11	CACHE# Setup Time to HCLKIN Rising	5.0		4	
t11a	M/IO# Setup Time to HCLKIN Rising	6.0		4	
t12	D/C# Setup Time to HCLKIN Rising	5.0		4	
t13	HLOCK#, SMIACT# Setup Time to HCLKIN Rising	5.0		4	
t14	HITM#, W/R#, M/IO#, D/C#, BE[7:0], HLOCK#, CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.0		4	
t15	A[31:3] Setup Time to HCLKIN Rising	3.0		4	
t16	A[31:3] Hold Time from HCLKIN Rising	1.0		4	
t18	A[31:3] Valid Delay from HCLKIN Rising	2.0	13	3	0 pf

Table 4. CPU Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C) (Sheet 2 of 2)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t21	BRDY# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pf
t22	NA# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pf
t23	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t24	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t25	EADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t26	KEN#/INV Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t30	HD[63:0] Setup Time to HCLKIN Rising	3.0		4	
t31	HD[63:0] Hold Time from HCLKIN Rising	1.5		4	
t32	HD[63:0] Valid Delay from HCLKIN Rising	1.5	7.5	3	0 pf
t33	HD[63:0] Valid Delay from HCLKIN Rising, 66 Mhz ECC enabled	1.5	8.0	3	0 pf
t34	HD[63:0] Valid Delay from HCLKIN Rising, 60 Mhz 4 clk Leadoff, no L2	1.5	7.0	3	0 pf
t35	HD[63:0] Valid Delay from HCLKIN Rising, 66 MHz 5-222	1.5	6.0	3	0 pf

Table 5. Second Level Cache Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
Pipelined Burst SRAMs					
t40	COE# Valid Delay from HCLKIN Rising	2.0	10.0	3	0 pf
t41	TIO [10:0] Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pf
t42	TIO[10:0] Setup time to HCLKIN Rising	3.0		4	
t43	TIO[10:0] Hold time from HCLKIN Rising	2.0		4	
t44	TWE# Valid Delay from HCLKIN Rising	2.0	10.0	3	0 pf
t45	GWE# Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pf
t45a	BWE# Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pf
t46	CCS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t47	CADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t48	CADV# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf

Table 6. DRAM Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Fig.	Notes
		Min	Max		
t50	RAS[4:0]# Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pf
t51	CAS[7:0]# Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pf
t52	MWE# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t53	MA[11:2] Valid Delay from HCLKIN Rising (Read Row Addr)	2.0	9.0	3	0 pf
t54	MAA/B[1:0] Valid Delay from HCLKIN Rising (Read Col Addr burst cycles)	2.0	7.0	3	0 pf
t55	MA[11:2], MAA/B[1:0] Flow Through Delay from HCLKIN Rising (Read Col Addr leadoff)	2.0	8.0	6	0 pF
t56	MA[11:2], MAA/B[1:0] Valid Delay from HCLKIN Rising for a Write Cycle	2.0	10.0	3	0 pF
t57	MD[63:0] Setup Time to HCLKIN Rising	0			
t58	MD[63:0] Setup Time to HCLKIN Rising for ECC cycles	11.0			
t59	MD[63:0], MPD[7:0] Hold Time from HCLKIN Rising	4.0			
t60	MD[63:0], MPD[7:0] Valid Delay from HCLKIN Rising	2.0	8.0		0 pF
t61	MPD[7:0] Setup Time to HCLKIN RISING	0			
t62	MPD[7:0] Setup Time to HCLKIN Rising for ECC cycles	11.0			

Table 7. PCI Clock Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figure	Notes
		Min	Max		
t70	PCLKIN High Time	12.0		1	
t71	PCLKIN Low Time	12.0		1	
t72	PCLKIN Rise Time		3.0	1	
t73	PCLKIN Fall Time		3.0	1	

Table 8. PCI Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t74	AD[31:0] Valid Delay from PCLKIN Rising	2	11	3	Min: 0 pF Max: 50 pF
t75	AD[31:0] Setup Time to PCLKIN Rising	7		4	
t76	AD[31:0] Hold Time from PCLKIN	0		4	
t77	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Valid Delay from PCLKIN Rising	2	11	3	Min: 0 pF Max: 50 pF
t78	C/BE[3:0]#, FRAME#, TRDY#, IRDY#,, STOP#, LOCK#, PAR, DEVSEL# Output Enable Delay from PCLKIN Rising	2		8	
t79	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Float Delay from PCLKIN Rising	2	28	5	
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Setup Time to PCLKIN Rising	7		4	
t81	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Hold Time from PCLKIN Rising	0		4	
t82	PHLDA# Valid Delay from PCLKIN Rising	2	9.0	3	Min: 0 pF Max: 50 pF
t83	PHLD# Setup Time to PCLKIN Rising	12		4	
t84	PHLD# Hold Time from PCLKIN Rising	0		4	
t85	GNT[3:0] # Valid Delay from PCLKIN Rising	2	9.0	3	Min: 0 pF Max: 50 pF
t86	REQ[3:0]# Setup Time to PCLKIN Rising	12		4	
t87	REQ[3:0]# Hold Time from PCLKIN Rising	0		4	
t88	RST# Low Pulse Width	1 ms		7	

1.5 82439HX System Controller (TXC) Timing Diagrams

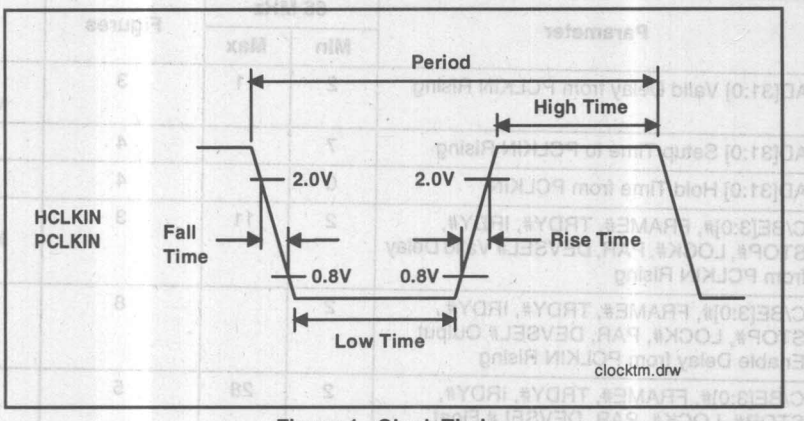


Figure 1. Clock Timing

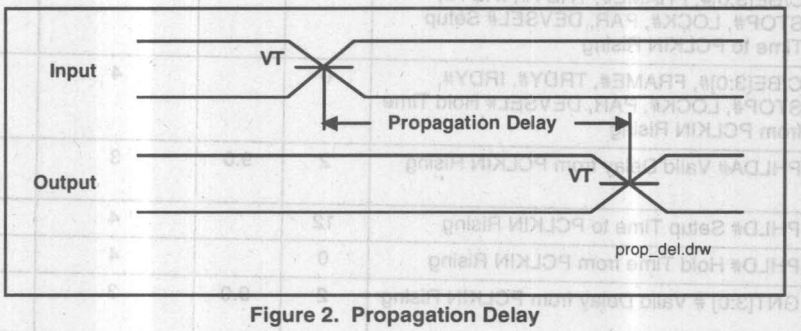


Figure 2. Propagation Delay

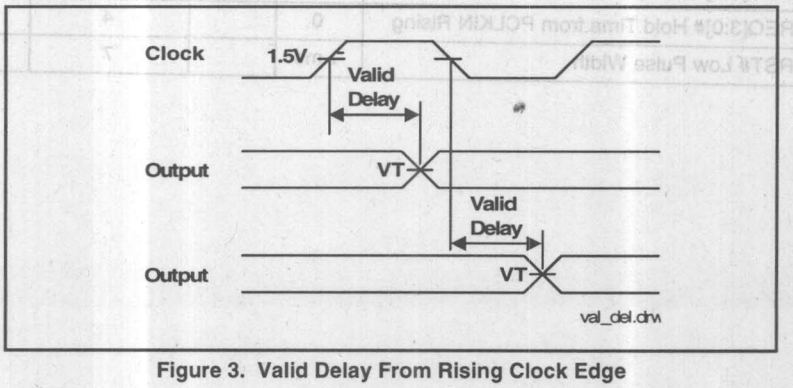


Figure 3. Valid Delay From Rising Clock Edge

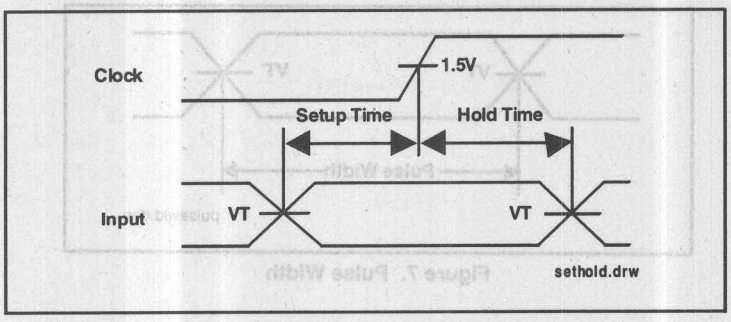


Figure 4. Setup and Hold Times

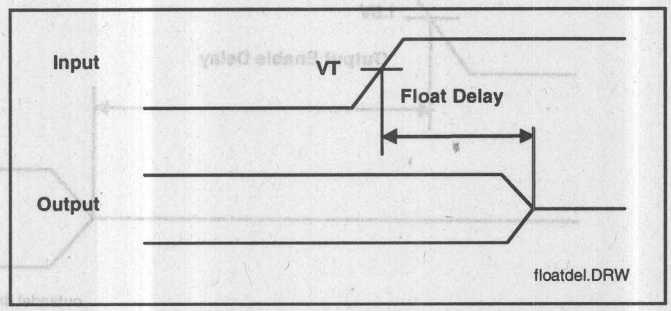
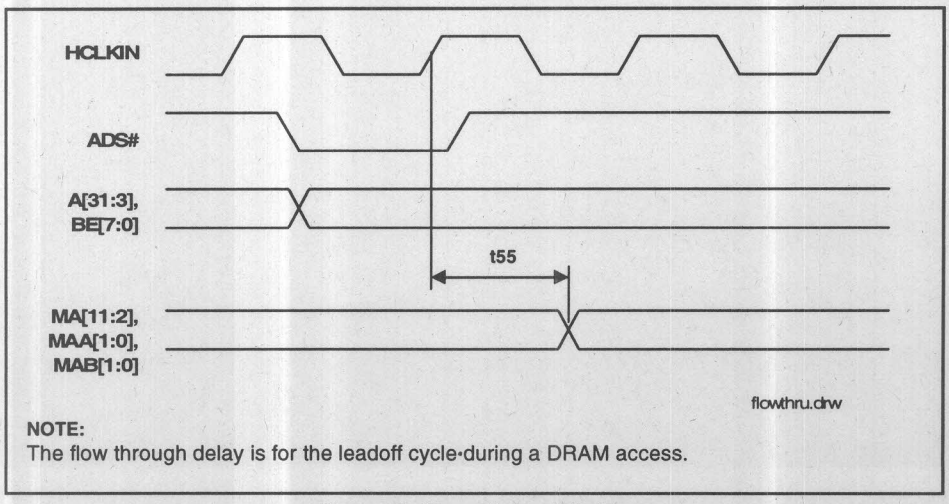


Figure 5. Float Delay



NOTE:
The flow through delay is for the leadoff cycle during a DRAM access.

Figure 6. Flow Through Delay

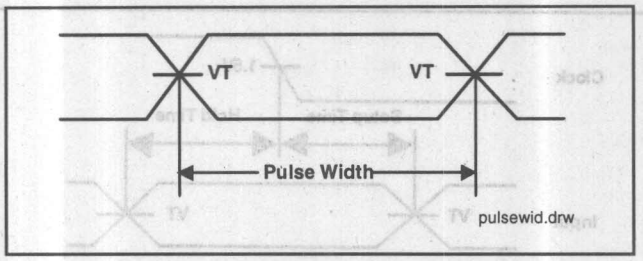


Figure 7. Pulse Width

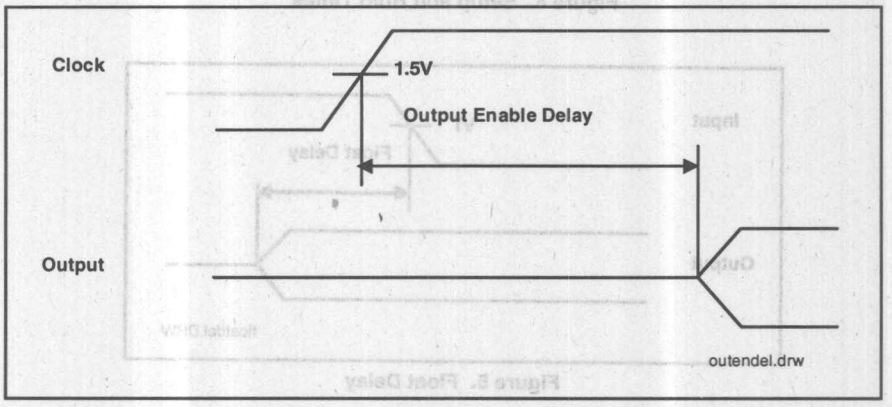


Figure 8. Output Enable Delay

- — Transfer Rates to 22 MB/Sec
- — 8 x 32-Bit Buffer for Bus Master IDE PCI Burst Transfers
- — Separate Master/Slave IDE Mode Support (PIIX3)

- Plug-n-Play Port for Motherboard Devices
  - — 2 Steerable DMA Channels (PIIX Only)
  - — Fast DMA with 4-Byte Buffer (PIIX Only)
  - — 2 Steerable Interrupts Lines on the PIIX and 1 Steerable Interrupt Line on the PIIX3
  - — 1 Programmable Chip Select
- Steerable PCI Interrupts for PCI Device Plug-n-Play
- PCI Specification Revision 2.1 Compliant (PIIX3)
- Functionality of One 82C54 Timer
  - — System Timer; Refresh Request; Speaker Tone Output
- Two 82C59 Interrupt Controller Functions
  - — 14 Interrupts Supported
  - — Independently Programmable for Edge/Level Sensitivity
  - — Controls Lower X-Bus Data Byte Transceiver
- I/O Advanced Programmable Interrupt Controller (IOAPIC) Support (PIIX3)
- Universal Serial Bus (USB) Host Controller (PIIX3)
  - — Compatible with Universal Host Controller Interface (UHCI)
  - — Contains Root Hub with 2 USB Ports
- System Power Management (Intel SMM Support)
  - — Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#
  - — Programmable CPU Clock Control (STPCLK#)
  - — Fast On/Off Mode
- Non-Maskable Interrupts (NMI)
  - — PCI System Error Reporting
- NAND Tree for Board-Level ATE Testing
- 208-Pin QFP

The 82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerators are multi-function PCI devices implementing a PCI-to-ISA bridge function and an PCI IDE function. In addition, the PIIX3 implements a Universal Serial Bus host/hub function. As a PCI-to-ISA bridge, the PIIX/PIIX3 integrates many common I/O functions found in ISA-based PC systems—a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and power management support. In addition to compatible transfers, each DMA channel supports type F transfers. Chip select decoding is provided for BIOS, real time clock, and keyboard controller. Edge/Level interrupts and interrupt steering are supported for PCI plug and play compatibility. The PIIX/PIIX3 supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. The PIIX/PIIX3 provides motherboard plug and play compatibility. PIIX implements two steerable DMA channels (including type F transfers) and up to two steerable interrupt lines. PIIX3 implements one steerable interrupt line. The interrupt lines can be routed to any of the available ISA interrupts. Both PIIX/PIIX3 implement a programmable chip select.

PIIX3 contains a Universal Serial Bus (USB) Host Controller that is UHCI compatible. The Host Controller's root hub has two programmable USB ports. PIIX3 also provides support for an external IOAPIC.

This document describes the PIIX3 Component. Unshaded areas describe the 82371FB PIIX. Shaded areas, like this one, describe the PIIX3 operations that differ from the 82371FB PIIX.

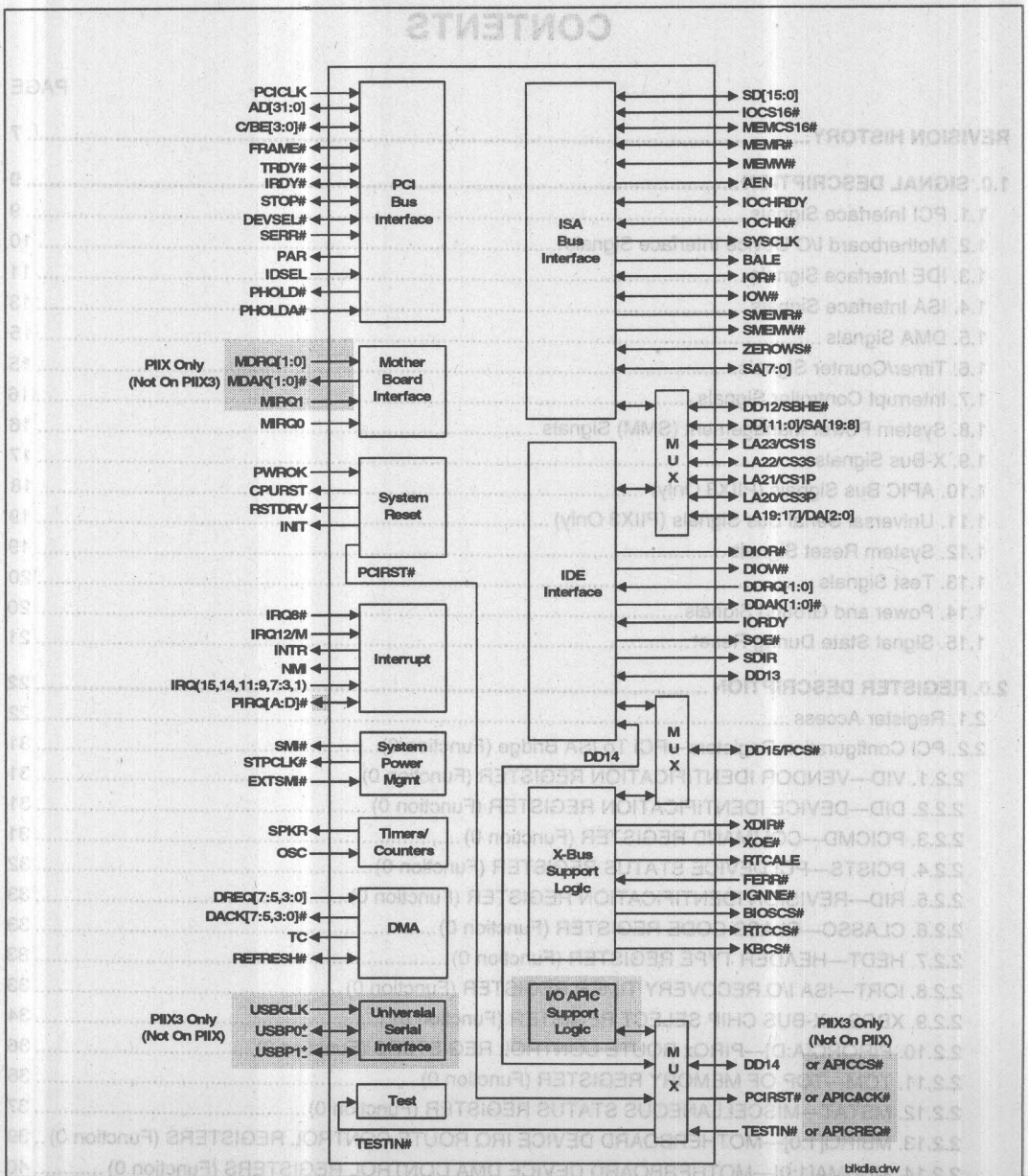
April 1997 Order Number: 290550-002

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Note:
1. IOAPIC signals are multiplexed with signals from the System Reset, Test, and IDE Interface blocks
2. PIRQD# is an input on the PIIX and bi-directional on PIIX3.

PIIX/PIIX3 Simplified Block Diagram

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REVISION HISTORY

Revision Date	Version	Description
May 1996	-001	Initial Release
April 1997	-002	Included information from Specification Update

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(PIIX3)
Timing Specification

272963-002

November, 1997

82371SB PCI ISA IDE Xcelerator (PIIX3)

Timing Specification

272963-002

November, 1997

82371SB (PIIX3) PCI ISA IDE Xcelerator Features

- Bridge Between the PCI Bus and ISA Bus
- PCI and ISA Master/Slave Interface
  - PCI from 25–33 MHz
  - ISA from 7.5–8.33 MHz
  - 5 ISA Slots
- Fast IDE Interface
  - Supports PIO and Bus Master IDE
  - Supports up to Mode 4 Timings
  - Transfer Rates to 22 MByte/Sec
  - 8 x 32-Bit Buffer for Bus Master IDE PCI Burst Transfers
  - Separate Master/Slave IDE Mode Support
- Plug-n-Play Port for Motherboard Devices
  - 1 Steerable Interrupt Line
  - 1 Programmable Chip Select
- Steerable PCI Interrupts for PCI Device Plug-n-Play
- PCI Specification Revision 2.1 Compliant
- Functionality of One 82C54 Timer
  - System Timer; Refresh Request; Speaker Tone Output
- Two 82C59 Interrupt Controller Functions
  - 14 Interrupts Supported
  - Independently Programmable for Edge/Level Sensitivity
- Enhanced DMA Functions
  - Two 8237 DMA Controllers
  - Fast Type F DMA
  - Compatible DMA Transfers
  - 7 Independently Programmable Channels
- X-Bus Peripheral Support
  - Chip Select Decode
  - Controls Lower X-Bus Data Byte Transceiver
- I/O Advanced Programmable Interrupt Controller (IOAPIC) Support
- Universal Serial Bus (USB) Host Controller
  - Compatible with Universal Host Controller Interface (UHCI)
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- NAND Tree for Board-Level ATE Testing
- 208-Pin QFP

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 430HX PCIset. Please refer to the standard package datasheet (order number 290551) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

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  - Supports up to Mode 4 Timings
  - Transfer Rates to 22 MBytes/Sec
  - 8 x 32-Bit Buffer for Bus Master IDE PCI Burst Transfers
  - Separate Master/Slave IDE Mode Support
- Plug-n-Play Port for Motherboard Devices
  - 1 Steerable Interrupt Line
  - 1 Programmable Chip Select
- Steerable PCI Interrupts for PCI Device Plug-n-Play
- PCI Specification Revision 2.1 Compliant
- Functionality of One 82C54 Timer
  - System Timer; Refresh Request; Speaker Tone Output
- Two 82C59 Interrupt Controller Functions
  - 14 Interrupts Supported
  - Independently Programmable for Edge/Level Sensitivity
- Enhanced DMA Functions
  - Two 8237 DMA Controllers
  - Fast Type F DMA
  - Compatible DMA Transfers
  - 7 Independently Programmable Channels
- X-Bus Peripheral Support
  - Chip Select Decode
  - Controls Lower X-Bus Data Byte Transceiver
- I/O Advanced Programmable Interrupt Controller (IOAPIC) Support
- Universal Serial Bus (USB) Host Controller
  - Compatible with Universal Host Controller Interface (UHCI)
  - Contains Root Hub with 2 USB Ports
- System Power Management (Intel SMM Support)
  - Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#
  - Programmable CPU Clock Control (STPCLK#)
  - Fast On/Off Mode
- Non-Maskable Interrupts (NMI)
  - PCI System Error Reporting
- NAND Tree for Board-Level ATE Testing
- 208-Pin QFP

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 430HX PCIset. Please refer to the standard package datasheet (order number 290551) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

1.0 Introduction

This document contains the Electrical and the Thermal Specification (ETS) for the 82371SB (PIIX3), which is a part of the 82440FX, 82430HX, and 82430VX PCIsets. The specifications refer to the 82371SB (PIIX3). The PIIX3 is a multi-function PCI device implementing a PCI-to-ISA bridge function and a PCI IDE function, in addition to integrating a Universal Serial Bus Host/Hub function.

The contents of this document are preliminary based on the first level estimates from simulation. This information will be modified as more data is available.

1.1 References

This documents assumes that the reader is familiar with the following documents:

Document Name	Order Number
Intel 430HX PCIset (TXC) Datasheet	290551
Intel430HX Design Guide	297467
82371FB (PIIX) and 82371SB (PIIX3) Datasheet	290550
Universal Serial Bus Specification	None (available at http://www.teleport.com/~usb)

2.0 Electrical Characteristics

2.1 Absolute Maximum Ratings

Case Temperature under Bias ..... 0°C to +85°C
Storage Temperature ..... -55°C to +150°C
Voltage on Any Pin with Respect to Ground[1] ..... -0.3 V to V_{CC} + 0.3 V
Supply Voltage with Respect to V_{SS} ..... -0.3 V to +6.5 V
3.3 V Supply Voltage with Respect to V_{SS} (V_{CC3}) ..... -0.3 V to +4.3 V
Maximum Power Dissipation ..... 1.0 W

[1] To ensure long term reliability of the device, worst case AC operating conditions on the PCI signals would include support for an overvoltage of +11.0 V and undervoltage of -5.5 V.

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.*

2.2 Thermal Characteristics

The 82371SB (PIIX3) is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the package are given in Table 1.

Table 1. 82371SB (PIIX3) Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/Watt)	34.5	26.1
θ_{jc} (°C/Watt)	12.0	

2.3 DC Characteristics

Table 2. 82371SB (PIIX3) DC Characteristics (Sheet 1 of 2)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL1}	Input Low Voltage	-0.3	0.8	V	
V_{IH1}	Input High Voltage	2.0	V_{CC}/V_{CC3} + 0.3	V	
V_{T1-}	Schmitt Trigger Threshold Voltage, Falling Edge	0.7	1.35	V	1, V_{CC}=5.0 V
V_{T1+}	Schmitt Trigger Threshold Voltage, Rising Edge	1.4	2.2	V	1, V_{CC}=5.0 V
V_{H1}	Hysteresis Voltage	0.3	1.2	V	1, V_{CC}=5.0 V
V_{OL1}	Output Low Voltage		0.4	V	2,3,4,5
V_{OH1}	Output High Voltage	V_{CC}/V_{CC3} - 0.5		V	2,3,4,5
V_{OL2}	Output Low Voltage		0.3	V	7
V_{OH2}	Output High Voltage	2.8	3.6	V	7
V_{DI}	Differential Input Sensitivity	0.2		V	7, |(USBPx+, USBPx-)|
V_{CM}	Differential Common Mode Range	0.8	2.5	V	7, Includes V_{DI}
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	7
I_{OL1}	Output Low Current	4		mA	2
I_{OH1}	Output High Current	-1		mA	2
I_{OL2}	Output Low Current	12		mA	3
I_{OH2}	Output High Current	-3		mA	3

NOTES:

1. V_{T1-}, V_{T1+} and V_{H1} apply to the following signals: IRQx, IOCHK#, ZEROWS#, PWROK.
2. I_{OL1}, I_{OH1} apply to the following signals (V_{OL1} pertains to the I_{OL1} condition and V_{OH1} pertains to the I_{OH1} condition): DD[15,13:0], APICCS#/DD14, PHOLD#, DDAK[1:0]#, IGNNE#, INTR, SMI#, STPCLK#, CPURST#, INIT, NMI, TC, DREQ[7:5,3:0], DACK[7:5,3:0]#, REFRESH#, SDIR, SOE#, BIOSCS#, RTCCS#, KBCS#, XOE#, XDIR, MIRQ[0], RTCALE, PIRQ[D:A].
3. I_{OL2}, I_{OH2} apply to the following signals (V_{OL1} pertains to the I_{OL2} condition and V_{OH1} pertains to the I_{OH2} condition): SYSCLK, SD[15:0], IOCHRDY, SMEMR#, AEN, SMEMW#, IOR#, IOW#, RSTDRV, SA[7:0], BALE, MEMCS16#, LA[23:17], MEMR#, MEMW#, SPKR, DIOW#, DIOR.
4. I_{OL3}, I_{OH3} apply to the following signals (V_{OL1} pertains to the I_{OL3} condition and V_{OH1} pertains to the I_{OH3} condition): AD[31:0], C/BE[3:0]#, PCIRST#/APICACK#.
5. I_{OL4}, I_{OH4} apply to the following signals (V_{OL1} pertains to the I_{OL4} condition and V_{OH1} pertains to the I_{OH4} condition): FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR.
6. These signals have weak internal pull-up resistors.
7. These parameters apply to USBP [1:0]+, USBP [1:0]-. I_{OL5}, I_{OH5} apply to the following signals (V_{OL2}, pertains to the I_{OL5} condition and V_{OH2} pertains to the I_{OH5} condition): USBP[1:0]+, USBP[1:0]-. The V_{OL2} assumes R_L of 1.5 KΩ to 3.6 V and V_{OH2} assumes R_L of 15 KΩ to GND.

Table 2. 82371SB (PIIX3) DC Characteristics (Sheet 2 of 2)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
I_{OL3}	Output Low Current		3	mA	4
I_{OH3}	Output High Current	-2		mA	4
I_{OL4}	Output Low Current		6	mA	5
I_{OH4}	Output High Current	-2		mA	5
I_{OL5}	Output Low Current		2	mA	7
I_{OH5}	Output High Current	-0.25		mA	7
I_{LI1}	Input Leakage Current		±1	µA	All, except I_{LI2} I_{LI3} and I_{LI4}
I_{LI2}	Input Leakage Current		±300	µA	TC (note 6)
I_{LI3}	Input Leakage Current		±250	µA	EXTSMI#, TESTIN# (note 6)
I_{LI4}	Hi-Z State Data Line Leakage	-10	+10	µA	7, 0 V< V_{IN}< 3.3 V
I_{CC}	V_{CC} Supply Current		155	mA	
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. V_{T1-}, V_{T1+} and V_{H1} apply to the following signals: IRQx, IOCHK#, ZEROWS#, PWROK.
2. I_{OL1}, I_{OH1} apply to the following signals (V_{OL1} pertains to the I_{OL1} condition and V_{OH1} pertains to the I_{OH1} condition): DD[15,13:0], APICCS#/DD14, PHOLD#, DDAK[1:0]#, IGNNE#, INTR, SMI#, STPCLK#, CPURST#, INIT, NMI, TC, DREQ[7:5,3:0], DACK[7:5,3:0]#, REFRESH#, SDIR, SOE#, BIOSCS#, RTCCS#, KBCS#, XOE#, XDIR, MIRQ[0], RTCALE, PIRQ[D:A].
3. I_{OL2}, I_{OH2} apply to the following signals (V_{OL1} pertains to the I_{OL2} condition and V_{OH1} pertains to the I_{OH2} condition): SYSCLK, SD[15:0], IOCHRDY, SMEMR#, AEN, SMEMW#, IOR#, IOW#, RSTDRV, SA[7:0], BALE, MEMCS16#, LA[23:17], MEMR#, MEMW#, SPKR, DIOW#, DIOR.
4. I_{OL3}, I_{OH3} apply to the following signals (V_{OL1} pertains to the I_{OL3} condition and V_{OH1} pertains to the I_{OH3} condition): AD[31:0], C/BE[3:0]#, PCIRST#/APICACK#.
5. I_{OL4}, I_{OH4} apply to the following signals (V_{OL1} pertains to the I_{OL4} condition and V_{OH1} pertains to the I_{OH4} condition): FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR.
6. These signals have weak internal pull-up resistors.
7. These parameters apply to USBP [1:0]+, USBP [1:0]-. I_{OL5}, I_{OH5} apply to the following signals (V_{OL2}, pertains to the I_{OL5} condition and V_{OH2} pertains to the I_{OH5} condition): USBP[1:0]+, USBP[1:0]-. The V_{OL2} assumes R_L of 1.5 KΩ to 3.6 V and V_{OH2} assumes R_L of 15 KΩ to GND.

2.4 AC Characteristics

Table 3. Clock/Reset Timings (Sheet 1 of 2)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
PCI Clock Timings						
	PCICLK					
t1a	Period	30	40	ns		2
t1b	High Time	12.0		ns		2
t1c	Low Time	12.0		ns		2
t1c	Rise Time		3.0	ns		2
t1d	Fall Time		3.0	ns		2
ISA Clock Timings						
	SYSCLK					
t1f	Period	120	125	ns		2
t1g	High Time	49		ns		2
t1h	Low time	49		ns		2
t1i	Rise Time		4	ns		2
t1j	Fall time		4	ns		2
Oscillator Clock Timings						
t1k	**OSC**					
t1l	OSC Period	67	70	ns		2
t1m	High Time	20				2
t1n	Low time	20		ns		2
USB Clock Timings						
f_{clk48}	**Operating Frequency**	48		MHz		
t1p	Frequency Tolerant		±2500	ppm	1	
t1q	High Time	7		ns		2
t1r	Low Time	7		ns		2
t1s	Rise Time		1.2	ns		2
t1t	Fall Time		1.2	ns		2
f_{clk24}	**Operating Frequency**	24		MHz		
t1p	Frequency Tolerant		±2500	ppm	1	
t1q	High Time	17.5		ns		2

NOTE:

1. The USBCLK is 24 MHz or 48 MHz that expects a 45/55% duty cycle for 24 MHz and 40/60% duty cycle for 48 MHz.

Table 3. Clock/Reset Timings (Sheet 2 of 2)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t1r	Low Time	17.5		ns		2
t1s	Rise Time		1.2	ns		2
t1t	Fall Time		1.2	ns		2
	Reset Timings					
t2a	-PCIRST#, RSTDRV Driven Inactive After PWROK is Driven Active High	1		ms		3
	- CPURST Driven Inactive After PWROK is Driven Active High	2		ms		
t2b	CPURST, PCIRST#, RSTDRV Active Pulse Width. Initiated via the RC Register	1		ms		4
t2c	CPURST Valid Delay from PCICLK Rising	3	17	ns		30

NOTE:
1. The USBCLK is 24 MHz or 48 MHz that expects a 45/55% duty cycle for 24 MHz and 40/60% duty cycle for 48 MHz.

Table 4. System Power Management Timings

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to + 85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
	SMI#					
t3a	Valid Delay from PCICLK	2	11	ns		7
t3b	Active Pulse Width	3		PCLKIN		5
t3c	Inactive Pulse Width	4		PCLKIN		5
	EXTSMI#					
t3d	Active Pulse Width	2		PCLKIN		5
t3e	Inactive Pulse Width	4		PCLKIN		5
t3f	Valid Setup to PCICLK	10		ns		6
t3g	Valid Hold from PCICLK	2		ns		6
	STPCLK#					
t3h	Valid Delay from PCICLK	2	11	ns		7
t3i	STPCLK# Inactive Pulse Width	5		PCLKIN		5

Table 5. ISA Bus and X-Bus Timings (Sheet 1 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
PIIX3 AS MASTER TIMINGS								
	BALE							
t4a	BALE Pulse Width	50		ns	M,I/O	8,16		8,9,10,11
t4b	BALE Driven Active from MEMx#, IOx# Inactive	44		ns	M,I/O	8,16		8,9,10,11
	LA[23:17]							
t5a	LA[23:17] Valid Setup to BALE Inactive	150		ns	M	8,16	7	8,9
t5b	LA[23:17] Valid Hold from BALE Inactive	26		ns	M	8,16		8,9
t5c	LA[23:17] Valid Setup to MEMx# Active	150		ns	M	16		9
t5d	LA[23:17] Valid Setup to MEMx# Active	173		ns	M	8		8
t5e	LA[23:17] Invalid from MEMx# Active	39		ns	M	16		9
t5f	LA[23:17] Invalid from MEMx# Active	39		ns	M	8		8
	SA[19:0], SBHE#							
t6a	SA[19:0], SBHE# Valid Setup to MEMx# Active	34		ns	M	16	13,15	9
t6b	SA[19:0], SBHE# Valid Setup to IOx# Active	100		ns	I/O	16		11
t6c	SA[19:0], SBHE# Setup to MEMx#, IOx# Active	100		ns	M,I/O	8		8,10
t6d	SA[19:0], SBHE# Valid Setup to BALE Inactive	37		ns	M,I/O	8,16	13,15	8,9,10,11
t6e	SA[19:0], SBHE# Valid Hold from MEMx#, IOx# Inactive	41		ns	M,I/O	8,16		8,9,10,11
	MEMR#, MEMW#, IOR# AND IOW#							
t7a	MEMx# Active Pulse Width (std)	225		ns	M	16		9
t7b	IOx# Active Pulse Width (std)	160		ns	I/O	16		11
t7c	MEMx# Active Pulse Width (nws)	105		ns	M	16	1	9
t7d	MEMx# or IOx# Active Pulse Width (std)	520		ns	M,I/O	8		8,10
t7e	MEMx# or IOx# Active Pulse Width (nws)	160		ns	M,I/O	8	1	8,10
t7f	MEMx# Inactive Pulse Width	103		ns	M	16		9
t7g	MEMx# Inactive Pulse Width	163		ns	M	8		8

†Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 2 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
t7h	IOx# Inactive Pulse Width	163		ns	I/O	8,16		10,11
t7i	MEMx#, IOx# Driven Inactive from IOCHRDY Active	120		ns	M,I/O	8,16		8,9,10,11
	SMEMR# and SMEMW#							
t8a	SMEMR# & SMEMW# Propagation Delay from MEMR# and MEMW#		16	ns	M	8,16		8,9
	Read Data							
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O	8,16		8,9,10,11
t9b	Read Data Valid Setup to MEMR#, IOR#	24		ns	M,I/O	8,16		8,9,10,11
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		8,9,10,11
t9d	Read Data Three-stated from MEMR# and IOR# Inactive		41	ns	M,I/O	8,16		8,9,10,11
	Write Data							
t10a	Write Data Valid Setup to MEMW# Active	-40		ns	M,I/O	8,16		8,9,10,11
	Write Data Valid Setup to IOW# Active	-40		ns	M,I/O	8		
	Write Data Valid Setup to IOW# Active	+23		ns	M,I/O	16		
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O	8,16		8,9,10,11
t10c	Write Data Three-Stated from MEMW#, IOW# Inactive		105	ns	M,I/O	8,16		8,9,10,11
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O	8,16		8,9,10,11
	MEMCS16#							
t11a	MEMCS16# Driven Active from LA[23:17] Valid		94	ns	M	16		9
t11b	MEMCS16# Inactive from LA[23:17] Valid		91	ns	M	8		8,9
t11c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		9
t11d	MEMCS16# Driven Active from SA[19:2] Valid		35	ns	M	16		9

†Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 3 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	IOCS16#							
t12a	IOCS16# Driven Active from Valid SA[19:0]		123	ns	I/O	16		11
t12b	IOCS16# Inactive from Valid SA[19:0]		91	ns	I/O	8		10,11
t12c	IOCS16# Valid Hold from SA[19:0] Invalid	0		ns	I/O	16		11
t12d	IOCS16# Driven Active from IOx Active		80	ns	I/O	16		11
	ZEROWS#							
t13a	ZEROWS# Driven Active from MEMx# Active		16	ns	M	16		9
t13b	ZEROWS# Driven Active from MEMx#, IOx# Active		80	ns	M,I/O	8		8,10
t13c	ZEROWS# Driven Active from LA[23:17] Valid		180	ns	M	16		9
t13d	ZEROWS# Driven Active from LA[23:17] Valid		300	ns	M	8		8
t13e	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		80	ns	M	16		9
t13f	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		200	ns	M,I/O	8		8,10
	AEN							
t14a	AEN Valid Setup to IOx# Driven Active	111		ns	I/O	8,16		10,11
t14b	AEN Valid Setup to BALE Driven Inactive	111		ns	I/O	8,16		10,11
t14c	AEN Valid Hold from IOx# Driven Inactive	41		ns	I/O	8,16		10,11
	IOCHRDY							
t15a	IOCHRDY Driven Valid from MEMx#, IOx# Active		78	ns	M,I/O	16		9,11
t15b	IOCHRDY Driven Valid from MEMx#, IOx# Active		366	ns	M,I/O	8		8,10
t15e	IOCHRDY Inactive Pulse Width	120	15.6	µs	M,I/O	8,16		8,9,10,11
PIIX3 AS SLAVE TIMINGS								
	LA[23:17]							
t16a	LA[23:17] Valid Setup to MEMx# Active	23		ns	M	16		12

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 4 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	SA[19:0],SBHE#							
t17a	SA[19:0],SBHE# Setup to MEMx# Active	23		ns	M	16		12
t17b	SA[19:0],SBHE# Setup to IOx# Active	89		ns	I/O	8		13
t17c	SA[19:0],SBHE# Valid Hold from MEMx#, IOx# Inactive	30		ns	M,I/O	8,16		12,13
	MEMR#, MEMW#, IOR#, IOW#							
t18a	MEMx# Active Pulse Width	214		ns	M	16		12
t18b	IOx# Active Pulse Width	509		ns	I/O	8		13
t18c	MEMx# Inactive Pulse Width	92		ns	M	16		12
t18d	IOx# Inactive Pulse Width	152		ns	I/O	8		13
	Read Data							
t19a	Read Data Valid from IOCHRDY Active		69	ns	M,I/O	8,16		12,13
t19b	Read Data Valid from IOR# Active		69	ns	I/O	8	11	13
t19c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		12,13
t19d	Read Data Three-State from MEMR#, IOR# Inactive		55	ns	M,I/O	8,16		12,13
	Write Data							
t20a	Write Data Valid Setup to MEMW#, IOW# Active	-54		ns	M,I/O	8,16		12,13
t20b	Write Data Valid Hold from MEMW#, IOW# Inactive	14		ns	M,I/O	8,16		12,13
	MEMCS16#							
t21a	MEMCS16# Driven Active from Valid LA[23:17]		65	ns	M	16		12
t21b	MEMCS16# Float from Valid LA[23:17]		31	ns	M	16		12
t21c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		12
	IOCHRDY							
t22a	IOCHRDY Inactive from MEMx#, IOx# Active		50	ns	M,I/O	8,16		12,13
t22b	IOCHRDY Float from IOCHRDY Rising		85	ns	M,I/O	8,16	4	12,13
t22c	IOCHRDY Inactive Pulse Width	120	2.5	µs	M,I/O	8,16		12,13

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 5 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
Interrupt and NMI Timings								
	NMI Timing							
t23a	SERR#, IOCHK# Active to NMI Driven Active		200	ns				14
	Interrupt Timing							
t24a	IRQx, MIRQ0 Inactive Pulse Width	100		ns				15
ISA Bus Master Timings								
	DACK#							
t26a	DACK#, Inactive from DREQ Inactive	240		ns				16
	Three-Stating and Driving the Bus							
t27a	PIIX3 Three-States Address, Data, and Control Signals from DACK#, Active	0	30	ns				16
t27b	PIIX3 Drives Address, Data, and Control Signals from DACK#, Inactive	71		ns				16
	SMEMR# and SMEMW#							
t28a	SMEMR# & SMEMW# Active (falling edge) from MEMR# and MEMW# Active (falling edge)		25	ns				16
t28b	SMEMR# & SMEMW# Inactive (rising edge) from MEMR# and MEMW# Inactive (rising edge)		35	ns				16
Data Swap Logic Timing (ISA Master to ISA Slave)								
t29a	SD[7:0] to SD[15:8] Propagation Delay		26	ns				17
t29b	SD[15:8] to SD[7:0] Propagation Delay		26	ns				17
t29c	PIIX3 Drives Data Bus from IOR#, IOW#, MEMR# or MEMW# Active		26	ns			2	17
t29d	PIIX3 Three-States Bus from IOR#, MEMR#, or SMEMR# Inactive	2	55	ns			2,3	17
t29e	PIIX3 Three-States Bus from IOW#, MEMW#, or SMEMW# Inactive	2	60	ns			2,3	17

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 6 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
DMA Compatible Timings								
	DREQ							
t30a	DREQ Active Hold from IOR# Active		558	ns			5	19
t30b	DREQ Active Hold from IOW# Active		315	ns			5	18
	DACK#							
t31a	DACK# Active to IOR# Active	73		ns				19
t31b	DACK# Active to IOW# Active	312		ns				18
t31c	DACK# Active Hold from IOR# Inactive	100		ns				19
t31d	DACK# Active Hold from IOW# Inactive	155		ns				18
	AEN and BALE							
t32a	AEN Active to IOx# Active	111		ns				18,19
t32b	AEN and BALE Inactive from IOx# Inactive	41		ns				18,19
	LA[23:19], SA[19:0], SBHE#							
t33a	LA[23:19],SA[19:0], SBHE# Valid Setup to MEMx# Active	99		ns				18,19
t33b	LA[23:19],SA[19:0], SBHE# Valid Hold from MEMx# Inactive	51		ns				18,19
	MEMR#, MEMW#, IOR#, IOW#							
t34a	IOW# and MEMW# Active Pulse Width	465		ns				18,19
t34b	MEMR# Active Pulse Width	495		ns				18
t34c	IOR# Active Pulse Width	760		ns				19
t34d	IOW# Inactive Pulse Width (continuous)	465		ns				18
t34e	IOR# Inactive Pulse Width (continuous)	160		ns				19
t34f	IOR# Active to MEMW# Active	230		ns				19
t34g	MEMR# Active to IOW# Active	-26		ns				18
t34h	MEMR# Active Hold from IOW# Inactive	40		ns				18
t34i	IOR# Active Hold from MEMW# Inactive	40		ns				19
t34j	MEMx# Active Hold from IOCHRDY Active	120		ns				18,19
	SMEMR# and SMEMW#							
t35a	SMEMR# & SMEMW# Valid from MEMR# and MEMW# Valid		15	ns				18,19

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 7 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	Read Data							
t36a	Read Data Valid from IOR# Active		237	ns				19
t36b	Read Data Valid Hold from IOR# Inactive	0		ns				19
t36c	Read Data Float from IOR# Inactive		61	ns				19
	Write Data							
t37a	Write Data Valid Setup to IOW# Inactive	225		ns				18
t37b	Write Data Valid Hold from IOW# Inactive	36		ns				18
	Data Swap Logic Timing (ISA to ISA Transaction)							
t38a	SD[7:0] to SD[15:8] Propagation Delay		26	ns				20
t38b	SD[15:8] to SD[7:0] Propagation Delay		26	ns				20
t38c	PIIX3 Drives Data Bus from IOR# or MEMR# Active		26	ns			2	20
t38d	PIIX3 Three-States Bus from IOR# or MEMR# Inactive		55	ns			2	20
	TC							
t39a	TC Active Setup to IOx# Inactive	511		ns			6	18,19
t39b	TC Active Hold from IOx# Inactive	71		ns			6	18,19
t39h	TC Pulse Width	700		ns				18,19
	IOCHRDY							
t40b	IOCHRDY Valid from MEMx# Active		315	ns				18,19
t40c	IOCHRDY Inactive Pulse Width	125		ns				18,19
	DMA Type "F" Timings							
	DREQ							
t55a	DREQ Active Hold from IOR# Active		82	ns			5, 16	21
t55b	DREQ Active Hold from IOW# Active		82	ns			5, 16	21
	DACK#							
t56a	DACK# Active to IOR# Active	77		ns			16	21
t56b	DACK# Active to IOW# Active	77		ns			16	21
t56c	DACK# Active Hold from IOR# Inactive	30		ns			16	21
t56d	DACK# Active Hold from IOW# Inactive	30		ns			16	21

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 8 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	AEN and BALE							
t57a	AEN Active to IOx# Active	111		ns				21
t57b	AEN and BALE Inactive from IOx# Inactive	41		ns				21
	IOR# and IOW#							
t58a	IOR# Active Pulse Width	110		ns				21
t58b	IOW# Active Pulse Width	110		ns				21
t58c	IOR# Inactive Pulse Width (Continuous)	115		ns				21
t58d	IOW# Inactive Pulse Width (Continuous)	115		ns				21
	Read Data							
t59a	Read Data Valid from IOR# Active		96	ns				21
t59b	Read Data Valid Hold from IOR# Inactive	2		ns				21
t59c	Read Data Float from IOR# Inactive		61	ns				21
	Write Data							
t60a	Write Data Valid Setup to IOW# Inactive	70		ns				21
t60b	Write Data Valid Hold from IOW# Inactive	31		ns				21
	TC							
t61a	TC Active Setup to IOR# Inactive	40		ns			6	21
t61b	TC Active Setup to IOW# Inactive	40		ns			6	21
t61c	TC Active Hold from IOx# Inactive	0		ns			6	21
ISA Refresh Timings								
	REFRESH#							
t62a	REFRESH# Active Setup to MEMR# Active	120		ns				22,23
t62b	REFRESH# Active Hold from MEMR# Inactive	31	218	ns				22,23
t62c	REFRESH# Driven Active to SA[15:0] Valid	11		ns				22,23
t62d	REFRESH# Active Hold from SA[15:0] Invalid	11		ns				22,23

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 9 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	AEN							
t63a	AEN Driven Active to MEMR# Active	11		ns				22,23
t63b	AEN Hold from MEMR# Inactive	11		ns				22,23
	SA[15:0]							
t64a	SA[15:0] Valid Setup to MEMR# Active	72		ns				22,23
t64b	SA[15:0] Valid Hold from MEMR# Inactive	35		ns				22,23
t64c	SA[15:0] Valid Float from MEMR# Inactive	46	120	ns			8	23
	MEMR#, SMEMR#							
t65a	MEMR# Active Pulse Width	225		ns				22,23
t65b	MEMR# Three-state from MEMR# Inactive	36	120	ns				22,23
t65c	MEMR# Driven Inactive from IOCHRDY Active	120		ns				22,23
t65d	SMEMR# Propagation Delay from MEMR#		25	ns				22,23
	IOCHRDY							
t66a	IOCHRDY Inactive from MEMR# Active		76	ns				22,23
t66b	IOCHRDY Valid from MEMR# Active		76	ns				22,23
t66c	IOCHRDY Active to Inactive	120		ns				22,23
	PIIX3 Driving Bus From REFRESH#							
t67a	PIIX3 Drives Control and Address from REFRESH# Active	5		ns			8	23
	PIIX3 and ISA Master Accesses to the X-Bus							
	BIOSCS#, KBCCS#, RTCCS#, AND PCS#							
t68a	CS# Driven Active from SA[19:0], LA[23:17] Valid		35	ns				24
t68b	CS# Driven Inactive from SA[16:0], LA[23:17] Invalid		35	ns				24

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 10 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	XDIR# and XOE#							
t69a	XDIR# Active from IOR#, MEMR# Active							24
	- PCI-Initiated Access		25	ns				
	- ISA-Initiated Access		35	ns				
t69b	XOE# Active from IOx#, MEMx# Active		29	ns				24
t69c	XDIR# Active Setup to XOE# Active	-2	8	ns				24
t69d	XOE# Inactive from IOx#, MEMx# Inactive	35	60	ns			9	24
t69e	XDIR# Inactive from IOR#, MEMR# Inactive	45	100	ns			9	24
t69f	XOE# Setup to XDIR# Inactive	7	45	ns			9	24
t69g	XOE# Inactive from SA[16:0] and LA[23:17]		25	ns			10	24
t69h	XDIR# Inactive from IOR#, MEMR# Inactive	13	60	ns			10	24
	DMA Accesses To X-Bus							
	XDIR#							
t70a	XDIR# Active from DACKx#, MDAKx# Active		25	ns			12, 14	25
t70b	XDIR# Inactive from DACKx#, MDAKx# Inactive	8	65	ns			12	25
	Miscellaneous X-Bus Timings							
	Mouse Timing Support							
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns				26

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 5. ISA Bus and X-Bus Timings (Sheet 11 of 11)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes†**	**Fig**
	Coprocessor Error Support							
t73a	IGNNE# Active from IOW# Active from Port F0H Access		220	ns				26
t73b	IGNNE# Inactive from FERR# Inactive		230	ns				26
	Real Time Clock Timing (RTCALE)							
t75a	RTCALE Pulse Width	200	300	ns				27
t75b	RTCALE Active from IOW# Active PCI-initiated Access ISA-Initiated Access		 85 156	 ns ns				27
	Speaker Timing							
t76a	SPKR Valid Delay from OSC Rising		200	ns				28

† Refer to the corresponding entry in Table 6 (page 17) for all notes.

Table 6. Notes to Table 5, "ISA and X-Bus Timings"

1. No-wait-state (ZEROWS#) asserted.
2. This applies to the byte lane that the data has been swapped to.
3. Data is three-stated from the standard memory commands (SMEMR# or SMEMW#) when they are generated.
4. This specification includes both the time the PIIX3 drives IOCHRDY active and the time it takes the PIIX3 to float IOCHRDY.
5. This applies to the last cycle of a demand mode DMA transfer.
6. Output from PIIX3.
7. 36 ns have been added to the ISA specification to meet ZEROWS# setup requirements.
8. This applies to ISA Master-initiated refresh only.
9. PIIX3 as a master cycle only.
10. ISA Master cycles only.
11. This applies to the PIIX3 cycles in which IOCHRDY is not driven low.
12. This applies to all DACK# signals.
13. 56 ns have been added to the ISA spec to meet MEMCS16# setup requirements. ISA devices generally do not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
14. X-Bus read.
15. For back-to-back "sub cycles" generated as a result of byte assembly or disassembly, this spec is 34 ns.
16. Type F transfers are selected via the MBDMAX register.

Table 7. PCI Interface Timing

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t77	AD[31:0] Valid Delay	2	11	ns	Min: 0 pF Max: 50 pF	30
t78	AD[31:0] Setup Time	7		ns		31
t79	AD[31:0] Hold Time	0		ns		31
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Valid Delay from PCLKIN Rising	2	11	ns	Min: 0 pF Max: 50 pF	30
t81	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Output Enable Delay from PCLKIN Rising	2		ns		34
t82	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# Float Delay from PCLKIN Rising	2	28	ns		32
t83	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# Setup Time to PCLKIN Rising	7		ns		31
t84	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# Hold Time from PCLKIN Rising	0		ns		31
t85	PHLD# Valid Delay from PCICLK Rising	2	12	ns	0 pF	30
t86	PHLDA# Setup Time to PCICLK Rising	10		ns		31
t87	PHLDA# Hold Time from PCICLK Rising	0		ns		31
t91	PIRQ[D:A]# Setup Time to PCICLK Rising				1	31
t92	PIRQ[D:A]# Hold Time From PCICLK Rising				1	31
t96	RST# Low Pulse Width	1		ms		33

NOTE:

1. This signal is internally synchronized.

Table 8. PCI Bus IDE Timing

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t102	DD[15:0] Valid Delay from PCICLK	2	20	ns		35,36
t103	DD[15:0] Setup to PCICLK	10		ns		35,36
t104	DD[15:0] Hold from PCICLK	2		ns		35,36
t105	DA[2:0] Valid Delay from PCICLK	2	20	ns		35
t108	SDIR# Valid Delay from PCICLK Rising	2	20	ns		35,36
t109	SOE# Valid Delay from PCICLK Rising	2	20	ns		35,36
t110	DIOx# Valid Delay from PCICLK Rising	2	20	ns		35,36
t111	CS1P#, CS3P#, CS1S#, CS3S# Valid Delay from PCICLK Rising	2	20	ns		35
t113	IORDY Setup to PCICLK Rising			ns	3	35
t114	IORDY Hold From PCICLK Rising			ns	3	35
t116	DDRQ[1:0] Setup Time to PCICLK Rising	10		ns		36
t117	DDRQ[1:0] Hold From PCICLK Rising	2		ns		36
t118	DDAK[1:0]# Valid Delay From PCICLK Rising	2	20	ns		36
t119	DIOx# Active Pulse Width			PCICLK	1,4	35,36
t120	DIOx# Inactive Pulse Width			PCICLK	2,4	35,36
t121	IORDY Sample Point From DIOx# Assertion			PCICLK	1,4	35

NOTES:

1. This parameter is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register.
2. This parameter is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.
3. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
4. The cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIME0/1 fields in the IDE timing register.

Table 9. Universal Serial Bus Timing (Sheet 1 of 2)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
	Full Speed Source (Note 7)					
t122	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	37
t123	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	37
t124	Source Differential Driver Jitter				2, 3	38
	To Next Transition	-2	2	ns		
	For Paired Transitions	-1	1	ns		
t125	Source EOP Width	160	175	ns	4	39
t126	Differential to SE0 Transition Skew	-2	5	ns	5	
t127	Receiver Data Jitter Tolerance				3	38
	To Next Transition	-20	20	ns		
	For Paired Transitions	-10	10	ns		
t128	EOP Width				4	39
	Must reject as EOP	40		ns		
	Must accept as EOP	85		ns		
t126	Differential to SE0 Transition Skew	-2	5	ns	5	
	Low Speed Source (Note 8)					
t127	USBPx+, USBPx- Driver Rise Time				1, 6	37
		75		ns	C_L = 50 pF	
			300	ns	C_L = 350 pF	
t128	USBPx+, USBPx- Driver Fall Time				1, 6	37
		75		ns	C_L = 50 pF	
			300	ns	C_L = 350 pF	
t129	Source Differential Driver Jitter				2, 3	38
	To Next Transition	-2	2	ns		
	For Paired Transitions	-1	1	ns		

NOTE:

1. Driver output resistance under steady state drive is specified at 28 Ω at minimum and 43 Ω at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

Table 9. Universal Serial Bus Timing (Sheet 2 of 2)

Functional Operating Range (V_{CC} = 5 V ± 5%, V_{CC3} = 3.3 V ± 0.3 V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t130	Source EOP Width	160	175	ns	4	39
t131	Differential to SE0 Transition Skew	-2	5	ns	5	
t132	Receiver Data Jitter Tolerance				3	38
	To Next Transition	-20	20	ns		
	For Paired Transitions	-10	10	ns		
t133	EOP Width				4	39
	Must reject as EOP	40		ns		
	Must accept as EOP	85		ns		
t134	Differential to SE0 Transition Skew	-2	5	ns	5	

NOTE:

1. Driver output resistance under steady state drive is specified at 28 Ω at minimum and 43 Ω at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

Table 10. IOAPIC Bus Timing

Functional Operating Range (V_{CC} = 5 V ± 5%, T_{CASE} = 0°C to + 85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t136	APICCS# Setup to MEMx#	2		PCICLK	1	40
t137	SA[19:0] Setup to APICCS#	2		PCICLK	1	40
t138	APICACK# Valid Delay from PCICLK	2.0	9.0	ns		30
t139	APICREQ# Valid Setup to PCICLK	10.0		ns		31
t140	APICREQ# Valid Hold from PCICLK	0.0		ns		31

NOTE:

1. With these exceptions the APIC configuration cycles conform to the 8-bit ISA Memory Slave Timing where PIIX3 is the master.

Table 11. A.C. Test Signals

Capacitive Load	Signals
120 pf	REFRESH#, TC, SD[15:0], SA[19:0], SBHE#, LA[23:17], IOCS16#, MEMCS16#, MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW#, AEN, BALE, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK
50 pf	DACK#[7:5,3:0], SPKR, INTR, NMI, BIOSCS#, KBCCS#, RTCCS#, RTCALE, XDIR#, XOE#, IGNNE#, SOE#, SDIR#, DD[15,13:0], DD14/APICCS#, DIOR#, DIOW#, DDAK[1:0]#, CS1S#, CS3S#, CS1P#, CS3P#, DA[2:0]

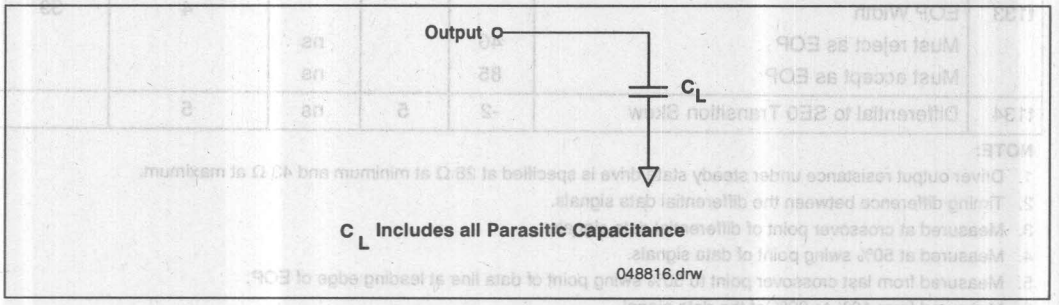


Figure 1. Test Load

2.5 Clock, Reset, ISA Bus, X-Bus, and Host Timing Diagrams

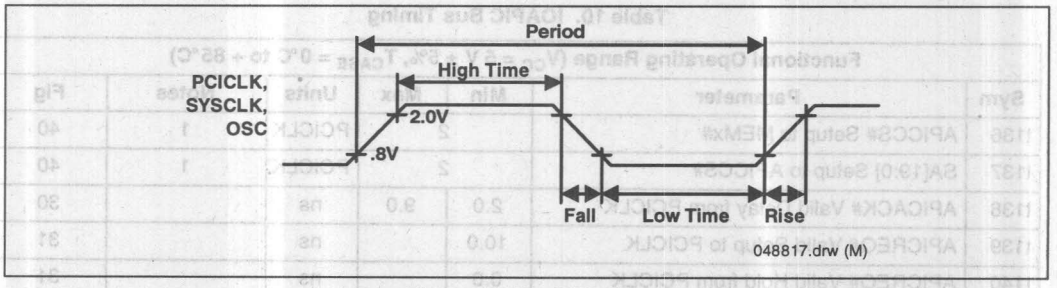


Figure 2. Clock Timing

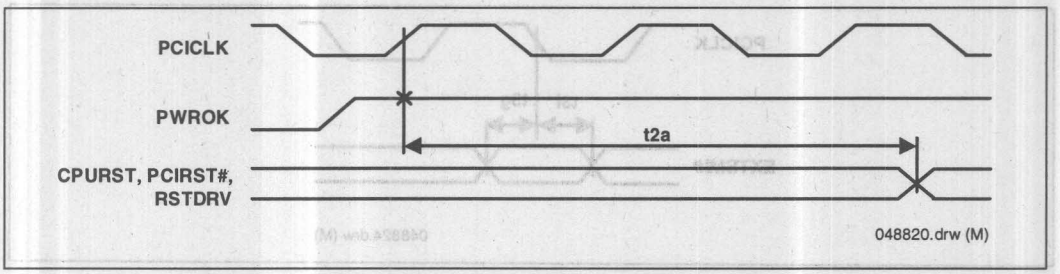


Figure 3. Reset Inactive After PWROK

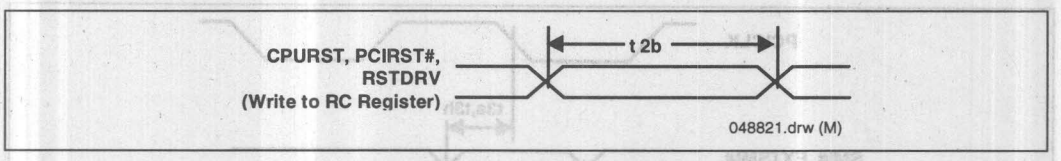


Figure 4. Reset Active Pulse Width

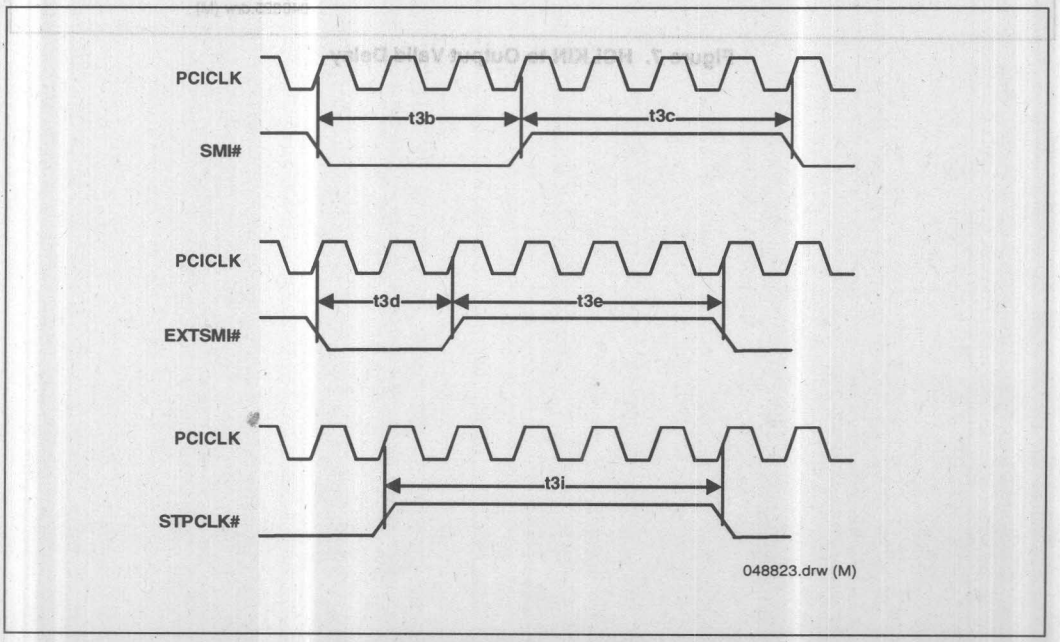


Figure 5. SMI#, EXTSMI#, and STPCLK# Timing

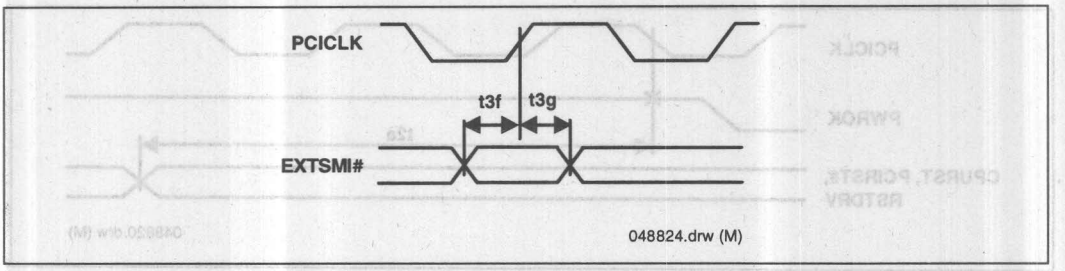


Figure 6. Input to PCICLK Setup/Hold Times

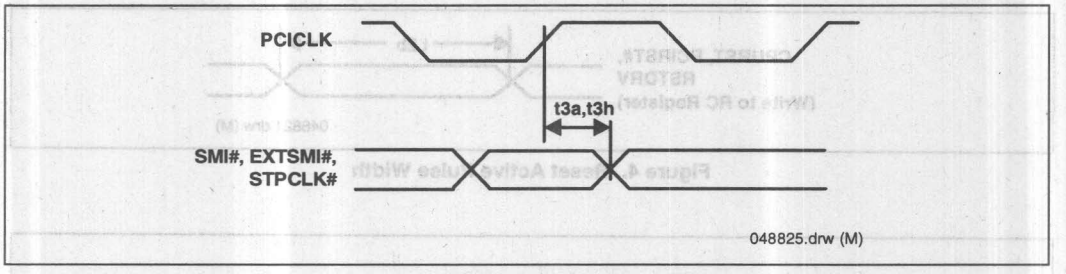


Figure 7. HCLKIN to Output Valid Delay

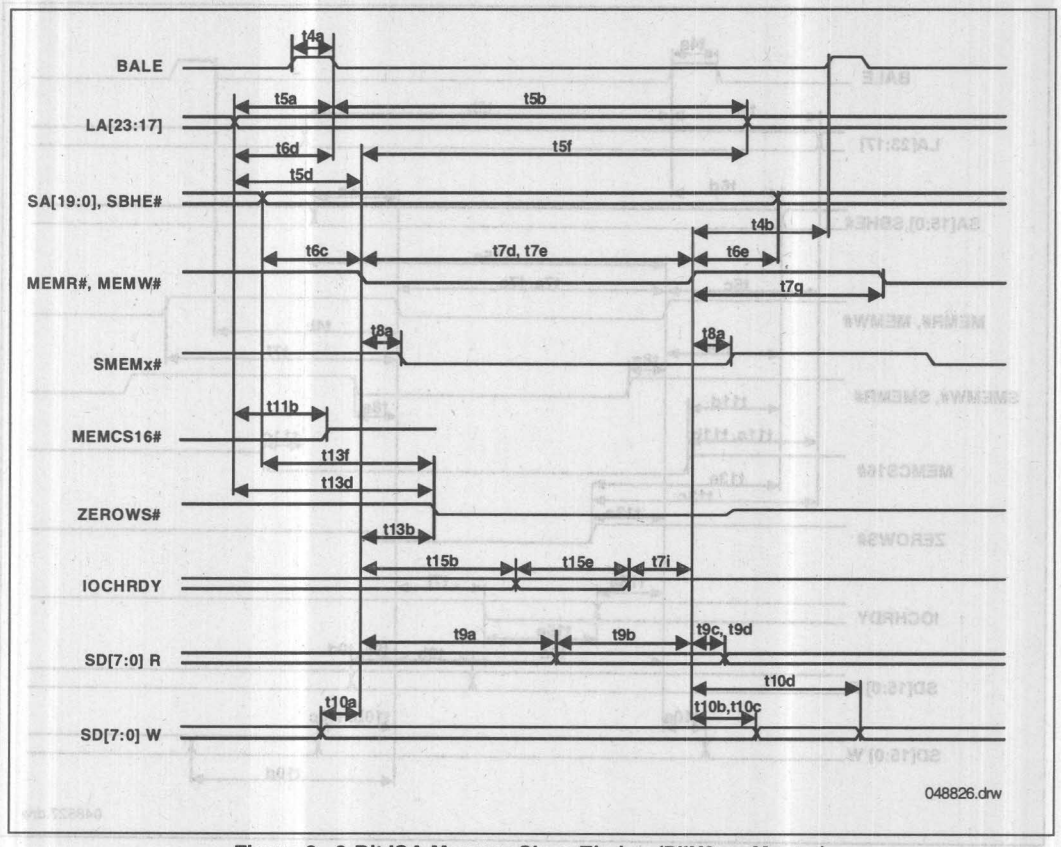


Figure 8. 8-Bit ISA Memory Slave Timing (PIIX3 as Master)

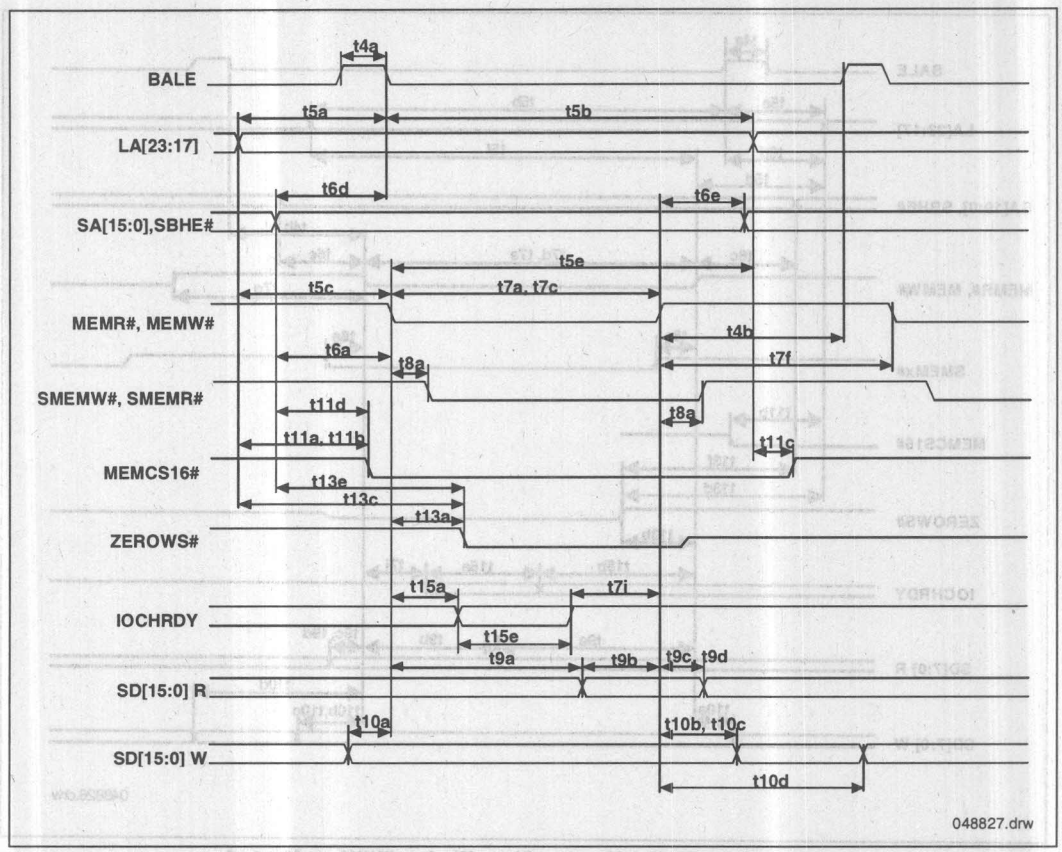


Figure 9. 16-Bit ISA Memory Slave Timing (PIIX3 as Master)

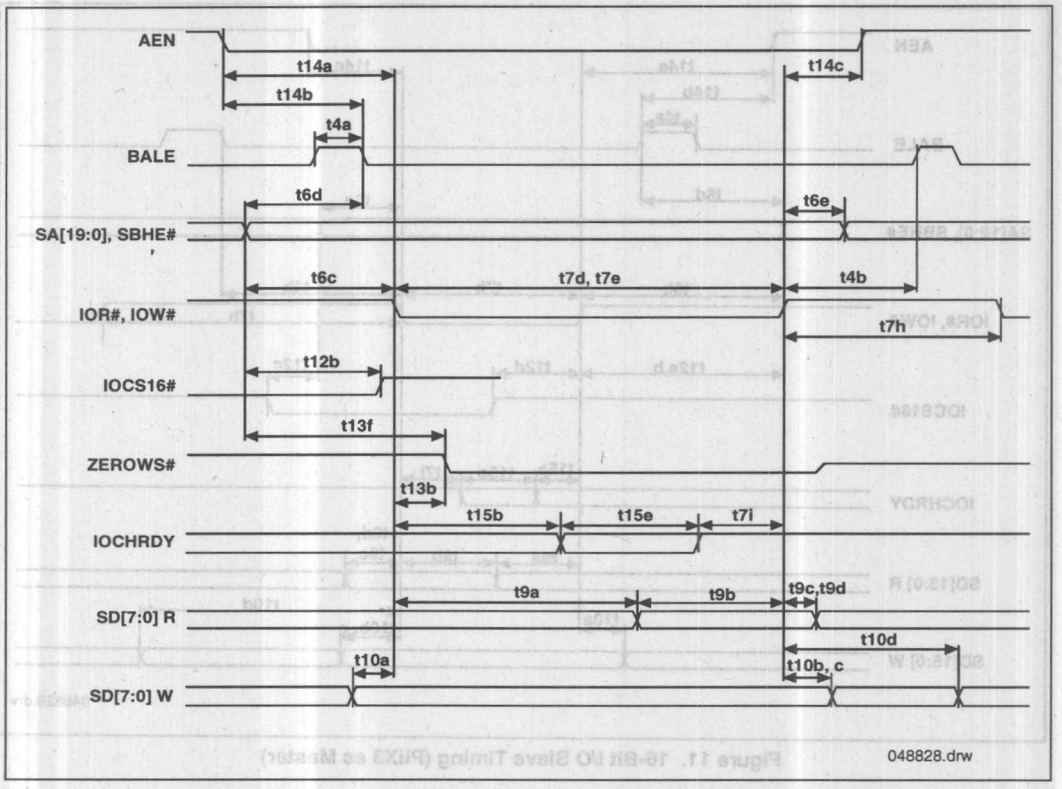


Figure 10. 8-Bit ISA I/O Slave Timing (PIIX3 as Master)

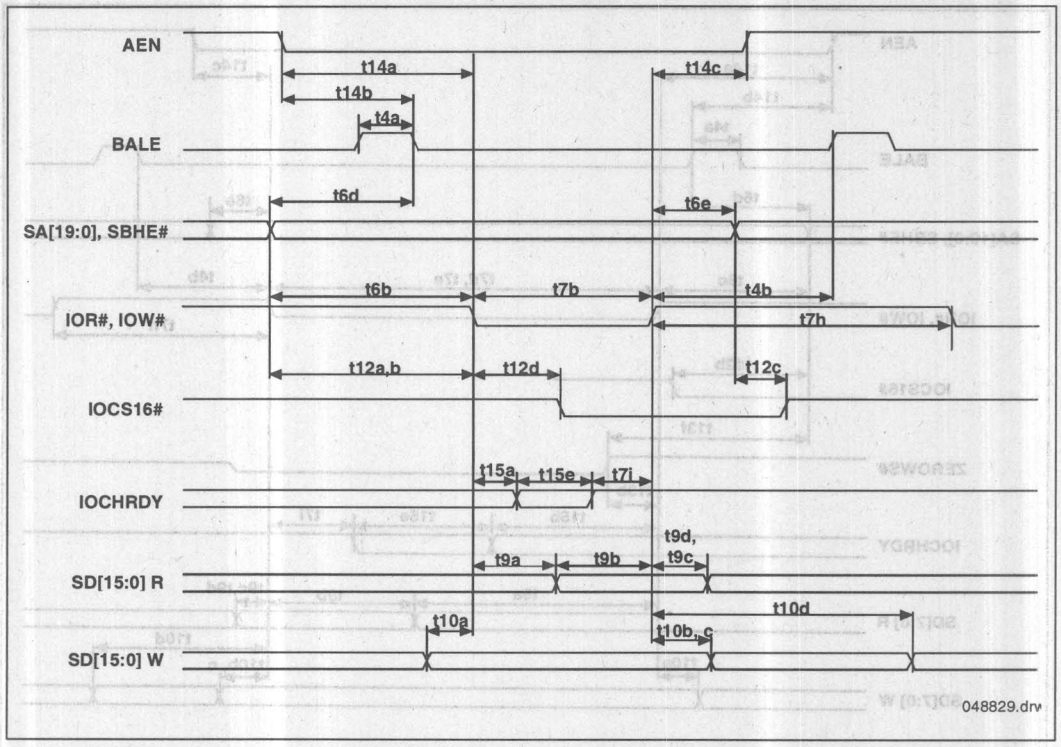


Figure 11. 16-Bit I/O Slave Timing (PIIX3 as Master)

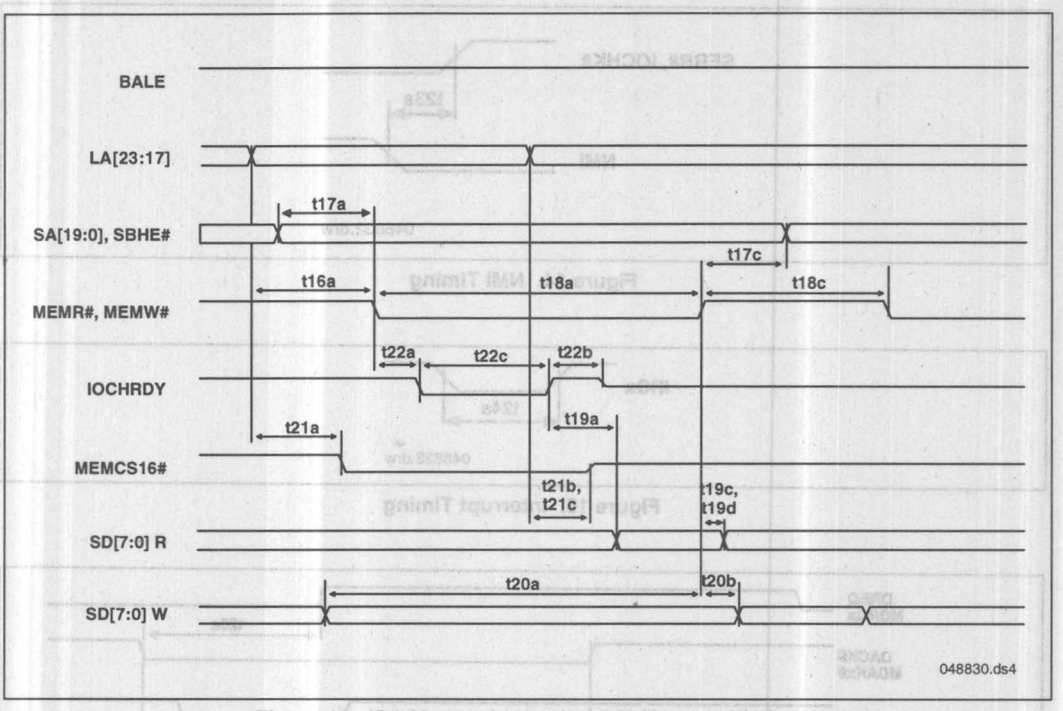


Figure 12. ISA Master Accessing PCI Memory Timing

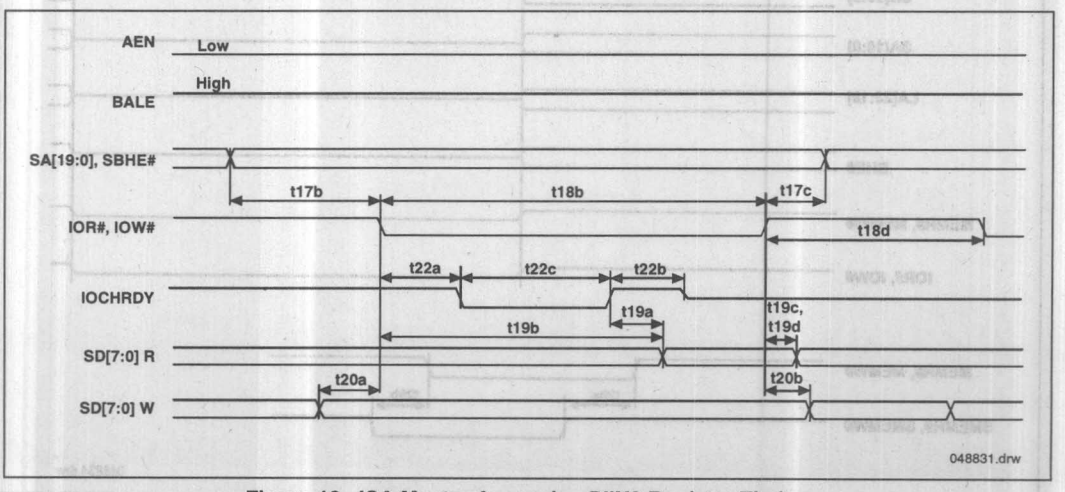


Figure 13. ISA Master Accessing PIIX3 Register Timing

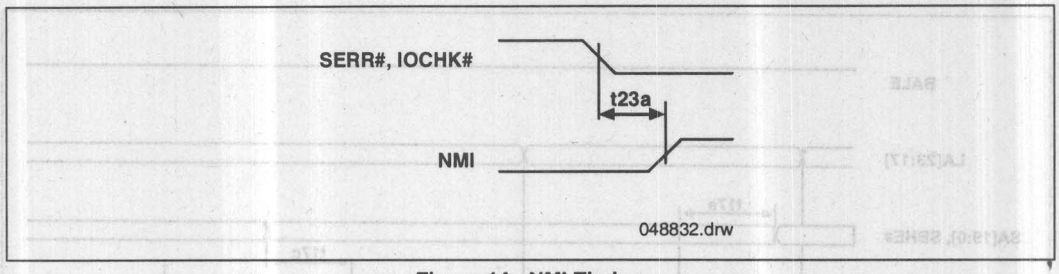


Figure 14. NMI Timing

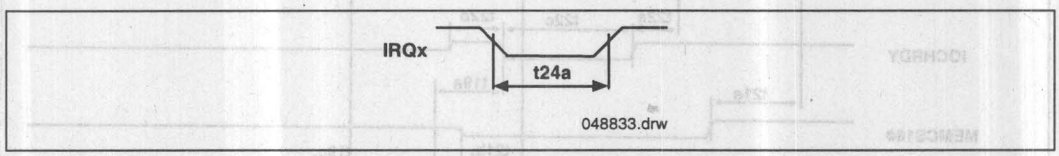


Figure 15. Interrupt Timing

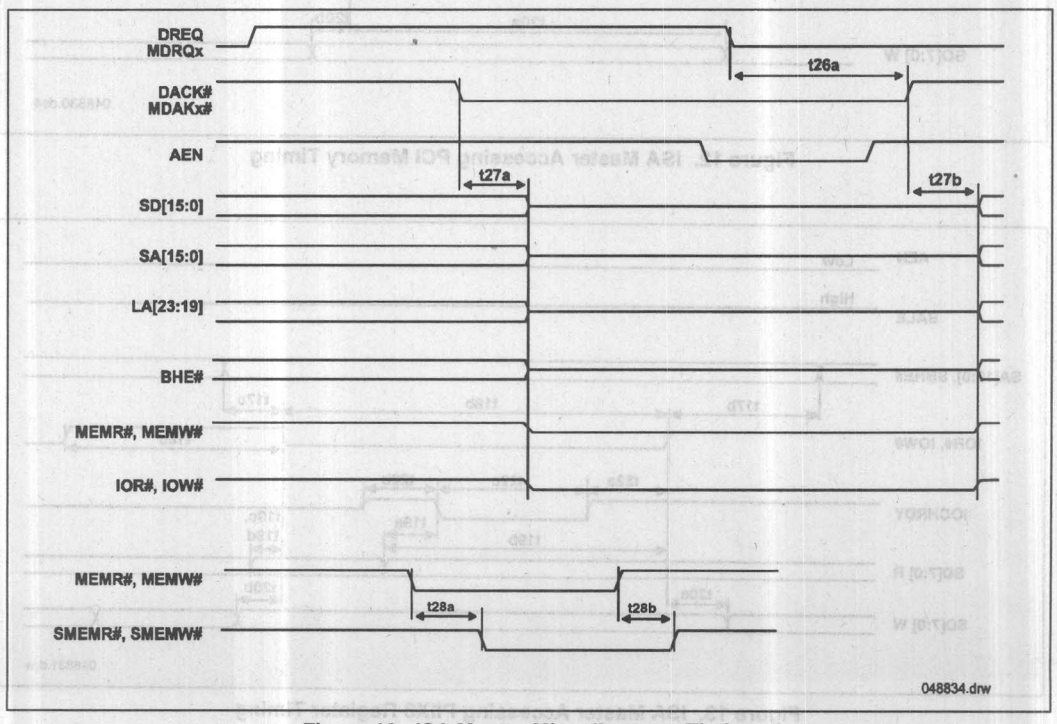


Figure 16. ISA Master Miscellaneous Timing

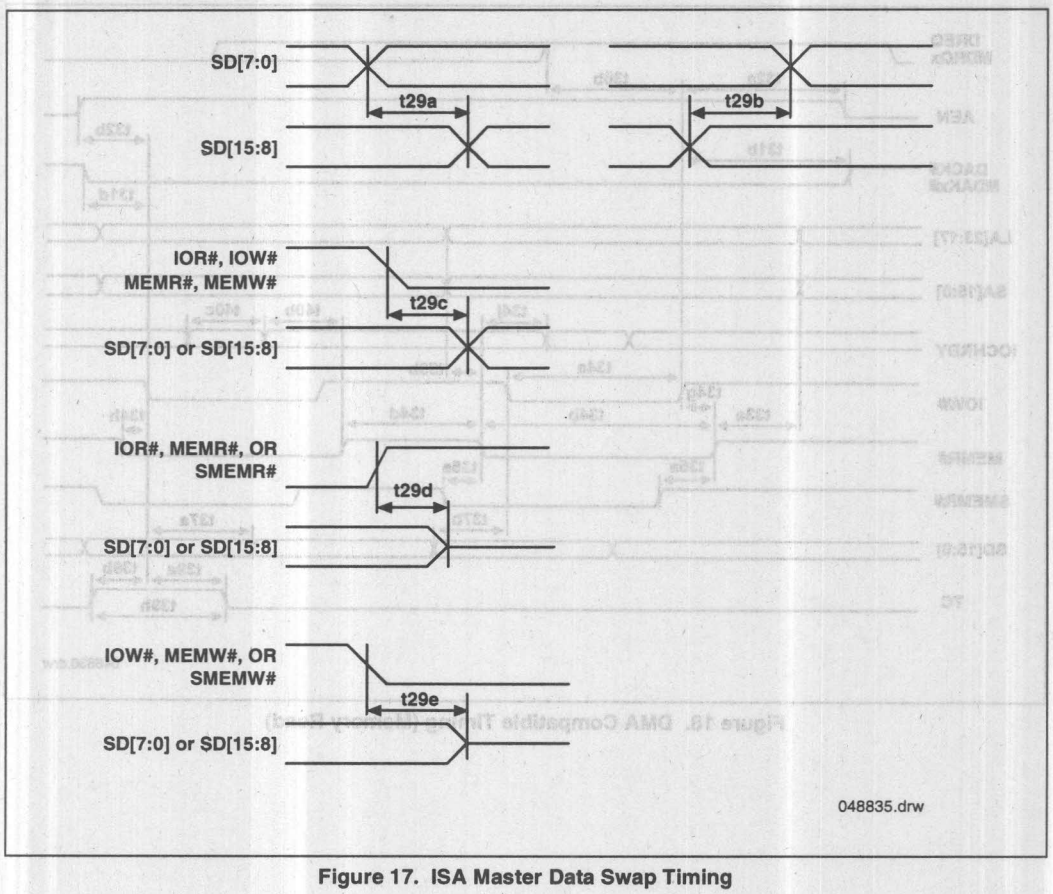


Figure 17. ISA Master Data Swap Timing

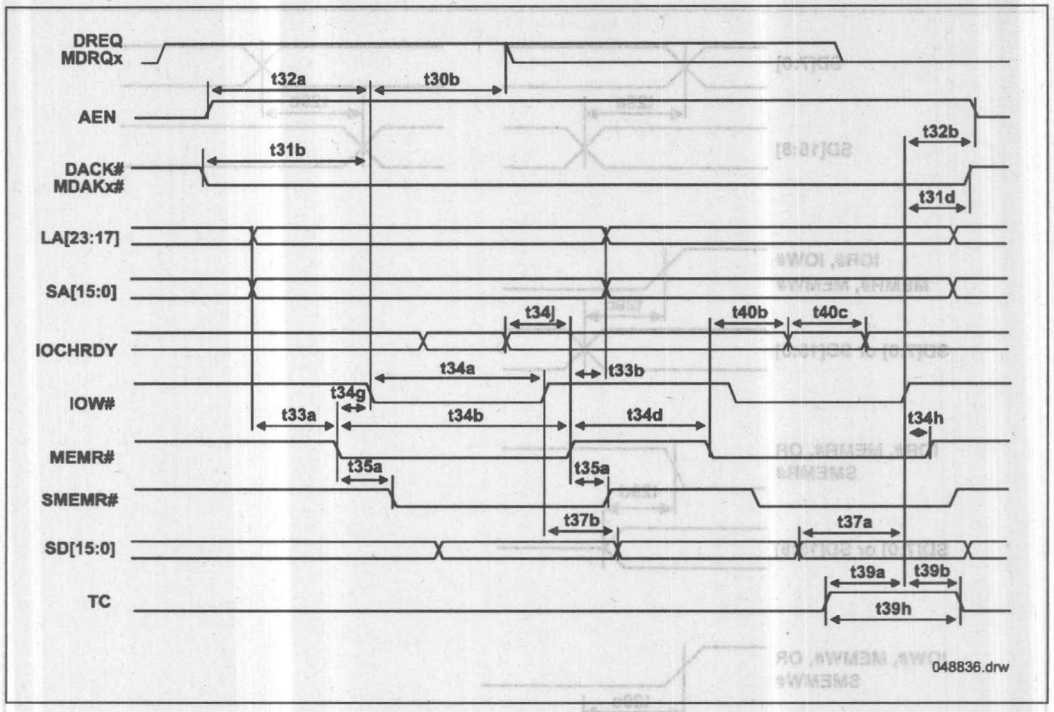


Figure 18. DMA Compatible Timing (Memory Read)

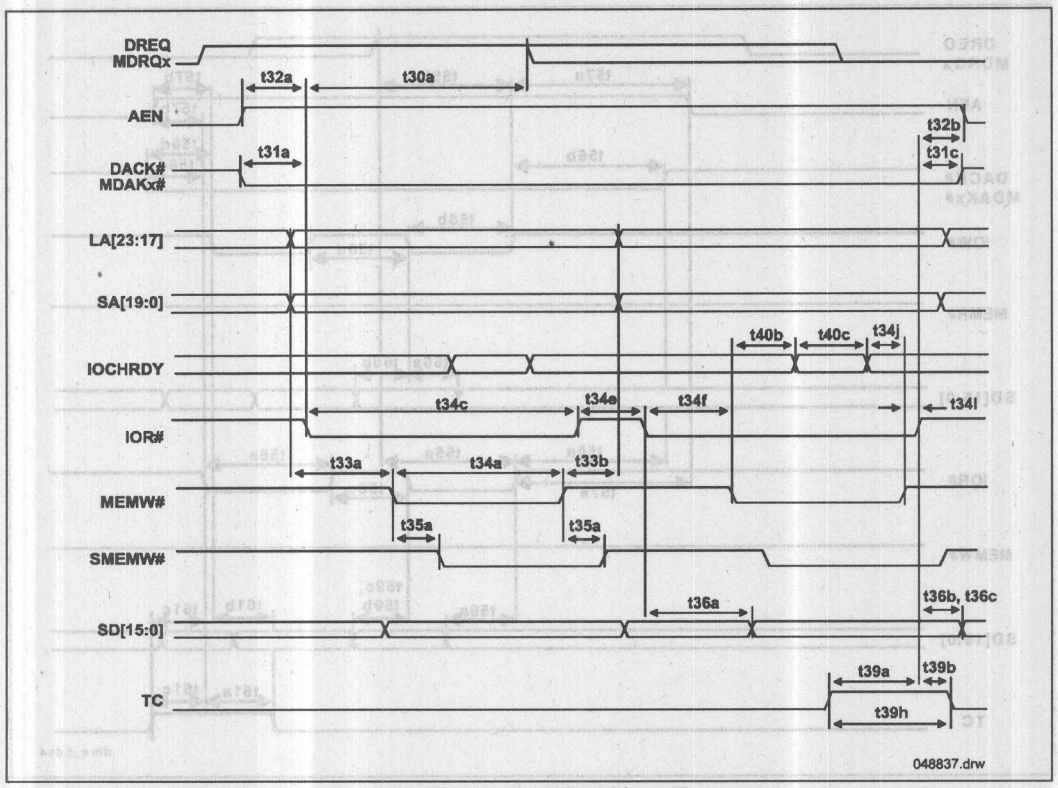


Figure 19. DMA Compatible Timing (Memory Write)

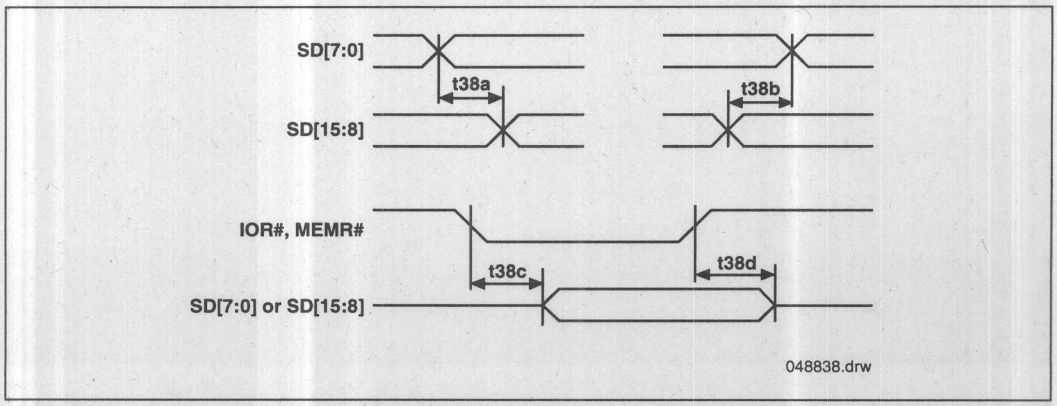


Figure 20. DMA Compatible Timing (Data Swap)

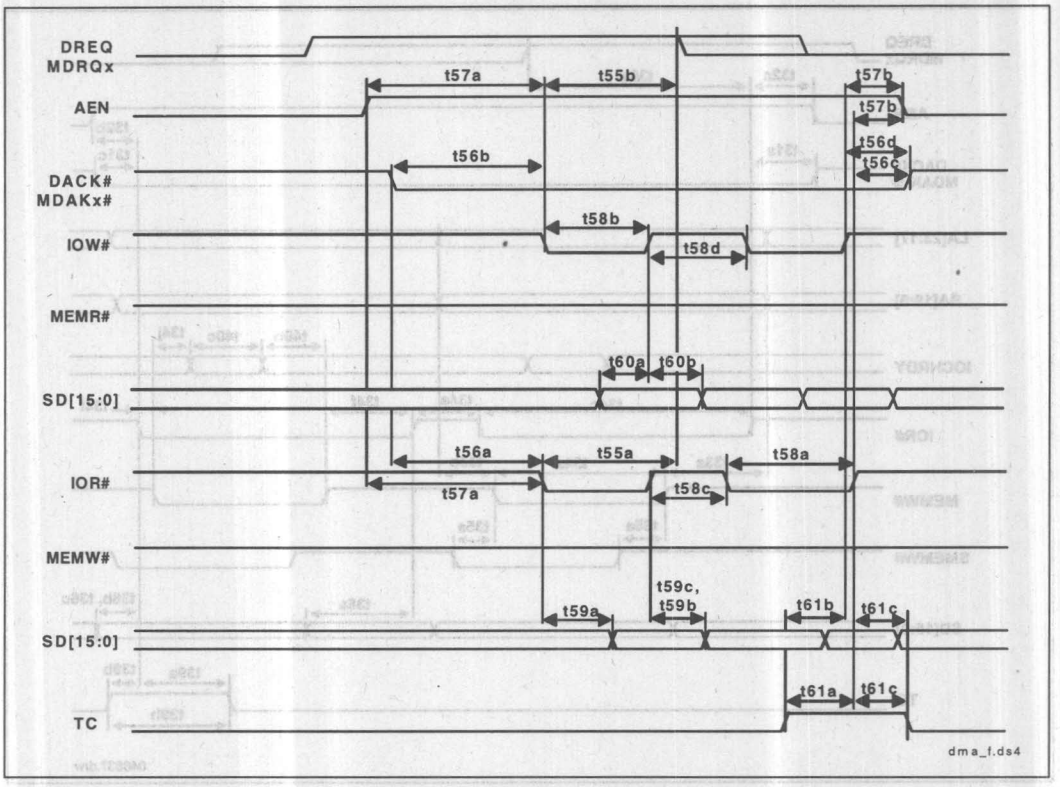


Figure 21. DMA Type F Timing

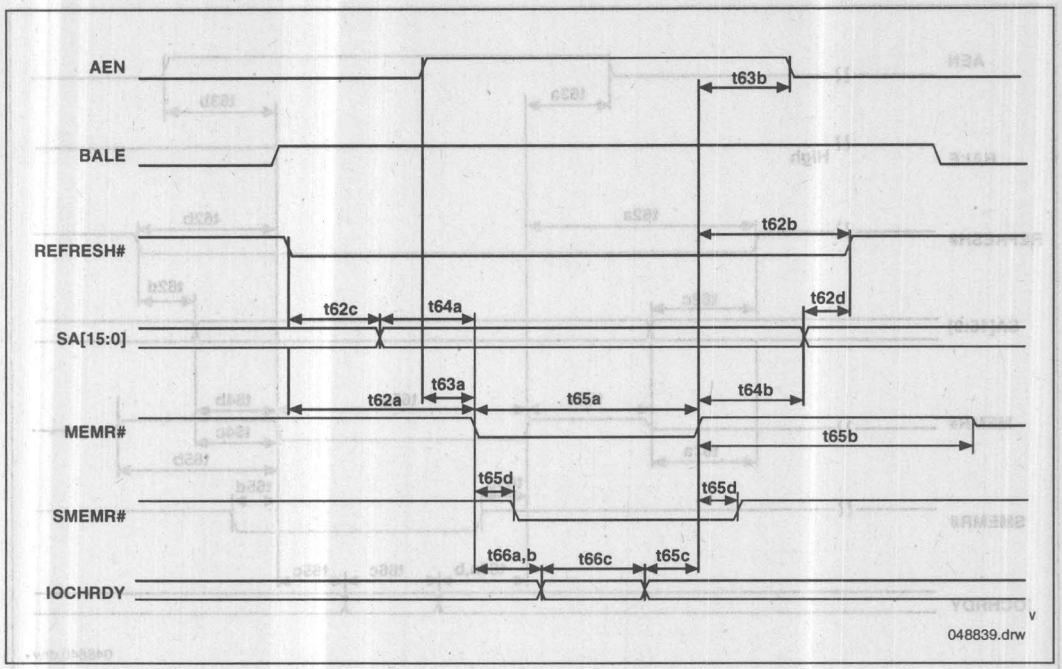


Figure 22. PIIX3-Initiated Refresh Timing

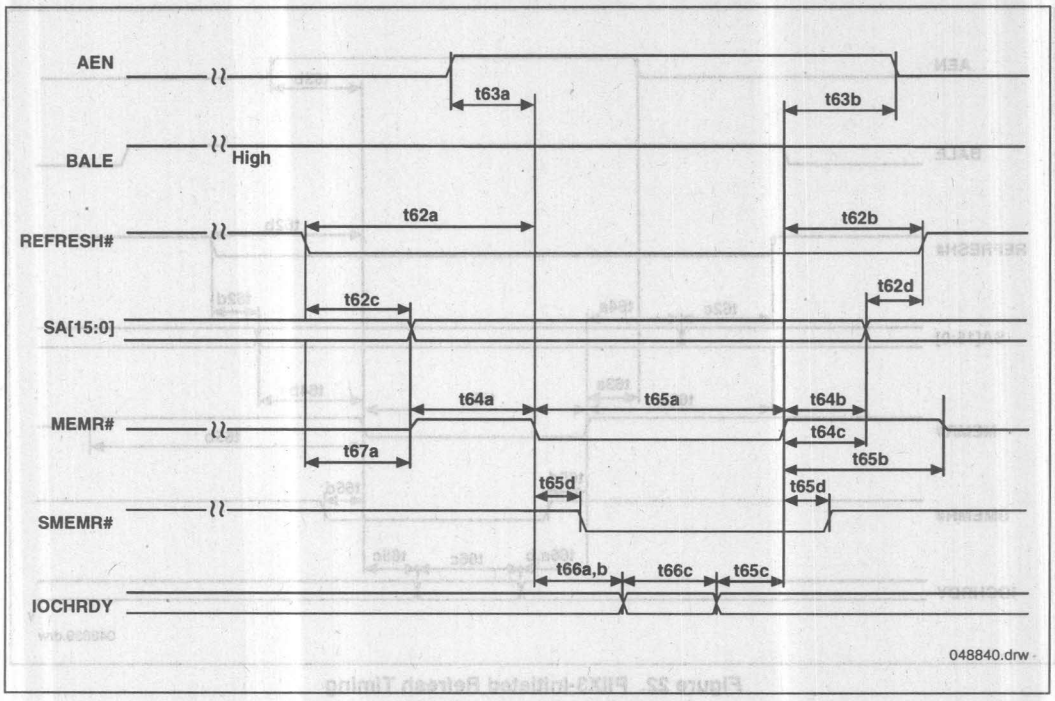


Figure 23. ISA Master-Initiated Refresh Timing

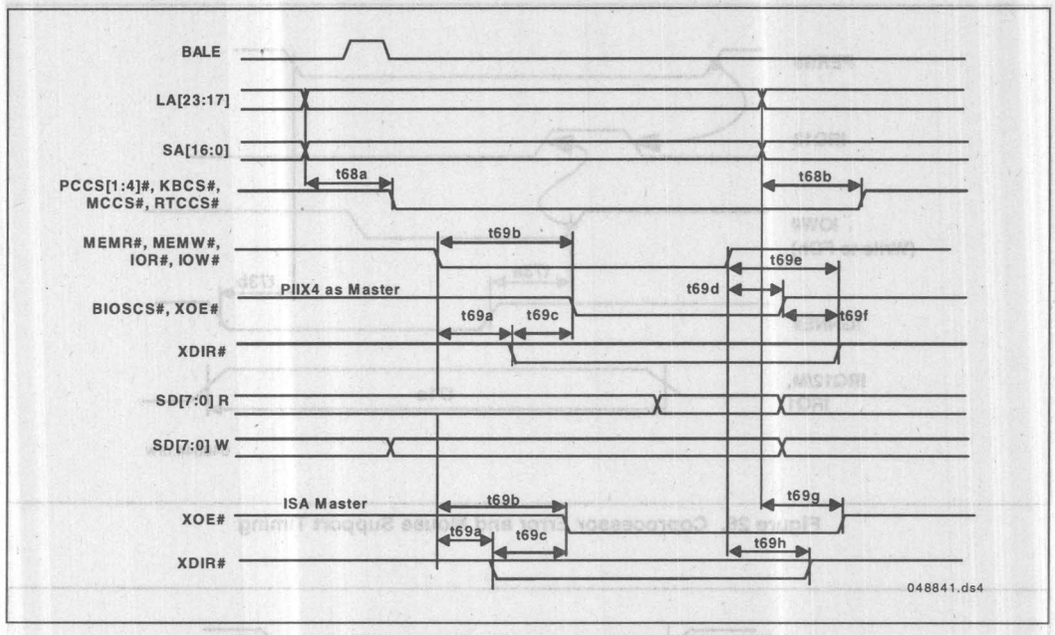


Figure 24. PIIX3 and ISA Master Access to X-Bus Timing

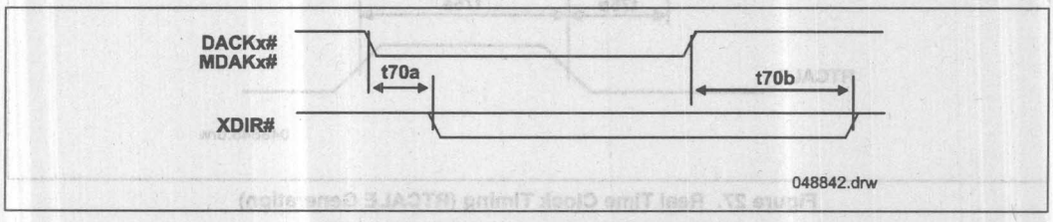


Figure 25. DMA Access to X-Bus Timing

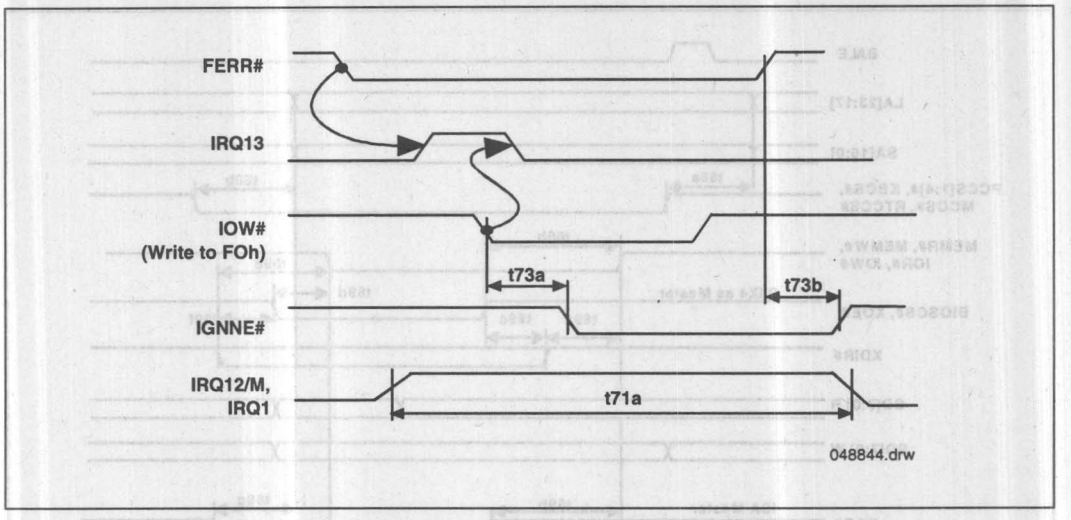


Figure 26. Coprocessor Error and Mouse Support Timing

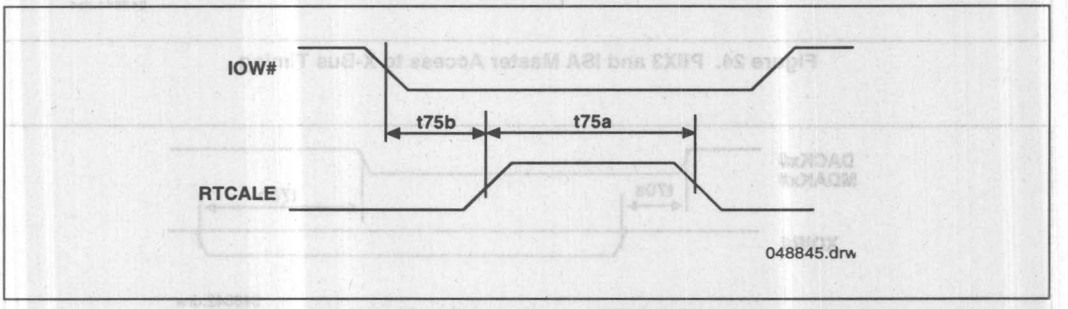


Figure 27. Real Time Clock Timing (RTCALE Generation)

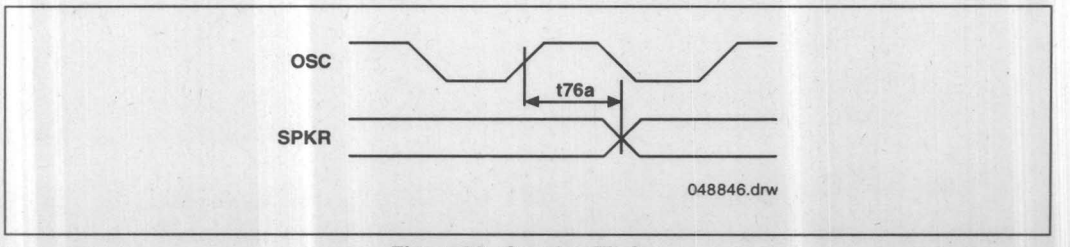


Figure 28. Speaker Timing

2.6 PCI Timing Diagrams

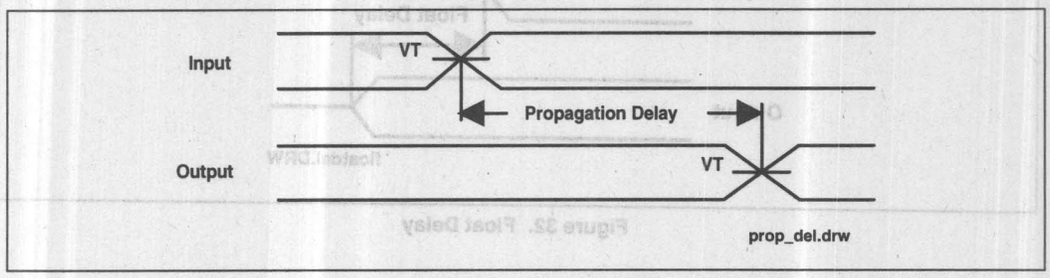


Figure 29. Propagation Delay

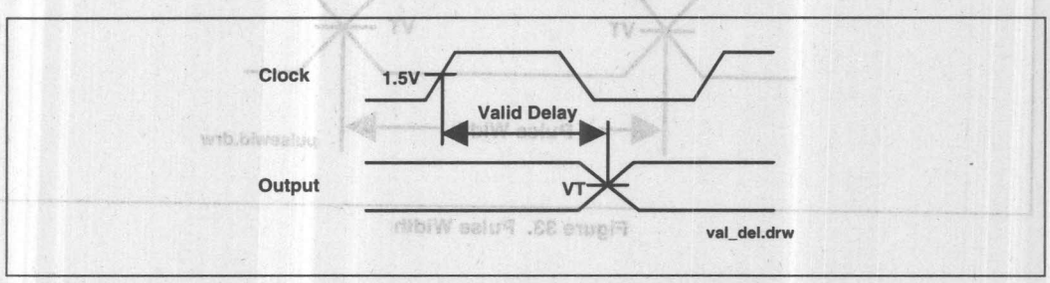


Figure 30. Valid Delay From Rising Clock Edge

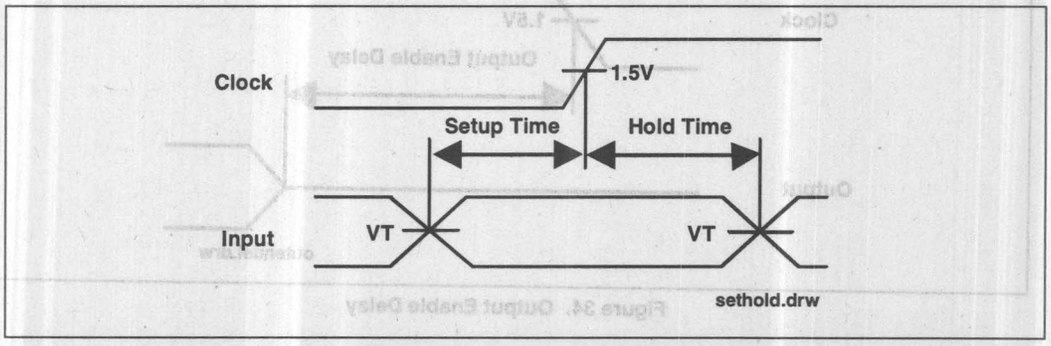


Figure 31. Setup and Hold Times

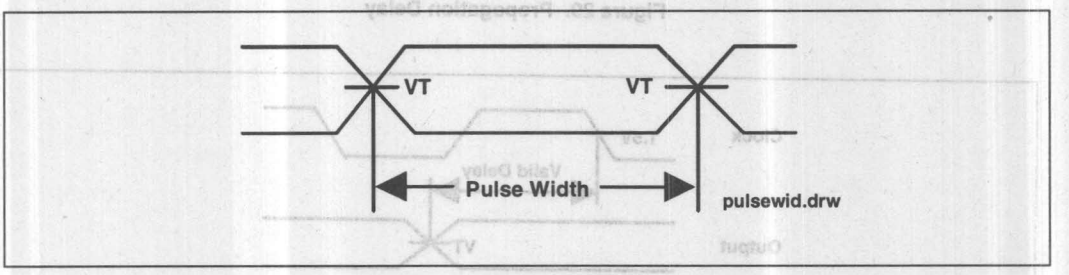


Figure 33. Pulse Width

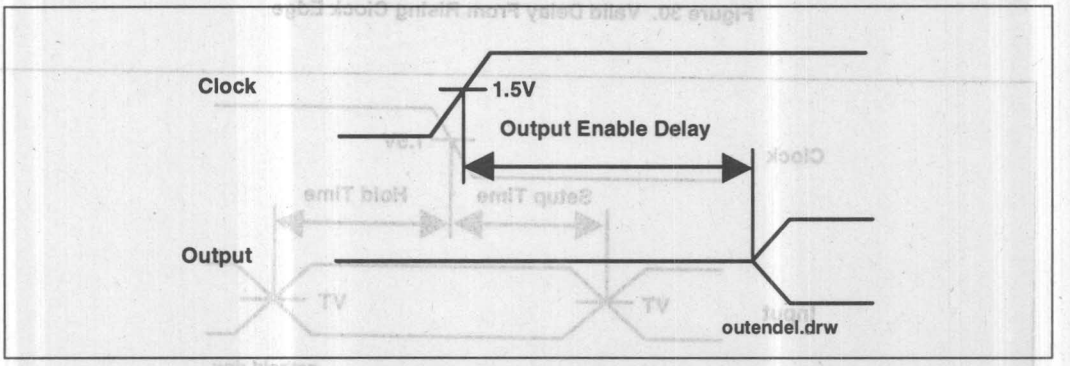


Figure 34. Output Enable Delay

2.7 IDE Timing Diagrams

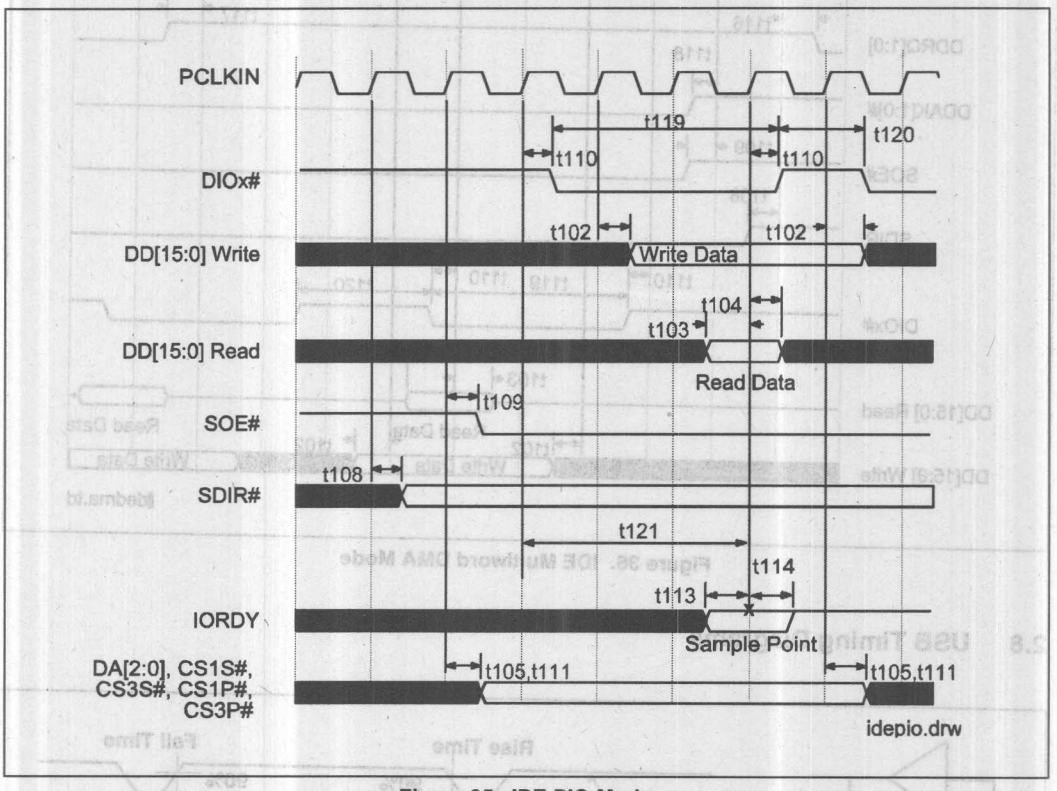


Figure 35. IDE PIO Mode

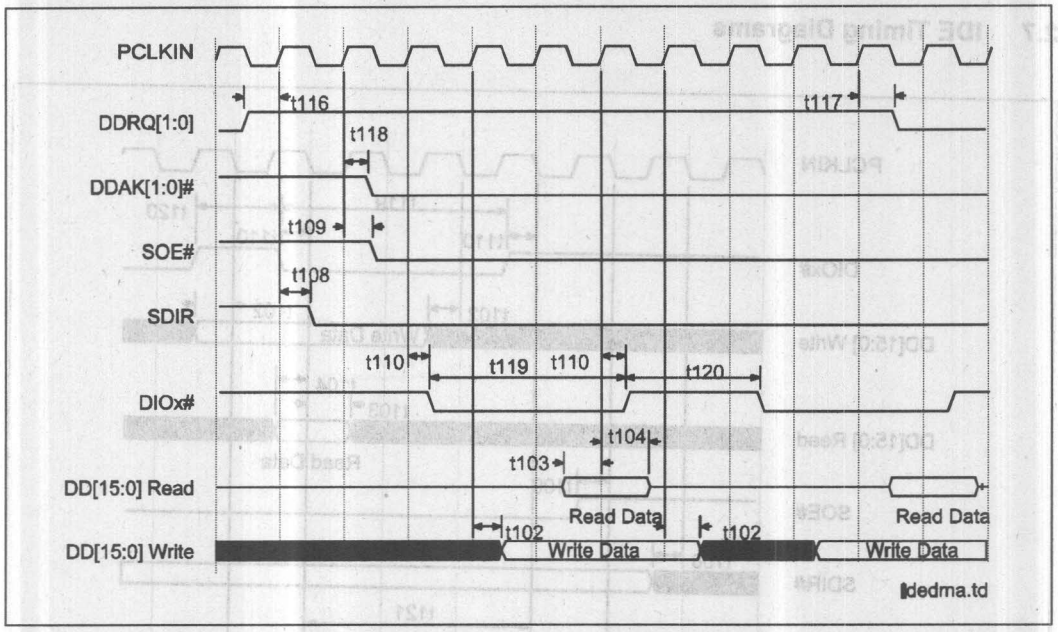


Figure 36. IDE Multiword DMA Mode

2.8 USB Timing Diagrams

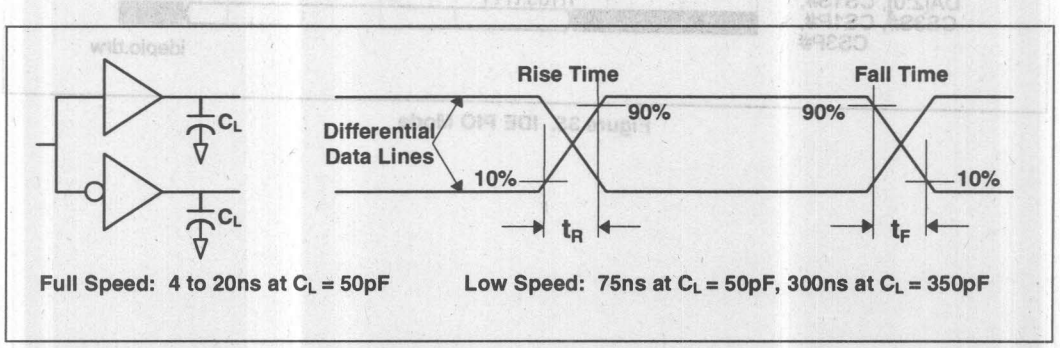


Figure 37. Data Signal Rise and Fall Time

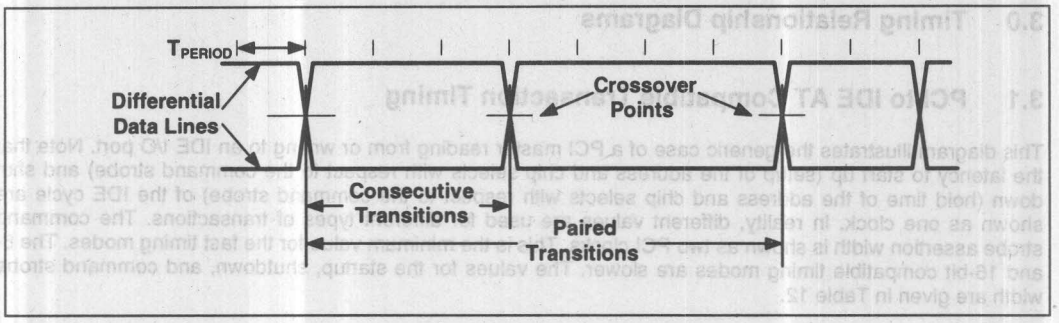


Figure 38. Data Jitter

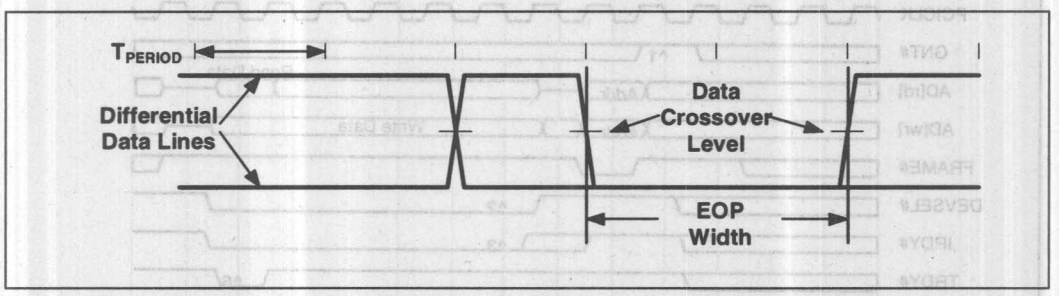


Figure 39. EOP Width Timing

2.9 IOAPIC Timing Diagrams

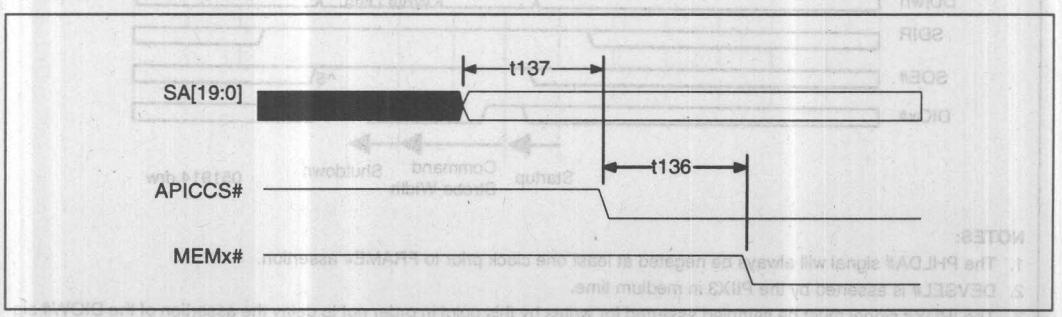
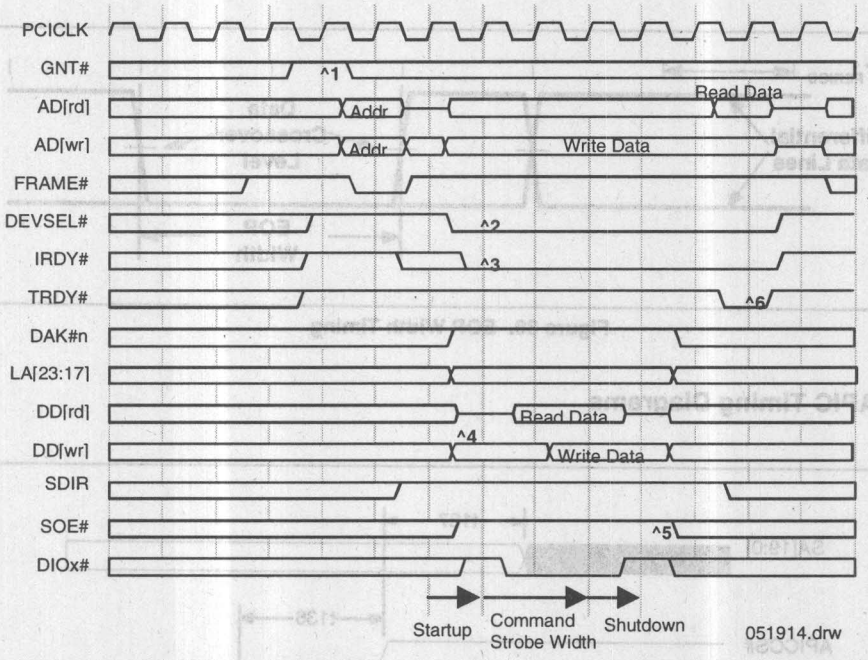


Figure 40. PIIX3 to IOAPIC Timing

3.0 Timing Relationship Diagrams

3.1 PCI to IDE AT Compatible Transaction Timing

This diagram illustrates the generic case of a PCI master reading from or writing to an IDE I/O port. Note that the latency to start up (setup of the address and chip selects with respect to the command strobe) and shut down (hold time of the address and chip selects with respect to the command strobe) of the IDE cycle are shown as one clock. In reality, different values are used for different types of transactions. The command strobe assertion width is shown as two PCI clocks. This is the minimum value for the fast timing modes. The 8- and 16-bit compatible timing modes are slower. The values for the startup, shutdown, and command strobe width are given in Table 12.



NOTES:

1. The PHLDA# signal will always be negated at least one clock prior to FRAME# assertion.
2. DEVSEL# is asserted by the PIIX3 in medium time.
3. The IRDY# signal must be sampled asserted for writes by this point in order not to delay the assertion of the DIOW# signal.
4. The DD[15:0] signals are three-stated on this clock in the case of reads from the IDE ports. Therefore, the earliest that the DIOR# signal (which enables data to be driven onto the DD[15:0] lines by the IDE slave device) can be driven is the following clock. (Therefore, the startup latency is at least one clock.)
5. The SOE# signal is reasserted when no more IDE transactions are pending.
6. TRDY# is asserted here with respect to the negation edge of the DIOR# and DIOW# signals.

Figure 41. PCI Master Access to IDE Device

Table 12. Command Strobe Width for IDE Transaction Type

IDE Transaction Type	Startup Latency	Shutdown Latency	ISP	RCT
Non-data port (8 bit)—25 MHz	4	1	9	17
Data port (16 bit)—25 MHz	3	1	5	11
Non-data port (8 bit)—30/33 MHz	4	1	11	22
Data port (16 bit)—30/33 MHz	3	1	6	14
Enhanced timing data port (MAX)	2	1	5	4
Enhanced timing data port (MIN)	2	1	2	1

NOTE: Startup and Shutdown latency will be incurred for all IDE PIO transactions except enhanced timing data port transactions. Further, the IDE chip selects are negated for at least two clocks after the Shutdown latency of the last transaction and before the Startup latency of the next.

intel®

AP-741

APPLICATION NOTE

Designing an Embedded System Using the Pentium® Processor with Voltage Reduction Technology (VRT) and the Intel 430HX PCIset

Intel Corporation
5000 W. Chandler Blvd.
Chandler, Arizona 85226

November 1996

Order Number: 272967-001

Designing an Embedded System Using the Pentium® Processor with Voltage Reduction Technology (VRT) and the Intel 430HX PCIset

Intel Corporation
5000 W. Chandler Blvd.
Chandler, Arizona 85226

November 1996

Order Number: 272907-001

1.0 Introduction

Designs that use the low power features of the Pentium® processors with Voltage Reduction Technology (VRT) can also take advantage of the high performance capabilities of the Intel 430HX PCIsets. This application note describes the differences between the Pentium processor with VRT and the 3.3 V Pentium processor and discusses some of the design considerations in using the Pentium processor with VRT with the Intel 430HX PCIset.

This application note should be used in conjunction with the Pentium processor documents listed in "Related Information" on page 7.

2.0 Voltage Reduction Technology (VRT)

The greatest challenge in developing systems based on new low power processor architectures is maintaining efficient thermal energy management. Since low power systems do not usually contain a cooling fan for internal components, heat is dissipated using innovative thermodynamic design techniques such as heat pipes and thermal sensors, and by using the mobile system chassis to vent heat externally. Proper thermal design is critical to ensuring the reliability of low power systems. Components that run too hot will be more likely to fail during normal use and may reduce the life of the system.

To help solve thermal issues, Intel developed Voltage Reduction Technology, which is integrated into new versions of the 75-, 90-, 100-, 120-, 133- and 150-MHz Pentium processors. The external pins of the Pentium processor with VRT remain powered at 3.3 Volts, which allows the processor to communicate with existing 3.3 Volt components in the system. The internal core of the processor operates at 2.9/3.1 Volts, resulting in up to a 40 percent power savings over its desktop counterpart. Consequently, the 150 MHz Pentium processor delivers over 60 percent faster performance than the 3.3 Volt 75 MHz version while retaining long battery life.

The Pentium processor with VRT is offered in the Tape Carrier Package (TCP) and the Staggered Pin Grid Array (SPGA) package. In this document, only the features of the SPGA package are discussed.

The architecture and internal features of the Pentium processor with VRT are identical to those of the desktop version of the Pentium processor, as described in the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors*, except some features which will be discussed later.

3.0 Intel 430HX PCIset

The Intel 430HX PCIset consists of the 82439HX System Controller (TXC) and the 82371SB PCI ISA IDE Xcelerator (PIIX3). The TXC is a single-chip host-to-PCI bridge and provides the second level cache control and DRAM control functions. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory is implemented with synchronous pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM is used for the cache line status bits. The TXC provides a 64/72-bit data path to main memory and memory sizes up to 512 Mbytes. The DRAM controller provides eight rows and optional DRAM error detection/correction or parity. The TXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, The TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC contains read prefetch and posted write buffers.

4.0 Differences Between the SPGA Pentium® Processor with Voltage Reduction Technology and the 3.3 V Pentium Processor

All specifications for the SPGA Pentium processor with VRT are identical to those of the 3.3 V Pentium processor, except for the differences described in this section.

4.1 Features Removed

The following features have been removed for the Pentium processor with VRT: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins on the 3.3 V Pentium processor that have been removed on the Pentium processor with VRT.

Table 1. Signals Removed from the Pentium® Processor with Voltage Reduction Technology

Signal	Type†	Function
ADSC#	O	Additional Address Status. This signal is mainly used for large or stand-alone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	I	Additional Burst Ready. This signal is mainly used for large or stand-alone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	I	CPU Type. This signal is used for dual processing systems.
D/P#	O	Dual/Primary processor identification. This signal is used only for an upgrade processor.
FRCMC#	I	Functional Redundancy Checking. This signal is used only for error detection via processor redundancy, and requires two Pentium® processors (master/checker).
PBGNT#	I/O	Private Bus Grant. This signal is used only for dual processing systems.
PBREQ#	I/O	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	I/O	Private Hit. This signal is used only for dual processing systems.
PHITM#	I/O	Private Modified Hit. This signal is used only for dual processing systems.
PICCLK	I	APIC Clock. This signal is the APIC interrupt controller serial data bus clock.
PICD0 [DPEN#]	I/O	APIC's Programmable Interrupt Controller Data line 0. PICD0 shares a pin with DPEN# (Dual Processing Enable).
PICD1 [APICEN]	I/O	APIC's Programmable Interrupt Controller Data line 1. PICD1 shares a pin with APICEN (APIC Enable upon RESET).

†The pins are classified as Input or Output based on their function in Master Mode.

4.2 Maximum Rating

The following values are stress ratings only. Functional operation at the maximum rating is neither implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the SPGA Pentium processor with VRT contains protective circuitry to resist damage from static electric discharge, precautions should be taken to avoid high static voltages or electric fields.

WARNING:

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 2. SPGA Absolute Maximum Ratings

Parameter	Value	Notes
Case temperature under bias	-65°C to 110°C	
Storage Temperature	-65°C to 150°C	
3.3 V Supply voltage with respect to V_{SS}	-0.5 V to +4.6 V	
3.1 V Supply voltage with respect to V_{SS}	-0.5 V to +4.1 V	
3.3 V Only Buffer DC Input Voltage	-0.5 V to V_{CC3} + 0.5 V	Not to exceed 4.6 V (1)
5 V Safe Buffer DC Input Voltage	-0.5 V to +6.5 V	(2)(3)

NOTES:

1. Applies to all SPGA Pentium processor with VRT inputs except CLK.
2. Applies to CLK.
3. See Table 4.

4.3 DC Specifications

Tables 3, 4, and 5 list the DC specifications that apply to the SPGA Pentium processor with VRT. The SPGA Pentium processor with VRT core operates at 3.1 V internally while the I/O interface operates at 3.3 V. The CLK input may be at 3.3 V or 5 V. Since the 3.3 V (5 V safe) input levels defined in Table 4 are the same as 5 V TTL levels, the CLK input is compatible with existing 5 V clock drivers. The power dissipation specification in Table 6 is provided for the design of thermal solutions during operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

Table 3. SPGA 3.3 V DC Specifications
T_{CASE} = 0 to 85°C; V_{CC2} = 3.1 V ± 165 mV; V_{CC3} = 3.3 V ± 165 mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	-0.3	0.8	V	TTL Level (1)
V_{IH3}	Input High Voltage	2.0	V_{CC3} + 0.3	V	TTL Level (1)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1)(2)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (1)(3)
I_{CC2}	Power Supply Current from 3.1 V core supply		2500 2775	mA mA	@120 MHz (4) @133 MHz (4)
I_{CC3}	Power Supply Current from 3.3 V I/O buffer supply		320 355	mA mA	@120 MHz (4) @133 MHz (4)

NOTES:

1. 3.3 V TTL level apply to all signals except CLK.
2. Parameter measured at 4 mA.
3. Parameter measured at 3 mA.
4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and V_{CC2} = 3.1 V ± 165 mV and V_{CC3} = 3.3 V ±165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes.

Table 4. 3.3 V (5 V safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	-0.3	0.8	V	TTL Level (1)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTE:

1. Applies to CLK only.

Table 5. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(1)
C_O	Output Capacitance		20	pF	(1)
$C_{I/O}$	I/O Capacitance		25	pF	(1)
C_{CLK}	CLK Input Capacitance		15	pF	(1)
C_{TIN}	Test Input Capacitance		15	pF	(1)
C_{TOUT}	Test Output Capacitance		20	pF	(1)
C_{TCK}	Test Clock Capacitance		15	pF	(1)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (2)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (2)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4 V (3)
I_{IL}	Input Leakage Current		400	µA	V_{IN} = 0.4 V (4)

NOTES:

1. Guaranteed by design.
2. This parameter is for input without pull up or pull down.
3. This parameter is for input with pull down.
4. This parameter is for input with pull up.

Table 6. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical(1)	Max(2)	Unit	Notes
Thermal Design Power (Typ)	2.5 - 3.5	7.1	Watts	@120 MHz
	3.0 - 4.0	7.9	Watts	@133 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		1.2	Watts	@120 MHz (3)
		1.3	Watts	@133 MHz (3)
Stop Clock Power Dissipation	0.02	0.05	Watts	(4)

NOTES:

1. This is typical power dissipation in a system. This value is the average value measured in a system using a typical device at V_{CC2} = 3.1 V and V_{CC3} = 3.3 V running typical applications. This value is highly dependent upon a specific system configuration.
2. Systems must be designed to thermally dissipate the maximum thermal design power (typ). It is determined using a worst case instruction mix with V_{CC2} = 3.1 V and V_{CC3} = 3.3 V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

4.4 AC Specifications

The AC specifications of the SPGA Pentium processor with VRT consist of setup times, hold times, and valid delays at 0 pF. All SPGA Pentium processor with VRT AC specifications are valid for V_{CC2} = 3.1 V ±165 mV, and T_{CASE} = 0 to 85°C.

For the AC timing changes for the Pentium processor with VRT (60 MHz and 66 MHz bus operations) refer to the *Pentium® Processor with Voltage Reduction Technology Datasheet*.

4.5 Thermal Specifications

The SPGA Pentium processor with VRT is specified for proper operation when the case temperature T_{CASE} (T_C) is within the specified range of 0°C to 85°C.

4.6 SPGA Package Differences

The SPGA Pentium processor with VRT has a pin array that is mechanically identical to the SPGA version of the 3.3 V Pentium, but some pins are connected differently. Also, there are small differences in the package dimensions. Refer to the *Pentium® Processor with Voltage Reduction Technology Datasheet* for these differences.

4.7 I/O Buffer Models

The I/O buffer models of the Pentium processor with VRT (both TCP and SPGA) differ from that of the 3.3 V Pentium processor. Refer to the *Pentium® Processor with Voltage Reduction Technology Datasheet*. Also, the capacitance (Cp) and inductance (Lp) parameter values differ between the two packages (TCP and SPGA) for the Pentium processor with VRT. For SPGA Pentium processors with VRT values, refer to the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors*.

5.0 Design Considerations

Designing a system that uses the Pentium processor with VRT and the Intel 430HX PCIset is similar to designing a single-processor, 3.3 V Pentium processor-based system, but without using the Advanced Programmable Interrupt Controller (APIC). The considerations for designing with the Pentium processor with VRT and the Intel 430HX PCIset are described below.

5.1 Power and Ground

For clean on-chip power distribution, the SPGA Pentium processor with VRT has 25 V_{CC2} (3.1 V power), 28 V_{CC3} (3.3 V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be must made to all external V_{CC2}, V_{CC3} and V_{SS} pins of the SPGA Pentium processor with VRT. On the circuit board all V_{CC2} pins must be connected to a 3.1 V V_{CC2} plane (or island) and all V_{CC3} pins must be connected to a 3.3 V V_{CC3} plane. All V_{SS} pins must be connected to a V_{SS} plane.

5.2 Power Sequencing

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, for compatibility with future processors, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both on or both off within one second of each other.

5.3 Decoupling Recommendations

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor. Low inductance capacitors and interconnects are recommended for best high frequency and electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the 3.3 V plane and the 3.1 V plane (or island). Capacitor values should be chosen to ensure that they eliminate both low and high frequency noise components. Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction,

causing the processor to enter the Auto HALT Powerdown state. Such occurrences may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 µF to 100 µF range are required to maintain a regulated supply voltage during the interval between when the current load changes and when the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel. These capacitors should be placed near the processor (on the 3.3 V plane and the 3.1 V plane or island) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems Application Note*.

5.4 Connection Specifications

All NC (No Connect) pins must remain unconnected and all RESERVED pins must remain unconnected. For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3} and unused active high inputs should be connected to ground.

6.0 Related Information

Intel offers a variety of information through the World Wide Web at http://www.intel.com.

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APPLICATION NOTE

The Advantages of Using the 82371SB PCI ISA IDE Xcelerator (PIIX3) with the Intel 430HX PCIset in Embedded Designs

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5000 W. Chandler Blvd.
Chandler, Arizona 85226

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1.0 Introduction

This application note explains the advantages of using the 82371SB PCI ISA IDE Xcelerator (PIIX3) in embedded designs that use the Intel 430HX PCIset. It highlights some of the important functions and features of the PIIX3 and addresses some of the design considerations when eliminating the PIIX3 from an embedded design.

2.0 Intel 430HX PCIset Overview

The Intel 430HX PCIset consists of the 82439HX System Controller (TXC) and the 82371SB PCI ISA IDE Xcelerator (PIIX3). The TXC is a single-chip host-to-PCI bridge and provides the second-level cache control and DRAM control functions. The second-level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. The cache controller also supports cacheless designs. The cache memory is implemented with synchronous pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM is used for the cache line status bits.

The TXC provides a 64/72-bit data path to main memory and memory sizes up to 512 Mbytes. The DRAM controller provides eight rows and optional DRAM error detection/correction or parity.

The TXC's optimized PCI interface allows the processor to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC contains read prefetch and posted write buffers.

The PIIX3 is a multi-function PCI device that implements a PCI-to-ISA bridge function and a PCI IDE function. The PIIX3 also implements a Universal Serial Bus host/hub function.

3.0 PIIX3 Features

As a PCI-to-ISA bridge, the PIIX3 integrates many common I/O functions found in ISA-based PC systems. These include a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer counter, and power management support.

In addition to compatible transfers, each DMA channel supports type F transfers. Edge/Level interrupts and interrupt steering are supported for PCI plug-and-play compatibility. The PIIX3 can be programmed to allow the PCI active low interrupts (PIRQ[D:A]#) to be internally routed to one of 11 interrupts (IRQ[15,14,12:9,7:3]). In addition, the motherboard interrupt (MIRQ0) can be routed to any of the 11 interrupts.

The PIIX3 supports two IDE connectors for up to four IDE devices, providing an interface for IDE hard disks and CD ROMs.

The PIIX3 contains a Universal Serial Bus (USB) host controller that is UHCI compatible. The host controller's root hub has two programmable UBS ports. The PIIX3 can support a stand-alone I/O APIC device on the ISA X-Bus. It provides the chip select signal (APICCS#) for the I/O APIC and the handshake signals to maintain buffer coherency in the I/O APIC environment.

The PIIX3 contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one PIIX3 timer unit, referred to as *Timer-1*. Each counter output provides a key system timer interrupt for a time-of-day, diskette time-out, or other system timing function. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker.

The PIIX3 has extensive power management capability, permitting a system to operate in a low power state without being powered down. The PIIX3 can put the processor in a low power state by asserting the STPCLK# signal, which is an interrupt to the processor. Once the STPCLK# interrupt is executed, the processor enters the stop grant state. In this state, the processor's internal clocks are disabled and instruction execution is stopped.

the TXC. Therefore, the PIIX3, and related technical support, will be available as long as the 430HX PCIset is available.

4.0 Designing without the PIIX3

If the PIIX3 is not implemented with the 430HX PCIset, several features that are typically supported by the PIIX3 and that are required in certain embedded designs must be provided by other means. This section discusses some design considerations with two alternatives: using the Super I/O* Controller and using another PCI-to-ISA bridge.

4.1 Using a Super I/O Controller

Using a Super I/O Controller is not new to the design world, but using the Super I/O Controller in a design that does not have an ISA bus interface is new. Using a Super I/O Controller in this type of design raises many issues:

- The Super I/O Controller must be interfaced with the PCI bus. This type of Super I/O Controller is not common in the market. A standard ISA Super I/O Controller can be used but requires additional logic to interface to the PCI bus.
- Most of the Super I/O Controllers do not have the interrupt, DMA, and IDE controllers and/or a timer counter. Separate devices may have to be added to the design.
- A PCI-to-Flash controller must be provided to access boot ROM code.
- A special software interface must be implemented for utilizing the processor's power management capabilities and handling the processor interface signals, such as different types of resets, NMI, and SMI# signals.

menting this type of design include:

- The PCI-to-ISA bridge timing specifications must be compatible with those of the PIIX3 to enable interfacing with the TXC.
- The availability of the new bridge may not be guaranteed for long-term embedded support.
- Intel cannot be responsible for the technical support of these types of designs.

5.0 Conclusion

Using the PIIX3 in embedded designs that use the 430HX PCIset makes the embedded design much easier to implement. Designing with the PIIX3 reduces the cost and embedded total number of components in the design. The PIIX3 will be available in the embedded market as long as the 430HX PCIset is available. Intel recommends and supports using the complete 430HX PCIset.

6.0 Related Information

Intel offers a variety of information through the World Wide Web at http://www.intel.com.

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